

FDR8508P

Dual P-Channel, Logic Level, PowerTrench™ MOSFET

General Description

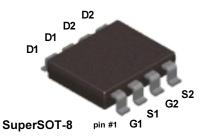
These P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on state resistance and yet maintain low gate charge for superior switching performance.

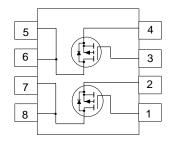
Applications

- · Load switch
- DC/DC converter
- Motor driving

Features

- -3.0 A, -30 V. $R_{DS(ON)} = 0.052\Omega$ @ $V_{GS} = -10V$ $R_{DS(ON)} = 0.086\Omega$ @ $V_{GS} = -4.5V$.
- Low gate charge. (8nC typical).
- High performance trench technology for extremely low $\boldsymbol{R}_{\text{DS(ON)}}$
- · High power and current handling capability.
- Small footprint (38% smaller than a standard SO-8); low profile package (1 mm thick); power handling capability similar to SO-8.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	FDR8508P	Units
V _{DSS}	Drain-Source Voltage	-30	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current - Continuous (Note 1a)	-3	А
	- Pulsed	-20	
P _D	Power Dissipation	0.8	W
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _e JA	Thermal Resistance, Junction-to-Ambient	(Note 1a)	156	°C/W
R _e JC	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

_ rackage marking and cracking information									
Device Marking	Device	Reel Size	Tape Width	Quantity					
.8508	FDR8508P	13"	12mm	3000 units					

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	racteristics		•	•		•
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-30			V
Δ BV _{DSS} / Δ T _J	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, Referenced to 25°C		24		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μΑ
I _{GSSF}	Gate-Body Leakage Current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
On Char	racteristics (Note 2)			•		
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-1	-1.8	-3	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μ A, Referenced to 25°C		-4		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -3 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -3 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = -4.5 \text{ V}, I_D = -2.3 \text{ A}$		0.040 0.057 0.058	0.052 0.078 0.086	Ω Ω Ω
I _{D(on)}	On-State Drain Current	V _{GS} = -10 V, V _{DS} = -5 V	-20			Α
g FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -3 \text{ A}$		9		mS
Dvnami	c Characteristics		•			
C _{iss}	Input Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$		750		pF
Coss	Output Capacitance	1		220		pF
C _{rss}	Reverse Transfer Capacitance	1		100		pF
Switchir	ng Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -15 \text{ V}, I_{D} = -1 \text{ A},$		12	22	ns
t _r	Turn-On Rise Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$		14	25	ns
t _{d(off)}	Turn-Off Delay Time	1		24	38	ns
t _f	Turn-Off Fall Time	1		16	27	ns
Qg	Total Gate Charge	$V_{DS} = -15 \text{ V}, I_{D} = -3\text{A},$		8	12	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -5 V$,		1.8		nC
Q _{gd}	Gate-Drain Charge	1		3		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings	•	•		
ls	Maximum Continuous Drain-Source				-0.67	Α
	Drain-Source Diode Forward	$V_{GS} = 0 \text{ V}, I_{S} = -0.67 \text{ A}$ (Note 2)		-0.75	-1.2	V

Notes:

1. R_{\text{\text{BJA}}} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{\text{\text{BJC}}} is guaranteed by design while R_{\text{\text{\text{\text{\text{e}CA}}}} is determined by the user's board design. R_{\text{\text{\text{\text{\text{\text{\text{BJA}}}}}} shown below for single device operation on FR-4 board instill air.}}





156°C/W when mounted on a 0.0025 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Characteristics

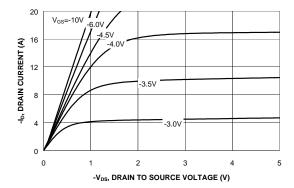


Figure 1: On-Region Characteristics

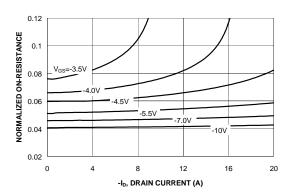


Figure 2: On-Resistance Variation vs Drain Current and Gate Voltage

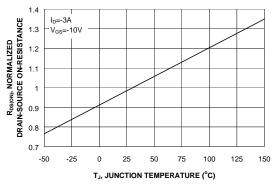


Figure 3: On-Resistance Variation vs Temperature

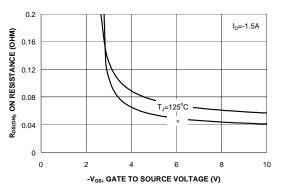


Figure 4: On-Resistance Variation vs Gate-To-Source Voltage

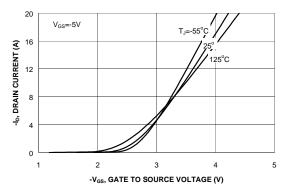


Figure 5: Transfer Characteristics

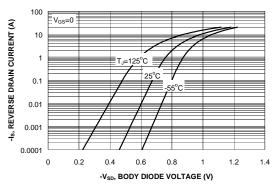


Figure 6: Body Diode Forward Voltage Variation vs Source Current and Temperature

Typical Characteristics (continued)

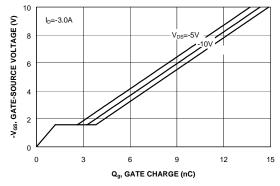


Figure 7: Gate-Charge Characteristics

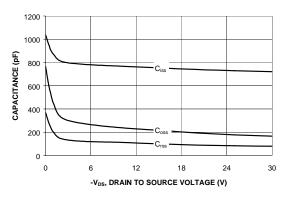


Figure 8: Capacitance Characteristics

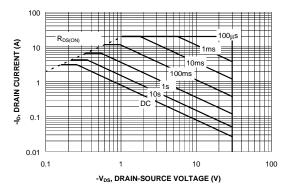


Figure 9: Maximum Safe Operating Area

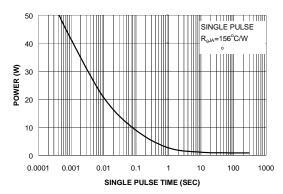


Figure 10: Single Pulse Maximum Power Dissipation

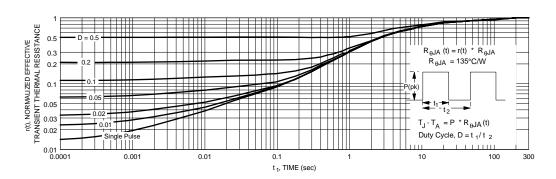
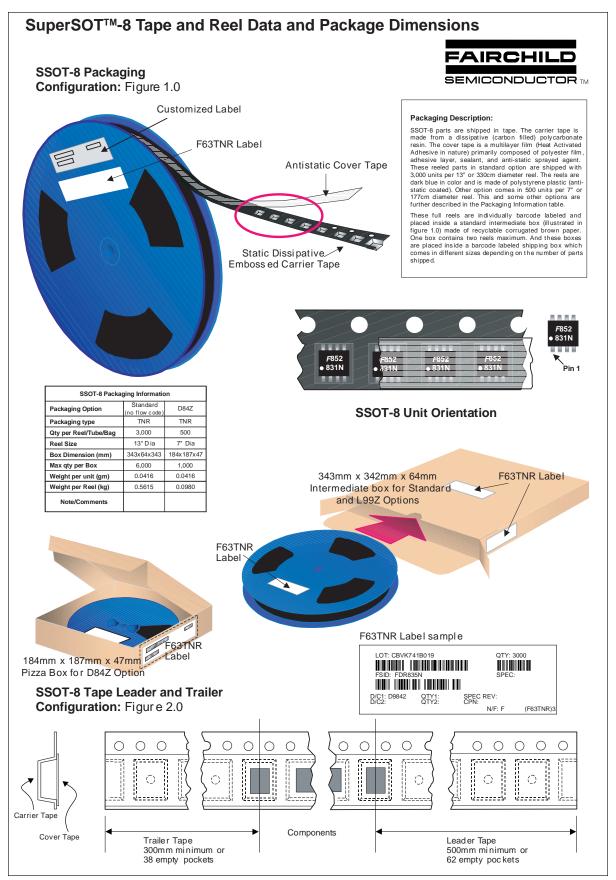
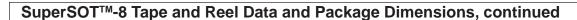


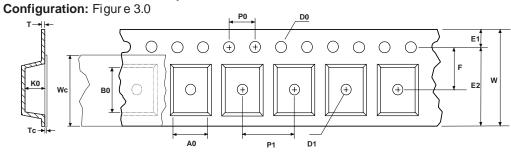
Figure 11. Transient Thermal Response Curve.

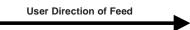
Thermal characterization performed using the conditions described in Note 1c. Transient themal response will change depending on the circuit board design.





SSOT-8 Embossed Carrier Tape



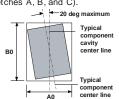


	Dimensions are in millimeter													
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
SSOT-8 (12mm)	4.47 +/-0.10	5.00 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.280 +/-0.150	9.5 +/-0.025	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

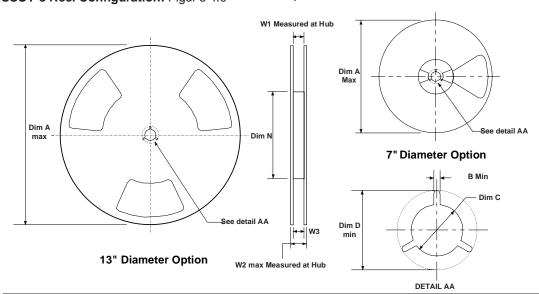


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

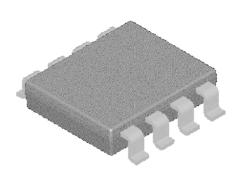
SSOT-8 Reel Configuration: Figur e 4.0

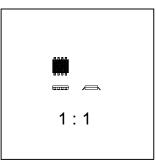


	Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)	
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4	

SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-8 (FS PKG Code 34, 35)

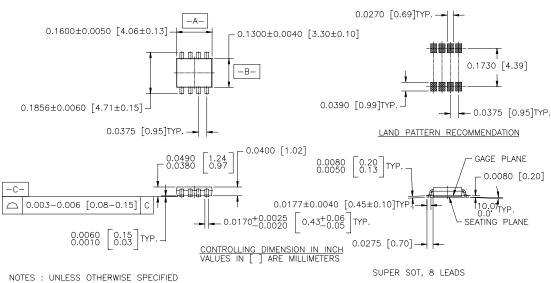




Scale 1:1 on letter size paper

Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 0.0416



STANDARD LEAD FINISH TI BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.

2. NO JEDEC REGISTRATION AS JAN. 1996

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CROSSVOLTTM POPTM

E²CMOS[™] PowerTrench[™]

FACTTM QSTM

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