19-4497; Rev 0; 7/09

High-Efficiency Power-Management IC with I²C Control for 2-Cell Li+ Battery Operated Devices

MAX8904

General Description

The MAX8904 power-management IC provides a complete power-supply solution for 2-cell Li+ handheld/Li-Poly applications such as point-of-sale terminals, digital SLR cameras, digital video cameras and ultra-mobile PCs.

The MAX8904 includes five step-down converters (1V2, 1V8, 3V3, 5V0, and ADJ) with internal MOSFETs and +1%/-3% accurate output voltages for processor core, memory, I/O, and other system power rail requirements. LCD backlighting is supported by a WLED boost converter that can provide 35mA for up to 8 WLEDs. This boost converter is also configurable as a 6-bit programmable voltage source that can provide up to 63mA of output current. A 500mA, internal MOSFET, current-limited switch (CLS), allows system designers to control input power to external peripheral devices.

The MAX8904 controls an external n-MOSFET for input overvoltage protection (13.5V, typ) and an external p-MOSFET for reverse polarity protection (up to -28V) of downstream circuits. System input current monitoring for power management is facilitated by an on-board current-sense amplifier (CSA) with differential inputs and a 1.2V full scale, ground-referenced analog output.

A 400kHz, I²C interface supports output voltage setting of the ADJ power rail and boost regulator (voltage source mode), WLED current setting for the boost regulator (WLED current regulator mode), GPIO control, and enable/disable of ADJ, 5V0, boost regulator, CSA blocks. The I²C interface also enables the host processor to read on-board fault status registers when interrupted by the MAX8904 $\overline{\text{FLT}}$ pin under system fault conditions.

An emergency shutdown input, $\overline{\text{SHDN}}$ allows converters preselected through I²C to turn off immediately under power-fail conditions, thus saving valuable firmware execution time. An uncommitted, active-low, 14V open-drain comparator (CMP) with a 1.25V internal reference is also provided in the MAX8904. The MAX8904 PWREN logic input turns on the 1V2, 1V8, 3V3, and 5V0 default power rails.

The MAX8904 is available in a 56-pin, 7mm x 7mm TQFN package.

Applications

Point-of-Sale Terminals
Digital Video Cameras
Digital SLR Cameras
Ultra-Mobile PCs

Pin Configuration appears at end of data sheet.

Features

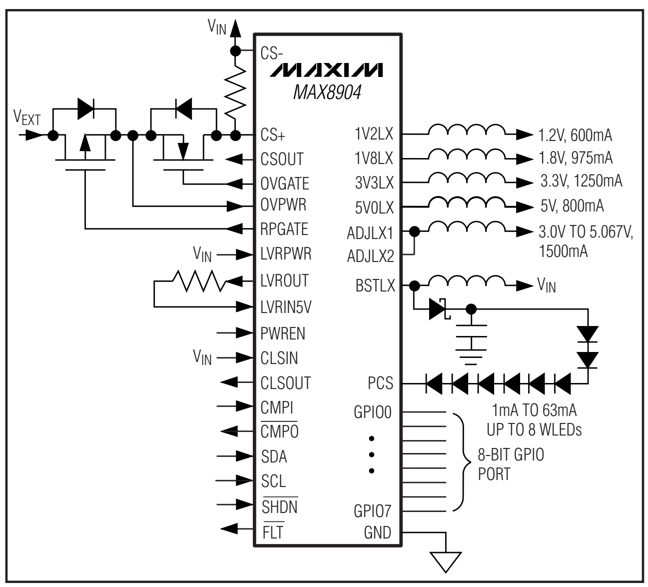
- ♦ **3.4V to 13.2V Input Voltage Range**
- ♦ **1MHz, Up to 90% Efficient, Synchronous DC-DC Step-Down Converters**
- ♦ **Power Converters 1V2, 1V8, and ADJ Operated Out-of-Phase with Respect to 3V3 and 5V0**
- ♦ **667kHz Step-Up Converter Provides Up to 32V Output for Driving Up to Eight WLEDs**
- ♦ **Internal Compensation on All Power Converters**
- ♦ **Fast Line and Load Transient Responses**
- ♦ **Internal Soft-Start and Short-Circuit Protection on All Power Converter Outputs**
- ♦ **Input Overvoltage and Reverse Polarity Protection**
- ♦ **250ms Fault Timer-Based Protection for Overload, Short Circuit**
- ♦ **I²C Serial Interface for On/Off Control, Output Voltage, WLED Current, GPIO Setting, Fault Monitoring**
- ♦ **< 15µA Standby Current Over Operating Voltage Range and Temperature**
- ♦ **Compact, 56-Pin, 7mm x 7mm TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8904ETN+T	-40°C to +85°C	56 THIN QFN-EP* (7mm x 7mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

OVPWR to GND..-0.3V to +30V
RPGATE to GND...-0.3V to +17V
OVPWR to RPGATE..-0.3V to +22V
OVGATE to CS+ ....-0.3V to +6V
BSTFB to GND...-0.3V to +40V
BSTLX to Exposed Pad (EP) ....-0.3V to +40V
BSTSW to BSTIN ....-16V to +0.3V
LVRPWR, BSTIN, BSTSW, 1V2IN, 3V3IN, 1V8IN, ADJIN,
5V0IN, CMPO, CLSIN to EP..............................-0.3V to +16V
GPIO_ to EP...-0.3V to +6V
CS+, CS- to GND ....-0.3V to +16V
CS+ to CS- ....-0.3V to +0.3V
CLSOUT to GND...................................-0.3V to (V_{CLSIN} + 0.3V)
LVROUT to GND...............................-0.3V to (V_{LVRPWR} + 0.3V)
1V2FB, 1V8FB, 3V3FB, 5V0FB, ADJFB, REF, CSOUT,
CMPI to GND ....-0.3V to ($V_{LVRIN5V}$ + 0.3V)
1V2BST to 1V2LX, 1V8BST to 1V8LX, 3V3BST to 3V3LX,
5V0BST to 5V0LX, ADJBST to ADJLX_................-0.3V to +6V
LVRIN5V, LVROUT, SHDN, PWREN, FLT, SDA, SCL,
GPIOPWR to GND ....-0.3V to +6V

PCS to GND ....-0.3V to (V_{BSTIN} + 0.3V)
EP to GND ....-0.3V to +0.3V
GPIOPWR to LVRIN5V...-6V to +0.3V
LVROUT to LVRIN5V ....-0.3V to +0.3V
ADJLX_, 5V0LX, 3V3LX, 1V8LX, 1V2LX,
BSTLX (Note 1)...±1.7A_{RMS}
Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN-EP Single-Layer PCB
(derate 27.8mW/°C above +70°C) 2222mW
56-Pin TQFN-EP Multilayer PCB
(derate 40mW/°C above +70°C) 3200mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2).....0.8°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2)
Single-Layer PCB ....36°C/W
Multilayer PCB ....25°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: _LX pins have internal clamp diodes to _IN and EP. Applications that forward bias these diodes should take care not to exceed the device's power-dissipation limits.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when $V_{\_IN}$ is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMMON BLOCKS						
Input Operating Supply Range	$V_{\_IN}$	$V_{\_IN}$ falling, OVP circuit not used	3.6		14	V
		$V_{\_IN}$ rising, OVP circuit not used	5.8		14	
		$V_{\_IN}$ falling, OVP circuit used	3.6		12.8	
		$V_{\_IN}$ rising, OVP circuit used	5.8		13.2	
Input Standoff Voltage	V_{OVPWR}				28	V
Standby Mode Supply Current	$I_{\_IN}$ + I_{LVRPWR} + $I_{CS\_}$	$V_{\_IN}$ = 13.2V; all channels off		5.5		µA
Quiescent Supply Current (CH7 + CH2 + CH3 + CH4 Only)	$\Delta I_{QLVRPWR}$ + I_{1V2IN} + I_{1V8IN} + I_{3V3IN} + I_{5V0IN} + I_{5V0FB}	No switching, V_{1V2FB} = 1.3V, V_{1V8FB} = 1.9V, V_{3V3FB} = 3.4V, V_{5V0FB} = 5.1V		100	165	µA

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when $V_{\_IN}$ is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REF Output Voltage	V_{REF}	I_{REF} = 0µA		1.240	1.250	1.260	V
		I_{REF} = 10µA			1.249		
OSC Frequency	f_{OSC}			0.9	1	1.1	MHz
LVROUT Output Voltage		5.4V < V_{LVRPWR} < 14V		4.9	5.1	5.3	V
LVRPWR Undervoltage Lockout Threshold		V_{LVRPWR} rising		5.3	5.55	5.8	V
		V_{LVRPWR} falling		3.2	3.4	3.6	
LVRIN5V Undervoltage Lockout Threshold		$V_{LVRIN5V}$ rising			3.45		V
		$V_{LVRIN5V}$ falling			2.6		
$\overline{SHDN}$ Input High Voltage	V_{IH}	3V < $V_{LVRIN5V}$ < 5.5V		1.6			V
$\overline{SHDN}$ Input Low Voltage	V_{IL}	3V < $V_{LVRIN5V}$ < 5.5V				0.5	V
$\overline{SHDN}$ Pullup Resistance to LVRIN5V					1		MΩ
$\overline{SHDN}$ Pulldown Resistance to GND					2		MΩ
PWREN Input High Voltage	V_{IH}	3.4V < V_{LVRPWR} < 14V		1.6			V
PWREN Input Low Voltage	V_{IL}	3.4V < V_{LVRPWR} < 14V				0.5	V
PWREN Pulldown Resistance					1		MΩ
PWREN Deglitch Delay		Rising			10		µs
$\overline{FLT}$ Output-Voltage Low	$V_{\overline{FLT}}$	$I_{\overline{FLT}}$ = 20mA		0		0.4	V
$\overline{FLT}$ Open-Drain Leakage Current		$V_{\overline{FLT}}$ = 5.5V	T_A = +25°C		0.01	0.1	µA
			T_A = +85°C		0.1		
FAULT Timer Delay	t_{FAULT}				250		ms
Overtemperature Warning Flag		Rising (Note 3) (bit D3 of register 0Dh)		110	120	130	°C
Overtemperature Warning Flag Hysteresis					10		°C
Thermal Shutdown Latch Threshold		(Note 3)		140	152	165	°C
INPUT VOLTAGE PROTECTION							
OVPWR Undervoltage Lockout Threshold		V_{OVPWR} rising		3.75	4	4.25	V
		V_{OVPWR} falling		2.7	2.85	3.0	
OVPWR_UVLO_Rising to OVGATE Startup Delay	$t_{STARTUP}$	V_{OVPWR} > $V_{OVPWR\_UVLO\_RISING}$			32		ms
OVP Threshold	V_{OVP}	V_{OVPWR} rising		13.3	13.65	14	V
		Hysteresis			0.17		
OVGATE Charge Current	I_{OVGATE_CHG}	V_{OVGATE} = 7.2V			10		µA
OVGATE Discharge Resistance	R_{DCHG}	V_{CS+} = 14.1V, V_{OVGATE} = 15.1V			40		Ω
RPGATE Pulldown Resistor	R_{RPGATE}				50		kΩ
RPGATE Clamp Voltage	V_{CLAMP}	14V ≤ V_{OVPWR} ≤ 28V			16	19	V

High-Efficiency Power-Management IC with I2C Control for 2-Cell Li+ Battery Operated Devices

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when $V_{\_IN}$ is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CH1 (CURRENT-LIMITED SWITCH)							
Current-Limited Switch On-Resistance	R_{ONCLS}	I_{CLS} = 400mA		200	300	425	m_
Current Limit	I_{LIMCLS}	V_{CLSIN} = 12V, V_{CLSOUT} = 9V		450		600	mA
Overcurrent Fault Latch-Off Delay	t_{OLFLT}				250		ms
Fault Voltage	V_{ACT}	V_{CLSIN} - V_{CLSOUT} > 1V, 150mV hysteresis			1		V
Thermal Loop Threshold	THM_{TH}	Current-limit-foldback temperature threshold (Note 3)		110	120	130	°C
CLSOUT Leakage Current	$I_{CLSOUTLKG}$	V_{CLSIN} = 14V, V_{CLSOUT} = 0	T_A = +25°C		0.01	1	µA
			T_A = +85°C		0.1		
CH2 (1V8 STEP-DOWN CONVERTER)							
Output Voltage	V_{1V8FB}	No load		1.800	1.818	1.836	V
Operating Frequency	f_{1V8LX}				1		MHz
Load Regulation					-2.5		%/A
Line Regulation		V_{1V8IN} = 3.4V to 14V			0.04		%/V
Idle-Mode Trip Level		(Note 4)			150		mA
1V8LX Leakage Current	$I_{1V8LXLKG}$	V_{1V8LX} = 0, 14V, V_{1V8IN} = 14V	T_A = +25°C	-5	0.01	+5	µA
			T_A = +85°C		0.1		
1V8BST Leakage Current	$I_{1V8BSTLKG}$	V_{1V8BST} = 5V + V_{1V8IN}	T_A = +25°C		0.01	0.1	µA
			T_A = +85°C		0.1		
Low-Side Switch On-Resistance	$R_{ONLS1V8}$				0.185		_
High-Side Switch On-Resistance	$R_{ONHS1V8}$				0.27		_
High-Side Switch Current Limit	$I_{LIMHS1V8}$			1.3	1.43	1.6	A
Low-Side Switch Turn-Off Current					10		mA
Output-OK (1V8OK) Threshold		(Bit D3 of register 0Fh)	Rising		94		%
			Falling		90		
Soft-Start Rate					1		V/ms
LX Discharge Resistance		PWREN = GND			350		_
Output-OK (1V8OK) Fault Blanking Time After Soft-Start Done					2		ms

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when $V_{\_IN}$ is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CH3 (3V3 STEP-DOWN CONVERTER)							
Output Voltage	V_{3V3FB}	No load		3.349	3.383	3.416	V
Operating Frequency	f_{3V3LX}				1		MHz
Load Regulation					-1.1		%/A
Line Regulation		V_{3V3IN} = 3.4V to 14V			0.04		%/V
Idle-Mode Trip Level		(Note 4)			150		mA
3V3LX Leakage Current	$I_{3V3LXLKG}$	V_{3V3LX} = 0, 14V, V_{3V3IN} = 14V	T_A = +25°C	-5	0.01	+5	µA
			T_A = +85°C		0.1		
3V3BST Leakage Current	$I_{3V3BSTLKG}$	V_{3V3BST} = 5V + V_{3V3IN}	T_A = +25°C		0.01	0.1	µA
			T_A = +85°C		0.1		
Low-Side Switch On-Resistance	$R_{ONLS3V3}$				0.185		_
High-Side Switch On-Resistance	$R_{ONHS3V3}$				0.185		_
High-Side Switch Current Limit	$I_{LIMHS3V3}$			1.8	2	2.2	A
Low-Side Switch Turn-Off Current					10		mA
Output-OK (3V3OK) Threshold		(Bit D4 of register 0Fh)	Rising		94		%
			Falling		90		
Maximum Duty Cycle					95		%
Soft-Start Rate					1		V/ms
LX Discharge Resistance		PWREN = GND			175		_
Output-OK (3V3OK) Fault Blanking Time After Soft-Start Done					2		ms
CH4 (5V0 STEP-DOWN CONVERTER)							
Output Voltage	V_{5V0FB}	No load		5.000	5.050	5.100	V
Operating Frequency	f_{5V0LX}				1		MHz
Load Regulation					-1.25		%/A
Line Regulation		V_{5V0IN} = 5.4V to 14V			0.04		%/V
Idle-Mode Trip Level		(Note 4)			60		mA
5V0LX Leakage Current	$I_{5V0LXLKG}$	V_{5V0LX} = 0, 14V, V_{5V0IN} = 14V	T_A = +25°C	-5	+0.01	+5	µA
			T_A = +85°C		0.1		
5V0BST Leakage Current	$I_{5V0BSTLKG}$	V_{5V0BST} = 5V + V_{5V0IN}	T_A = +25°C		0.01	0.1	µA
			T_A = +85°C		0.1		
Low-Side Switch On-Resistance	$R_{ONLS5V0}$				0.27		_
High-Side Switch On-Resistance	$R_{ONHS5V0}$				0.27		_
High-Side Switch Current Limit	$I_{LIMHS5V0}$			1.26	1.4	1.54	A
Low-Side Switch Turn-Off Current					10		mA

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when $V_{\_IN}$ is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output-OK (5V0OK) Threshold		(Bit D5 of register 0Fh)	Rising		94		%
			Falling		90		
Soft-Start Rate					1		V/ms
LX Discharge Resistance		PWREN = GND			350		_
Output-OK (5V0OK) Fault Blanking Time After Soft-Start Done					2		ms
CH5 (ADJ STEP-DOWN CONVERTER)							
Quiescent Supply Current	$\Delta(I_{QLVRPWR} + I_{5V0FB}) + I_{ADJIN}$	No switching (CH5 only), V_{ADJFB} = 4V, ADJSP register = 1Fh			65	100	µA
Output Voltage Adjust Range	V_{ADJFB}			3		5.067	V
Operating Frequency	$f_{ADJLX\_}$				1		MHz
Output Voltage Accuracy		No load		-1	0	+1	%
Load Regulation					-0.75		%/A
Line Regulation		V_{ADJIN} = 5.4V to 14V, V_{ADJFB} = 4V, ADJSP register = 1Fh			0.04		%/V
Idle-Mode Trip Level		(Note 4)			180		mA
ADJLX_ Leakage Current	$I_{ADJLX\_}$	V_{ADJLX} = 0, 14V, V_{ADJIN} = 14V	T_A = +25°C	-5	0.01	+5	µA
			T_A = +85°C		0.1		
ADJBST Leakage Current	$I_{ADJBSTLKG}$	V_{ADJBST} = 5V + V_{ADJIN}	T_A = +25°C		0.01	0.1	µA
			T_A = +85°C		0.1		
Low-Side Switch On-Resistance	$R_{ONLSADJ}$				0.185		_
High-Side Switch On-Resistance	$R_{ONHSADJ}$				0.185		_
High-Side Switch Current Limit	$I_{LIMHSADJ}$			2.7	3.0	3.3	A
Low-Side Switch Turn-Off Current					10		mA
Output-OK (ADJOK) Threshold		(Bit D6 of register 0Fh)	Rising		94		%
			Falling		90		
Soft-Start Rate					1		V/ms
LX Discharge Resistance		ADJEN = logic 0 (bit D3 of register 07h)			175		_
Output-OK (ADJOK) Fault Blanking Time After Soft-Start Done					2		ms
CH6 (BST STEP-UP CONVERTER)							
Quiescent Supply Current	$\Delta I_{QLVRPWR} + I_{BSTIN}$	No switching (CH6 only), BSTIV = logic 1 (bit D4 of register 09h), V_{BSTFB} = 14V, BSTVSP register (0Ch) = 0Fh			100		µA
Typical Output Voltage Range	V_{BSTFB}	Current mode		17.4		33.5	V
		Voltage mode (typical DAC codes)		12.5		18.7	
Overvoltage Protection Range		Current mode (typical DAC codes)		17.4		36	V
Overvoltage Protection Accuracy		Current mode, V_{BSTFB} = 26.7V		-3		+3	%

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when $V_{\_IN}$ is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Accuracy		Voltage mode, BSTVSP register (0Ch) = 10h		-3		+3	%
Operating Frequency	f_{BSTLX}				667		kHz
Minimum Duty Cycle					10		%
Maximum Duty Cycle				90	93	97	%
PCS Current Accuracy	I_{PCS}	BSTCSP register (0Bh) = 20h	T_A = +25°C	31.04	32	32.96	mA
			T_A = -40°C to +85°C	30.4		33.6	
PCS Leakage Current	I_{PCSLKG}	V_{PCS} = 0 to LVRIN5V	T_A = +25°C		0.01	1	µA
			T_A = +85°C		0.1		
BSTSW Leakage Current	$I_{BSTSWLKG}$	V_{BSTSW} = 0, V_{BSTIN} = 14V, BSTEN = logic 0 (bit D4 of Register 09h)	T_A = +25°C		0.01	5	µA
			T_A = +85°C		0.1		
BSTLX Leakage Current	$I_{BSTLXLKG}$	V_{BSTLX} = 0 to 36V	T_A = +25°C		0.01	5	µA
			T_A = +85°C		1		
BSTSW Switch On-Resistance	$R_{ONBSTSW}$				0.1		_
BSTLX Switch On-Resistance	$R_{ONBSTLX}$				0.3		_
BSTSW Switch Short-Circuit Current Limit	$I_{LIMBSTSW}$				1.35		A
BSTLX Switch Current Limit	$I_{LIMBSTLX}$				1.13		A
Output Voltage OK (BSTOK) Threshold		(Bit D7 of register 0Fh)	Rising, voltage mode only		95		%
			Falling, voltage mode only		90		
Soft-Start Time		Voltage mode and current mode			4.096		ms
BSTOK Fault Blanking Time After Soft-Start Done		Voltage mode and current mode			1.024		ms
CH7 (1V2 STEP-DOWN CONVERTER)							
Output Voltage	V_{1V2FB}	No load		1.200	1.212	1.224	V
Operating Frequency	f_{1V2LX}				1		MHz
Load Regulation					-2.5		%/A
Line Regulation		V_{1V2IN} = 3.4V to 14V			0.04		%/V
Idle-Mode Trip Level		(Note 4)			200		mA
1V2LX Leakage Current	$I_{1V2LXLKG}$	V_{1V2LX} = 0, 14V, V_{1V2IN} = 14V	T_A = +25°C	-5	0.01	+5	µA
			T_A = +85°C		0.1		
1V2BST Leakage Current	$I_{1V2BSTLKG}$	V_{1V2BST} = 5V + V_{1V2IN}	T_A = +25°C		0.01	0.1	µA
			T_A = +85°C		0.1		

High-Efficiency Power-Management IC with I²C Control for 2-Cell Li+ Battery Operated Devices

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when V_IN is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Side Switch On-Resistance	$R_{ONLS1V2}$				0.185		_
High-Side Switch On-Resistance	$R_{ONHS1V2}$				0.27		_
High-Side Switch Current Limit	$I_{LIMHS1V2}$			1.08	1.2	1.32	A
Low-Side Switch Turn-Off Current					10		mA
Output-OK (1V2OK) Threshold		(Bit D2 of register 0Fh)	Rising		94		%
			Falling		90		
Soft-Start Rate					1		V/ms
LX Discharge Resistance		PWREN = GND			175		_
Output-OK (1V2OK) Fault Blanking Time After Soft-Start Done					2		ms
CSA (CURRENT-SENSE AMPLIFIER)							
Differential Input Range	$V_{CS+} - V_{CS-}$	$V_{LVRPWR} = V_{CS-}$ = 5.4V to 14V		0		60	mV
Maximum CSOUT Output Capacitive Load	C_{LOAD}	(Note 3)				50	pF
CSOUT Pulldown Resistor	R_{PD}				350		k_
Bandwidth					150		kHz
Common-Mode Voltage Range	V_{CMR}			5.4		14	V
Common-Mode Rejection	CMR	$V_{LVRPWR} = V_{CS-}$ = 5.4V to 14V, $V_{CS+} = V_{CS-}$ + 24mV			100		dB
CS_ Input Current	$(I_{CS-} + I_{CS+})$	$V_{LVRPWR} = V_{CS-} = V_{CS+}$ = 5.4V to 13.2V			2	4	µA
CS+/CS- Input-Referred Offset	V_{IOCS}	Gain = 20, $V_{CS+} = V_{CS-} = V_{LVRPWR}$ = 5.4V to 14V		-2.0	0	+2.0	mV
CSOUT Voltage Accuracy		V_{LVRPWR} = 5.4V to 14V	$V_{CS+} - V_{CS-}$ = 48mV, gain = 20		1	5	%
			$V_{CS+} - V_{CS-}$ = 24mV, gain = 20		2	5	
			$V_{CS+} - V_{CS-}$ = 24mV, gain = 40		1	5	
CSOUT Load Current	I_{CSOUT}	$V_{CS+} - V_{CS-}$ = 48mV, gain = 20				20	µA
CS Flag (BIT D1 of Register 0Dh)		(Bit D6 of register 09h)	Rising, CSFLGEN = logic 1	0.912	0.96	1.008	V
			Falling, CSFLGEN = logic 1	0.862	0.91	0.958	
Start-Up Time						60	µs
CSOUT Clamp Voltage	$V_{CSOUTCLP}$			1.215	1.242	1.270	V

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when V_IN is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GPIO LOGIC INPUT/OUTPUT							
GPIOPWR UVLO		Rising			2.8		V
		Falling			2.5		
Input Threshold		Rising		0.7 x $V_{GPIOPWR}$			V
		Falling				0.25 x $V_{GPIOPWR}$	
Output-Voltage Low		$I_{GPIO\_}$ = -20mA, open-drain output				0.5	V
Open-Drain Leakage Current		$V_{GPIO\_}$ = 5.5V	T_A = +25°C		0.01	0.1	µA
			T_A = +85°C		0.1		
Minimum Input Data Setup Time	t_{DS}				100		ns
Minimum Input Data Hold Time	t_{DH}				1		µs
Minimum Delay to Output Data Valid					5		µs
Pullup Resistor from GPIO_ to GPIOPWR		$V_{GPIOPWR}$ = 5V	Input mode		1		M_
			Open-drain output mode		10		k_
GPIO_ PWM Clock Frequency					244		Hz
OPEN-DRAIN COMPARATOR							
CMPI Input Current	I_{CMPI}	V_{CMPI} = 600mV			0.01		µA
CMPI Threshold	V_{CMPI}	Rising		1.2125	1.25	1.2875	V
CMPI Hysteresis	$V_{CMPIHYS}$				40		mV
$\overline{CMPO}$ Delay	$t_{\overline{CMPO}}$	25mV overdrive			5		µs
Output-Voltage Low	$V_{\overline{CMPO}}$	$I_{\overline{CMPO}}$ = -20mA				0.4	V
Open-Drain Leakage Current	$I_{CMPOLKG}$	$V_{\overline{CMPO}}$ = 14V	T_A = +25°C		0.01	1.0	µA
			T_A = +85°C		0.1		

ELECTRICAL CHARACTERISTICS (continued)

($V_{\_IN}$ = 7.2V, EP = GND, V_{PWREN} = 5V, _LX unconnected, C_{REF} = 0.1µF; when $V_{\_IN}$ is specified, it implies all _IN pins; T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C SERIAL INPUT/OUTPUT AND LOGIC						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.0			V
Input Leakage Current	I_{LKG}		-1		+1	µA
Output-Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Input/Output Capacitance	$C_{I/O}$			10		pF
Serial-Clock Frequency	f_{SCL}				400	kHz
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
BUS Free Time	t_{BUF}		1.3			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Data-In Setup Time	$t_{SU:DAT}$		100			ns
Data-In Hold Time	$t_{HD:DAT}$		0		900	ns
Receive SCL/SDA Minimum Rise Time	t_R	(Note 5)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Rise Time	t_R	(Note 5)		300		ns
Receive SCL/SDA Minimum Fall Time	t_F	(Note 5)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Fall Time	t_F	(Note 5)		300		ns
Transmit SDA Fall Time	t_F	C_{BUS} = 400pF	20 + 0.1 x C_{BUS}		300	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 6)		50		ns
SEQUENCER						
POWER-UP SEQUENCING						
1V8 VOK to 3V3 Start Delay				3.6		ms
POWER-DOWN SEQUENCING						
3V3 Disable to 1V8 Disable Delay				15		ms
1V8 Disable to 1V2 Disable Delay				15		ms

Note 3: Not tested. Design guidance only.

Note 4: The idle-mode current threshold is the transition point between fixed-frequency PWM operation and idle-mode operation. The specification is given in terms of output load current for inductor values specified in Figure 1.

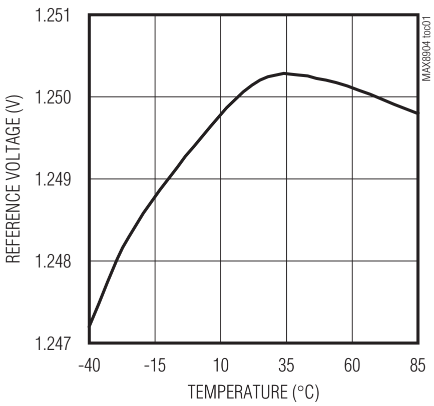
Note 5: C_{BUS} = total capacitance of one bus line in pF. Rise and fall times are measured between 0.1 x V_{BUS} and 0.9 x V_{BUS}.

Note 6: Input filters on SDA and SCL suppress noise spikes < 50ns.

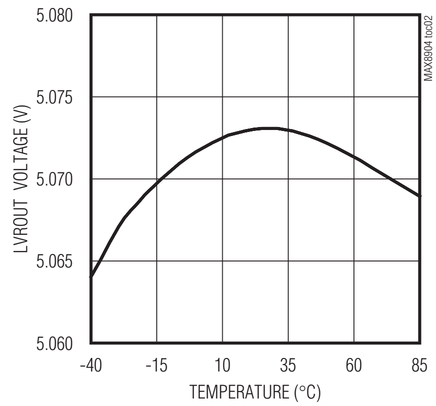
Typical Operating Characteristics

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

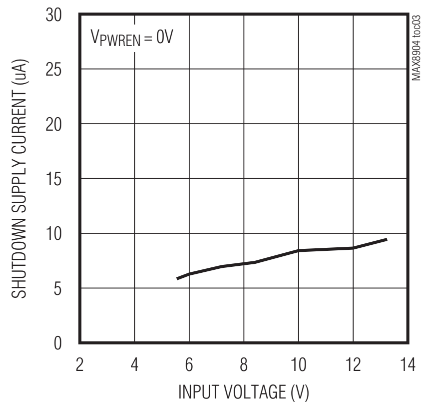
REFERENCE VOLTAGE vs. TEMPERATURE



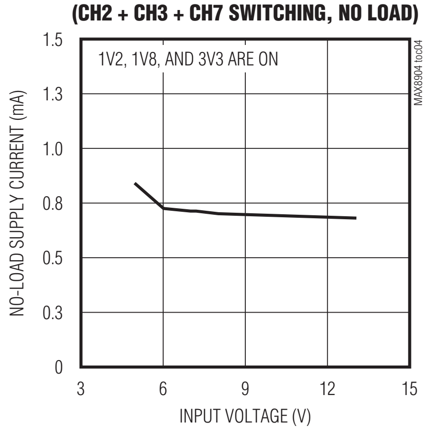
LVROUT VOLTAGE vs. TEMPERATURE



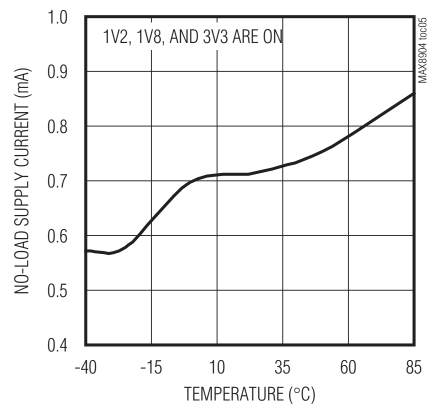
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



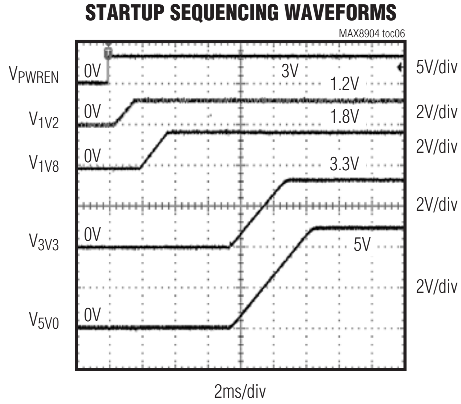
INPUT CURRENT vs. INPUT VOLTAGE (CH2 + CH3 + CH7 SWITCHING, NO LOAD)



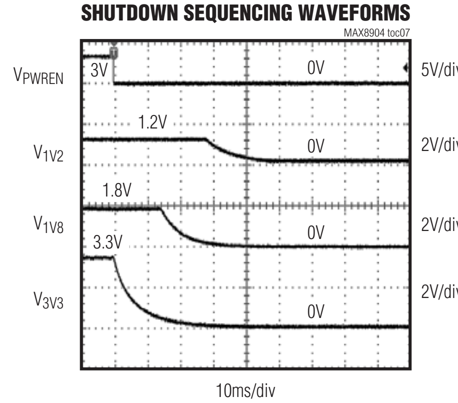
INPUT CURRENT vs. TEMPERATURE (CH2 + CH3 + CH7, SWITCHING, NO LOAD)



STARTUP SEQUENCING WAVEFORMS



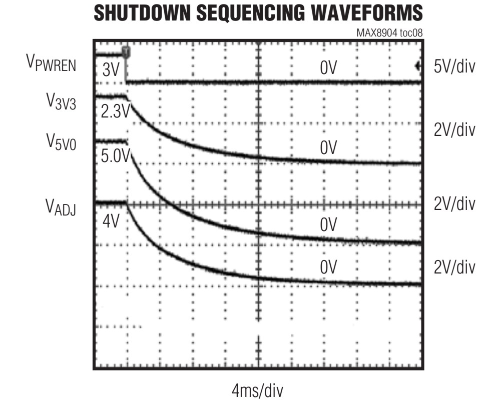
SHUTDOWN SEQUENCING WAVEFORMS



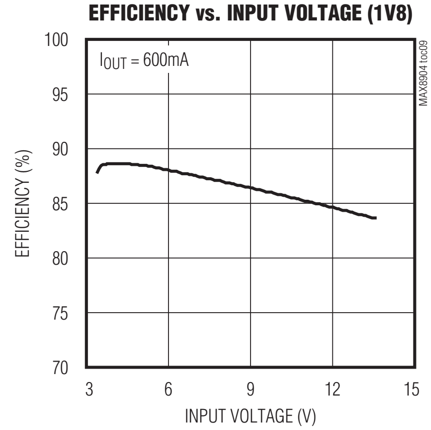
Typical Operating Characteristics (continued)

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

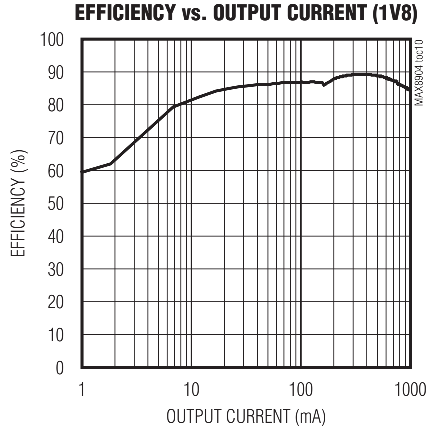
SHUTDOWN SEQUENCING WAVEFORMS



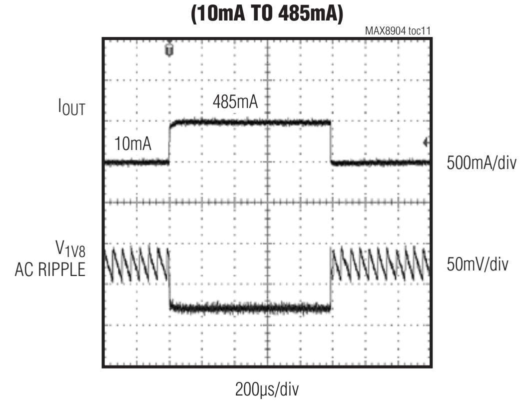
EFFICIENCY vs. INPUT VOLTAGE (1V8)



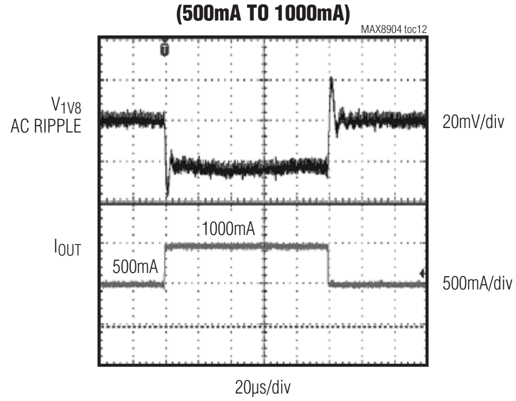
EFFICIENCY vs. OUTPUT CURRENT (1V8)



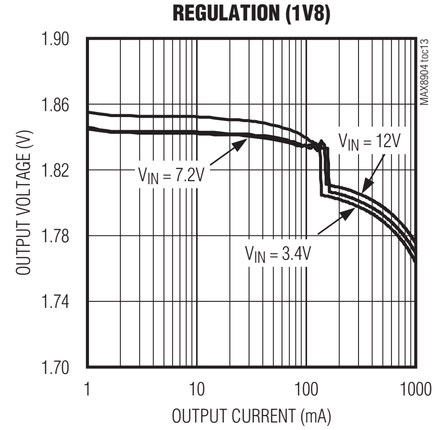
1V8 LOAD TRANSIENT RESPONSE (10mA TO 485mA)



1V8 LOAD TRANSIENT RESPONSE (500mA TO 1000mA)



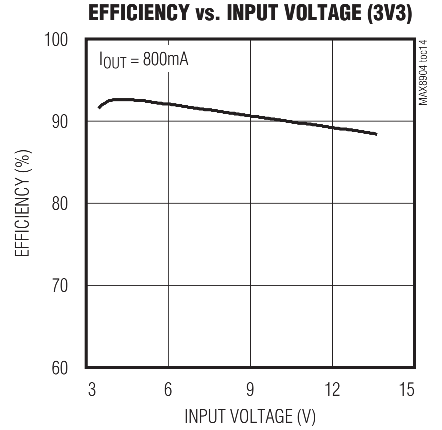
OUTPUT VOLTAGE LOAD REGULATION (1V8)



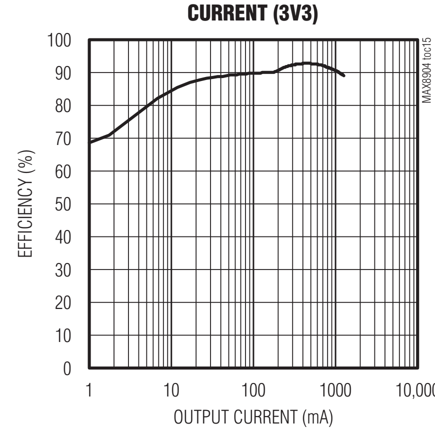
Typical Operating Characteristics (continued)

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

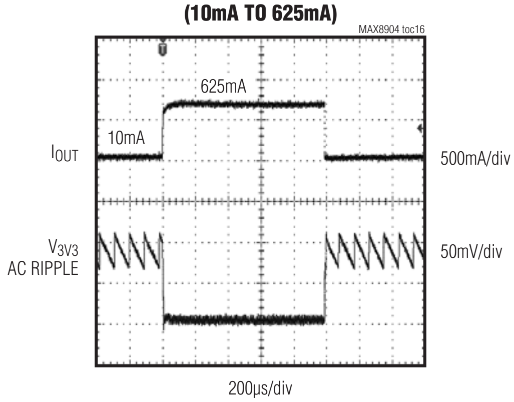
EFFICIENCY vs. INPUT VOLTAGE (3V3)



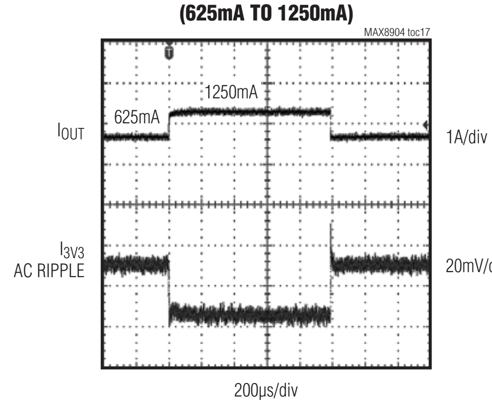
EFFICIENCY vs. OUTPUT CURRENT (3V3)



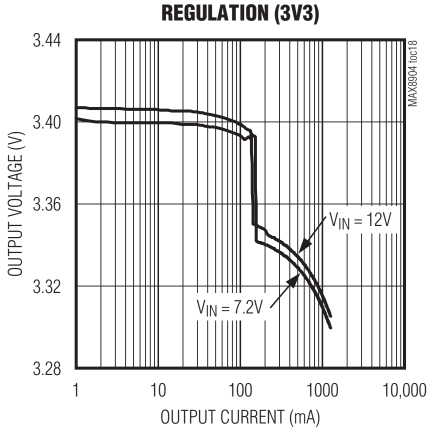
3V3 LOAD TRANSIENT RESPONSE (10mA TO 625mA)



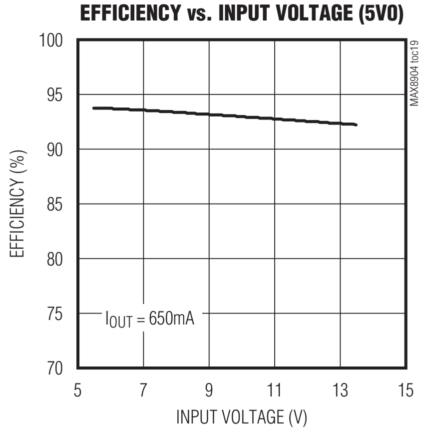
3V3 LOAD TRANSIENT RESPONSE (625mA TO 1250mA)



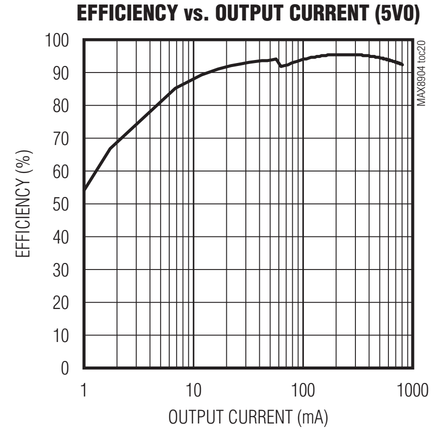
OUTPUT VOLTAGE LOAD REGULATION (3V3)



EFFICIENCY vs. INPUT VOLTAGE (5V0)



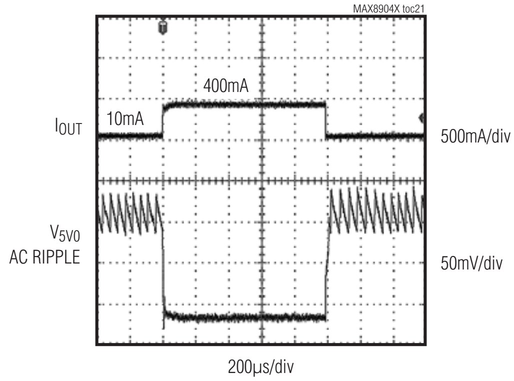
EFFICIENCY vs. OUTPUT CURRENT (5V0)



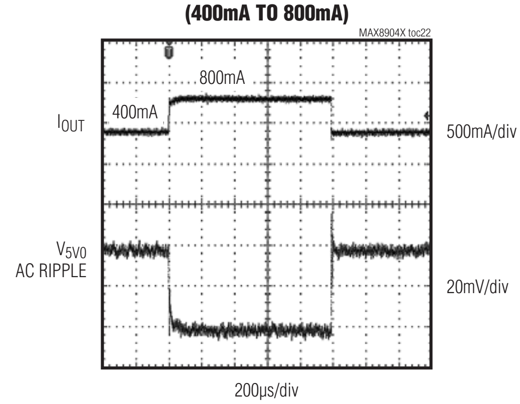
Typical Operating Characteristics (continued)

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

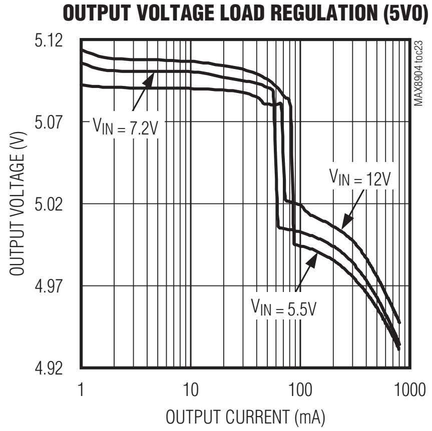
5V0 LOAD TRANSIENT RESPONSE (10mA TO 400mA)



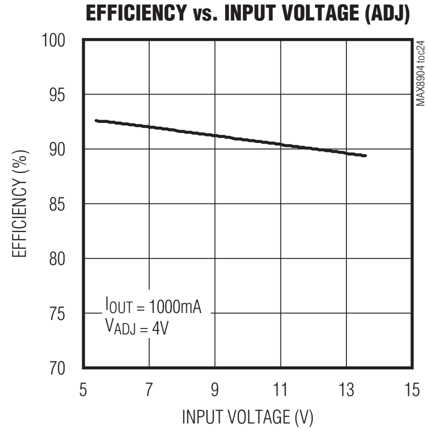
5V0 LOAD TRANSIENT RESPONSE (400mA TO 800mA)



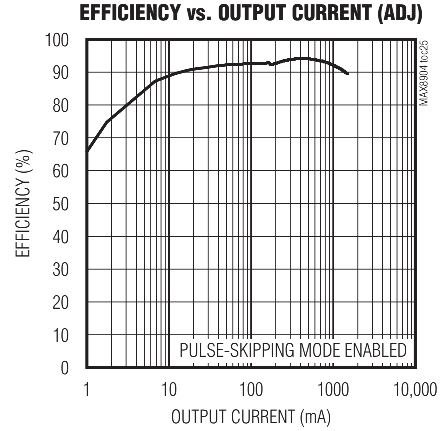
OUTPUT VOLTAGE LOAD REGULATION (5V0)



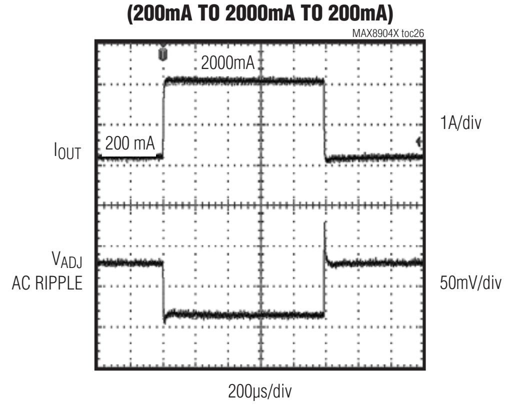
EFFICIENCY vs. INPUT VOLTAGE (ADJ)



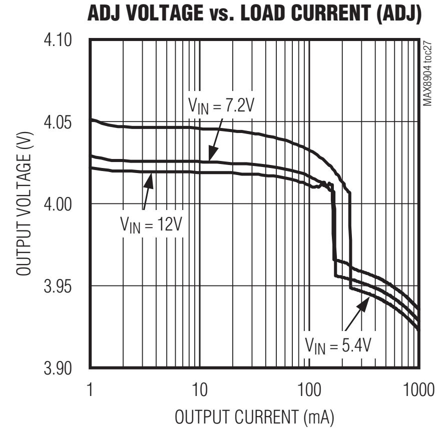
EFFICIENCY vs. OUTPUT CURRENT (ADJ)



ADJ LOAD TRANSIENT RESPONSE (200mA TO 2000mA TO 200mA)



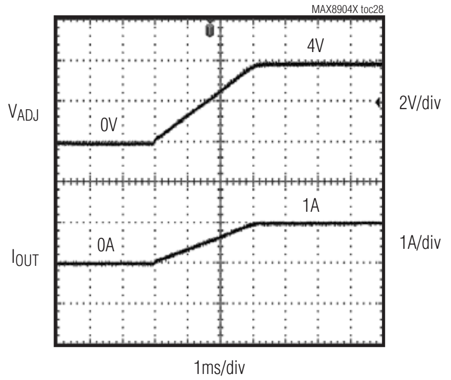
ADJ VOLTAGE vs. LOAD CURRENT (ADJ)



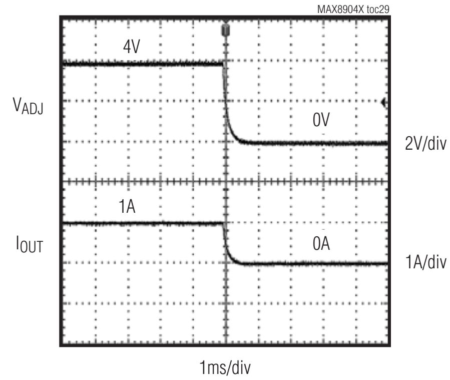
Typical Operating Characteristics (continued)

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

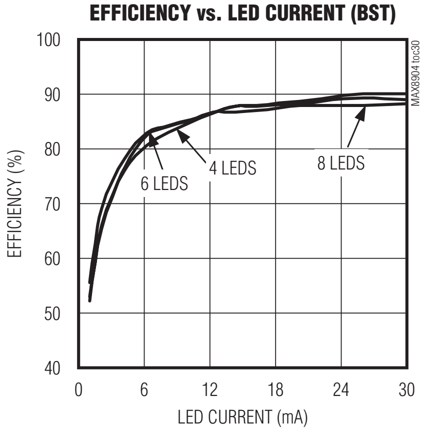
ADJ STARTUP RESPONSE



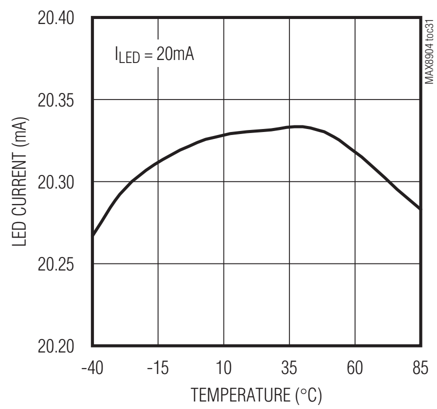
ADJ SHUTDOWN RESPONSE



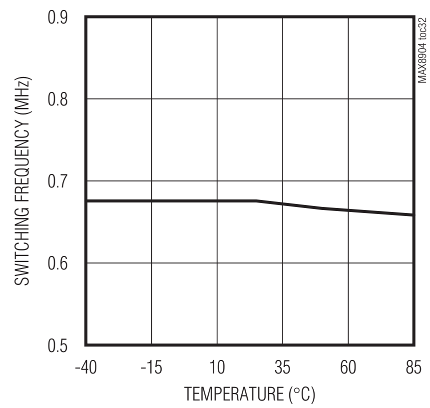
EFFICIENCY vs. LED CURRENT (BST)



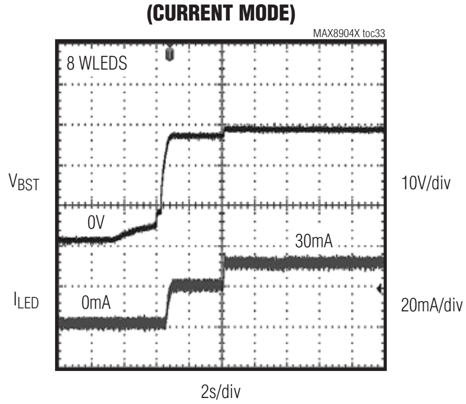
LED CURRENT vs. TEMPERATURE



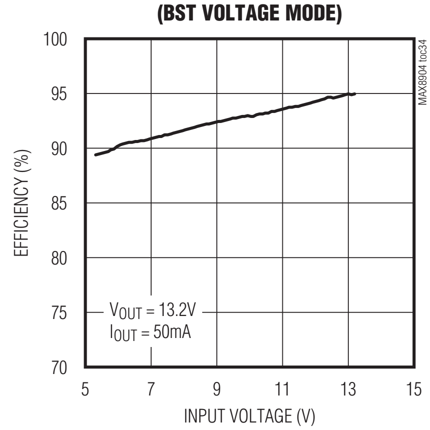
BST SWITCHING FREQUENCY vs. TEMPERATURE



BST STARTUP RESPONSE (CURRENT MODE)



EFFICIENCY vs. INPUT VOLTAGE (BST VOLTAGE MODE)

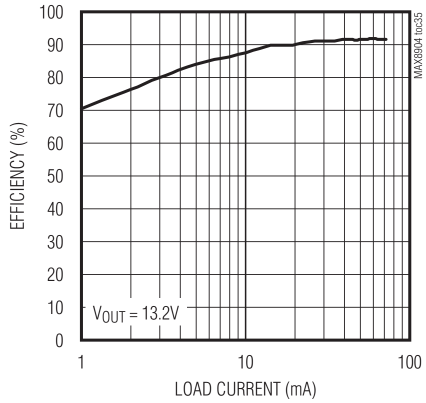


High-Efficiency Power-Management IC with I²C Control for 2-Cell Li+ Battery Operated Devices

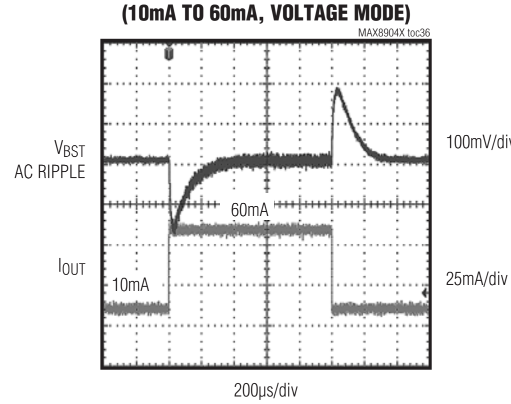
Typical Operating Characteristics (continued)

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

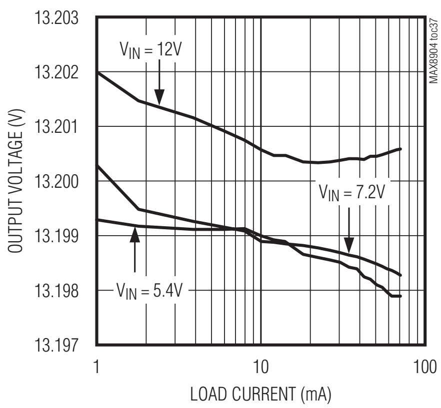
EFFICIENCY vs. LOAD CURRENT (BST VOLTAGE MODE)



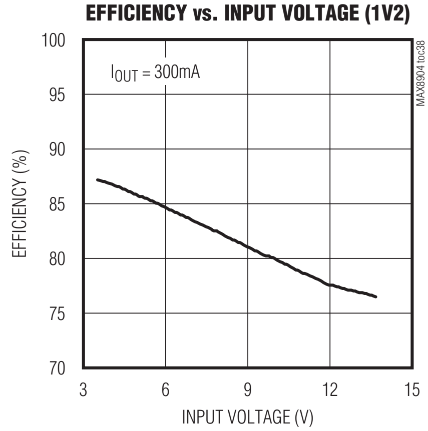
BST LOAD TRANSIENT RESPONSE (10mA TO 60mA, VOLTAGE MODE)



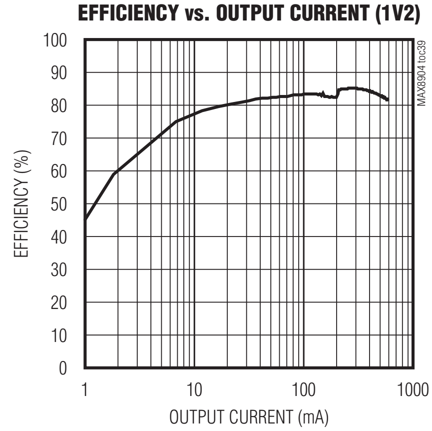
BST VOLTAGE vs. LOAD CURRENT



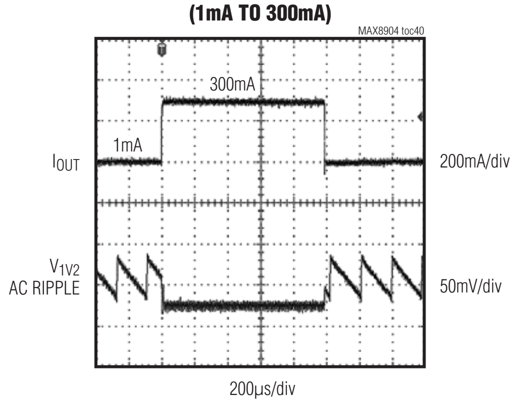
EFFICIENCY vs. INPUT VOLTAGE (1V2)



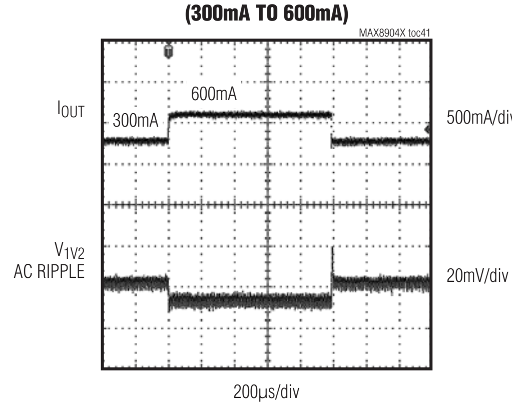
EFFICIENCY vs. OUTPUT CURRENT (1V2)



1V2 LOAD TRANSIENT RESPONSE (1mA TO 300mA)



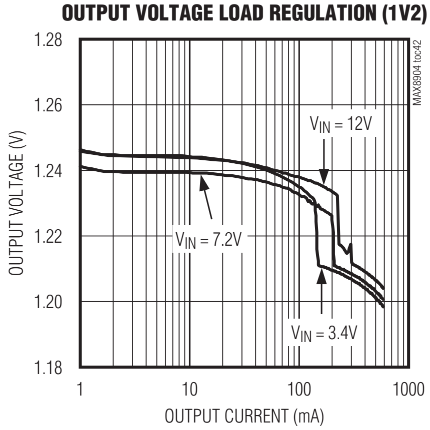
1V2 LOAD TRANSIENT RESPONSE (300mA TO 600mA)



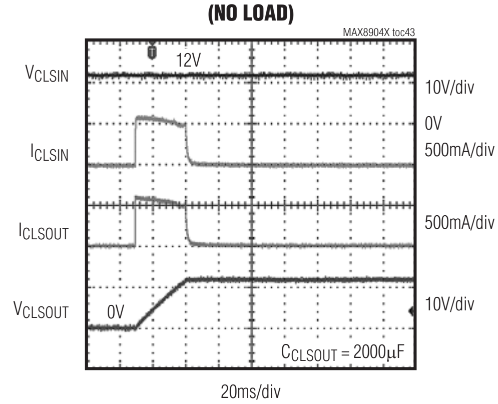
Typical Operating Characteristics (continued)

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

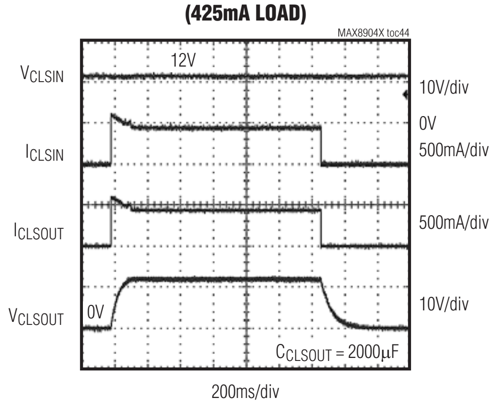
OUTPUT VOLTAGE LOAD REGULATION (1V2)



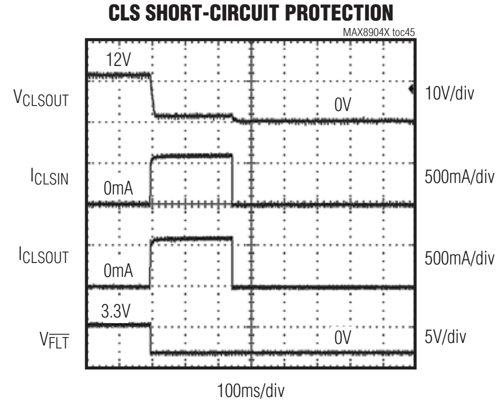
CLS STARTUP RESPONSE (NO LOAD)



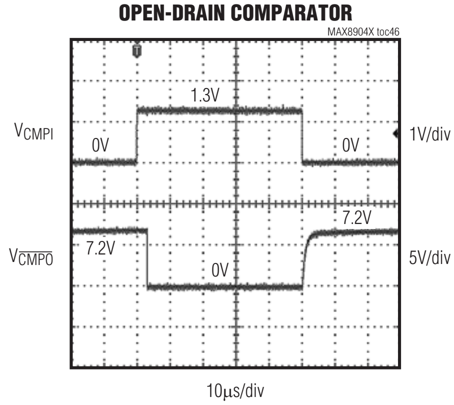
CLS STARTUP AND SHUTDOWN RESPONSE (425mA LOAD)



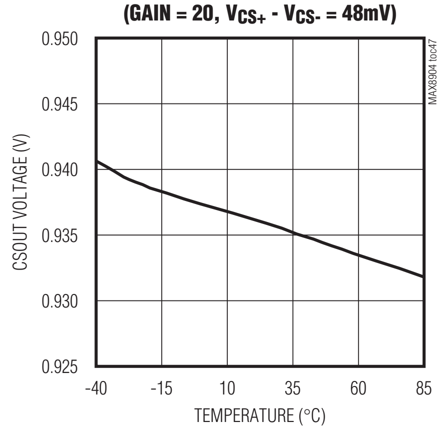
CLS SHORT-CIRCUIT PROTECTION



OPEN-DRAIN COMPARATOR



CSOUT VOLTAGE vs. TEMPERATURE (GAIN = 20, V_{CS+} - V_{CS-} = 48mV)



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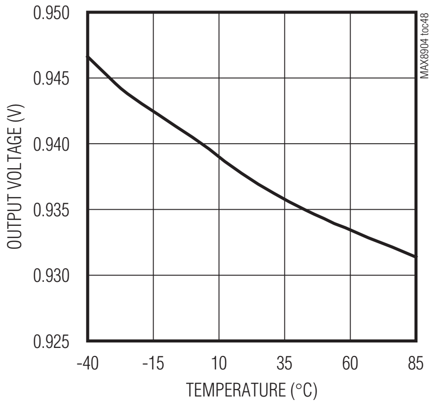
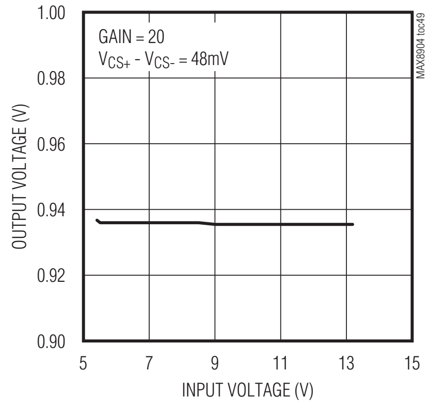
Typical Operating Characteristics (continued)

(V_{IN} = 7.2V, V_{PWREN} = 3V, $\overline{SHDN}$ unconnected, V_{ADJ} = 4V, C_{REF} = 0.1µF, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

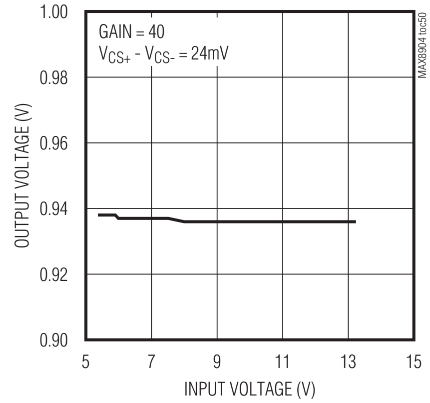
CSOUT VOLTAGE vs. TEMPERATURE (GAIN = 40, V_{CS+} - V_{CS-} = 24mV)



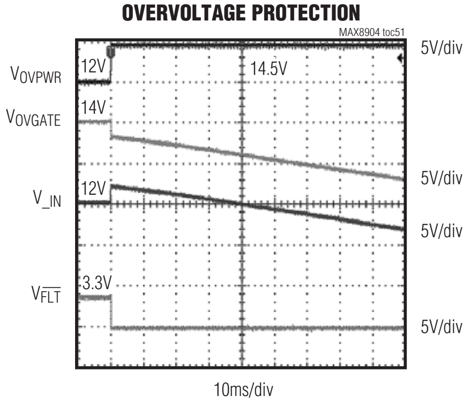
CSA OUTPUT VOLTAGE vs. INPUT VOLTAGE



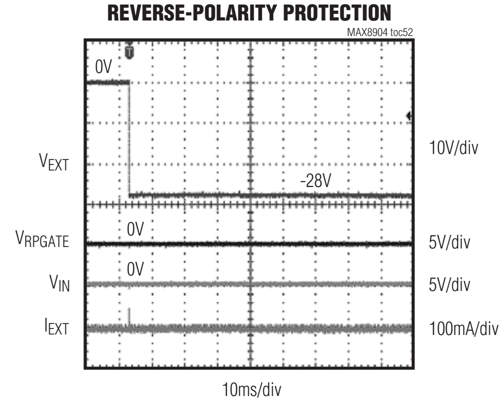
CSA OUTPUT VOLTAGE vs. INPUT VOLTAGE



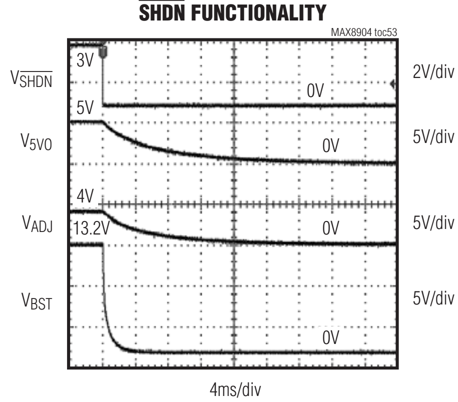
OVERVOLTAGE PROTECTION



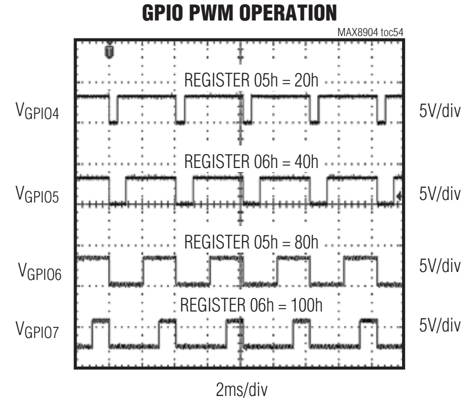
REVERSE-POLARITY PROTECTION



$\overline{SHDN}$ FUNCTIONALITY



GPIO PWM OPERATION



Pin Description

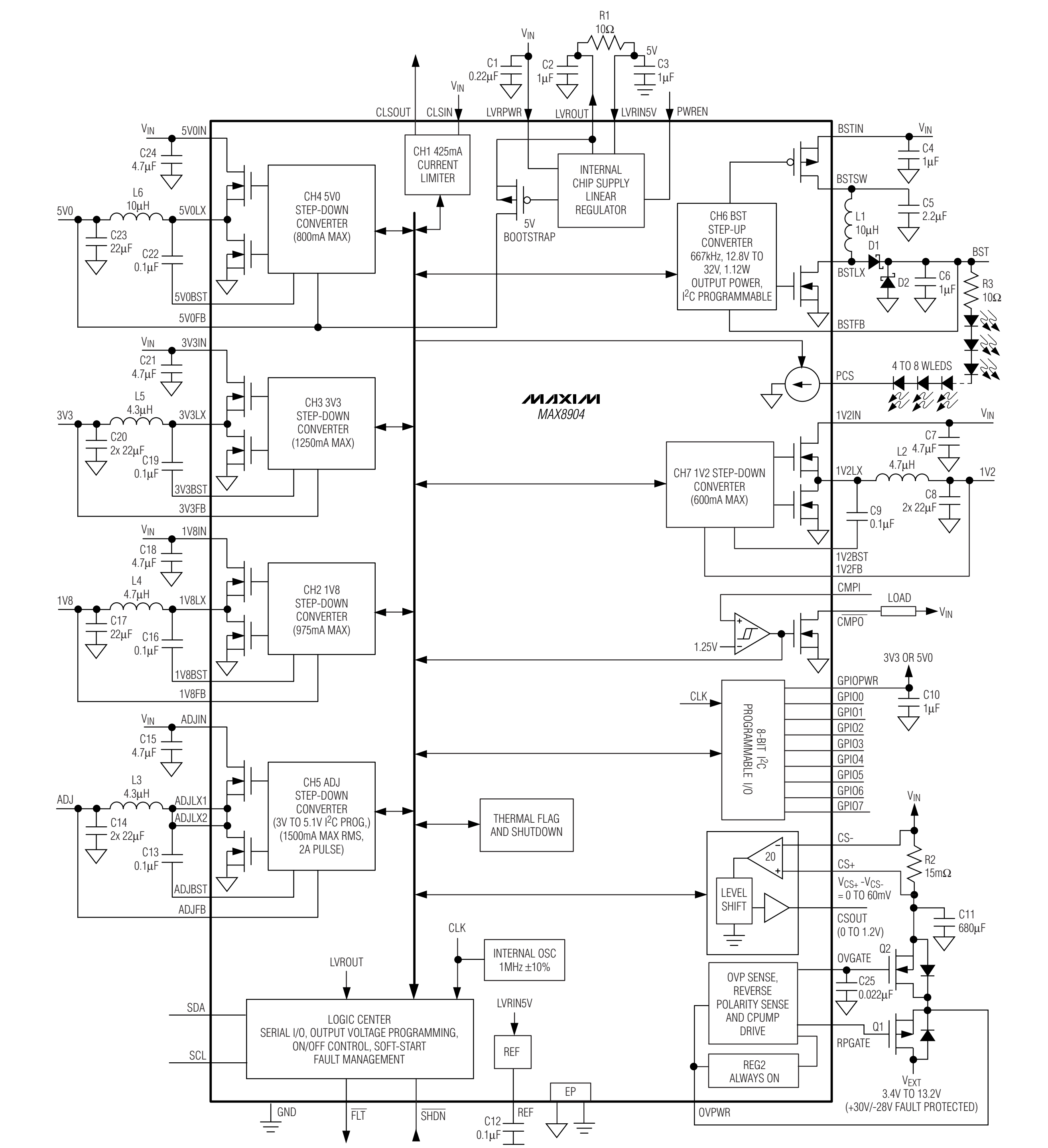
PIN	NAME	FUNCTION
1	CSOUT	Output Voltage of the Current-Sense Amplifier. CSOUT is referenced to analog ground, GND. Its full-scale voltage is 1.2V for 60mV differential input voltage at CS+ and CS-.
2	RPGATE	External p-MOSFET Gate Control Node for Reverse Polarity Protection. Internal reverse polarity sense circuitry controls the gate so that power is applied to the following n-MOSFET stage if and only if proper (positive) polarity of power is applied. If reverse polarity input power is applied, the p-MOSFET is kept off to protect the n-MOSFET stage and the IC.
3	OVPWR	Supply Voltage and Overvoltage Detection Node for the Overvoltage Protection Circuitry. Connect OVPWR to system external supply in the absence of reverse polarity protection p-MOSFET. When reverse polarity protection p-MOSFET is used, connect OVPWR to the source of the reverse polarity protection p-MOSFET.
4	OVGATE	External n-MOSFET Gate Control Node for Input Overvoltage Protection. The external n-MOSFET is turned on as long as V_{OVPWR} is less than 13.3V. The external n-MOSFET is immediately turned off by pulling OVGATE low, when V_{OVPWR} exceeds 13.3V, and the IC asserts the $\overline{FLT}$ output. The external n-MOSFET is turned back on when V_{OVPWR} falls below OVP threshold. Note that the I^2C interface is always alive, is independent of the overvoltage protection circuit, and turns off only when V_{LVROUT} falls below 3.4V.
5	ADJBST	ADJ Step-Down Converter Boost Capacitor Connection. Connect a 0.1µF ceramic capacitor between ADJBST and ADJLX_.
6, 7	ADJLX1, ADJLX2	ADJ Step-Down Converter Switching Node. Connect an inductor between ADJLX_ and the output of the ADJ converter. Connect a 0.1µF ceramic capacitor between ADJLX_ and ADJBST. Connect ADJLX1 to ADJLX2.
8	ADJIN	ADJ Step-Down Converter Supply Input. Bypass ADJIN to power ground with a 4.7µF ceramic capacitor. Connect ADJIN to the input power supply node, V_{IN}.
9	ADJFB	ADJ Step-Down Converter Feedback Input. Connect two 22µF or a 47µF output ceramic capacitor from the output inductor to power ground, and route the sense trace to ADJFB.
10	REF	1.25V Reference Output. Bypass REF to GND with a 0.1µF ceramic capacitor. REF is internally pulled to GND in shutdown.
11	GND	Ground. Connect GND to the ground plane. Connect the ground plane with a short wide connection to the exposed pad (EP).
12	LVRIN5V	Power Supply for the Internal Analog Circuitry. It is derived from an internal low-voltage regulator output, LVROUT. Connect a 10_ resistor between LVRIN5V and LVROUT. Bypass LVRIN5V to GND with a 1.0µF or greater ceramic capacitor.
13	LVROUT	Internal Low-Voltage Regulator Output Bootstrapped to 5V0 Step-Down Converter Output. LVROUT is the power supply for the internal drive circuitry. LVROUT provides a 5V output when PWREN is pulled high. Bypass LVROUT to power ground with a 1.0µF or greater ceramic capacitor.
14	LVRPWR	Internal 5V Low-Voltage Linear Regulator Input Supply. Decouple LVRPWR to power ground with a 0.22µF or greater ceramic capacitor. Connect LVRPWR to the input power-supply node, V_{IN}.
15	5V0FB	5V0 Step-Down Converter Feedback Input. Connect a 22µF output ceramic capacitor from the output inductor to power ground, and route the sense trace to 5V0FB.
16	5V0IN	5V0 Step-Down Converter Input Supply. Bypass 5V0IN to power ground with a 10µF ceramic capacitor. Connect 5V0IN to the input power-supply node, V_{IN}.

Pin Description (continued)

PIN	NAME	FUNCTION
17	5V0LX	5V0 Step-Down Converter Switching Node. Connect an inductor between 5V0LX and the output of the 5V0 converter. Connect a 0.1µF capacitor between 5V0LX and 5V0BST.
18	5V0BST	5V0 Step-Down Converter Boost Capacitor Connection. Connect a 0.1µF ceramic capacitor between 5V0BST and 5V0LX.
19	GPIOPWR	Power Supply for GPIO Inputs and Outputs. GPIOPWR can be connected to a supply voltage from 3.0V up to 5.5V. Correct a 1µF ceramic capacitor between GPIOPWR and GND.
20–27	GPIO0–GPIO7	I^2C-Controlled GPIO Port. GPIO_ can be configured as: • Schmitt-trigger inputs with internal 1M pullup resistor to GPIOPWR • Open-drain outputs with internal 10k pullup resistor off-state and capable of sinking 20mA current from GPIOPWR • Open-drain outputs with high-impedance off-state and capable of sinking 20mA current from GPIOPWR • High-impedance outputs The default configuration during power-up is Schmitt-trigger inputs until reconfigured through the I^2C interface. The GPIO block has a dedicated power input supply, GPIOPWR. The MAX8904 samples its GPIO0 at GPIOPWR power-up and selects one of two internal hardwired slave addresses for I^2C addressing.
28	$\overline{\text{CMPO}}$	Active-Low, Open-Drain Output of an Uncommitted Comparator. $\overline{\text{CMPO}}$ can be pulled up to 14V.
29	CMPI	Comparator Input. Internal reference voltage is 1.25V.
30	3V3FB	3V3 Step-Down Converter Feedback Input. Connect two 22µF or a 47µF output ceramic capacitor from the inductor to power ground, and route the sense trace to 3V3FB. The 3V3FB provides power to the I^2C registers. Connect the SDA and SCL pullup resistors to 3V3FB.
31	3V3IN	3V3 Step-Down Converter Input Supply. Connect a 4.7µF ceramic capacitor between 3V3IN and power ground. Connect 3V3IN to the input power supply node, V_{IN}.
32	3V3LX	3V3 Step-Down Converter Switching Node. Connect an inductor between 3V3LX and the output of the 3V3 converter. Connect a 0.1µF ceramic capacitor between 3V3LX and 3V3BST.
33	3V3BST	3V3 Step-Down Converter Boost Capacitor Connection. Connect a 0.1µF ceramic capacitor between 3V3BST and 3V3LX.
34	SCL	I^2C Serial-Clock Input
35	SDA	I^2C Serial-Data Input/Output. Data is read on the rising edge of SCL.
36	1V2BST	1V2 Step-Down Converter Boost Capacitor Connection. Connect a 0.1µF ceramic capacitor between 1V2BST and 1V2LX.
37	1V2LX	1V2 Step-Down Converter Switching Node. Connect an inductor between 1V2LX and the output of the 1V2 converter. Connect a 0.1µF ceramic capacitor between 1V2LX and 1V2BST.
38	1V2IN	1V2 Step-Down Converter Input Supply. Bypass 1V2IN to power ground with a 4.7µF ceramic capacitor. Connect 1V2IN to the input power supply node, V_{IN}.
39	1V2FB	1V2 Step-Down Converter Feedback Input. Connect two 22µF or a 47µF output ceramic capacitor from the inductor to power ground, and route sense trace to 1V2FB. 1V2FB is sampled at power-up to determine if the 1V2 step-down converter is used or not. See the *Power-Up/Down Sequencing for 1V2, 1V8, 3V3, and 5V0 Supplies* section. Pull 1V2FB to LVRIN5V to configure the IC for operation without the 1V2 step-down converter.
40	$\overline{\text{FLT}}$	Active-Low, Open-Drain Fault Output. Low $\overline{\text{FLT}}$ indicates a fault condition. See the *Fault Handling* section for details.

Pin Description (continued)

PIN	NAME	FUNCTION
41	$\overline{SHDN}$	Shutdown Input. When $\overline{SHDN}$ is pulled low, the power converters that are selected in the SHUTDOWN register, if currently active, are immediately shut down. The IC recognizes a valid signal on $\overline{SHDN}$ only if 1V2, 1V8, and 3V3 supplies are in regulation.
42	PWREN	Enable Input. When PWREN is driven high, the LVROUT regulator is turned on, and the 1V2, 1V8, 3V3, and 5V0, are turned on with correct sequencing depending on the status of 1V2FB at LVR power-up. When PWREN is pulled low, the MAX8904 turns off all converters and internal blocks and goes into low-power standby mode.
43	TEST	Test Pin. Leave as no connection. Do not connect power or ground.
44	1V8FB	1V8 Step-Down Converter Feedback Input. Connect a 22µF output ceramic capacitor from the output inductor to power ground, and route the sense trace to 1V8FB.
45	1V8IN	1V8 Step-Down Converter Input Supply. Bypass 1V8IN to power ground with a 4.7µF ceramic capacitor. Connect the 1V8IN to the input power supply node, V_{IN}.
46	1V8LX	1V8 Step-Down Converter Switching Node. Connect an inductor between 1V8LX and the output of 1V8 converter. Connect a 0.1µF ceramic capacitor between 1V8LX and 1V8BST.
47	1V8BST	1V8 Step-Down Converter Boost Capacitor Connection. Connect a 0.1µF ceramic capacitor between 1V8BST and 1V8LX.
48	BSTLX	BST Open-Drain Switch Node. Connect an inductor between BSTSW and BSTLX. BSTLX is high impedance in standby mode.
49	BSTSW	BST True Shutdown Switch Terminal. Connect an inductor between BSTSW and BSTLX. Bypass BSTSW to power ground with a 2.2µF ceramic capacitor.
50	BSTIN	BST Step-Up Converter Supply Input. Bypass BSTIN to power ground with a 1µF ceramic capacitor. Connect BSTIN to the input power supply node, V_{IN}.
51	BSTFB	BST Step-Up Converter Feedback Input. Connect BSTFB to the output ceramic capacitor of the step-up converter. Use a 1µF capacitor in current regulator mode and use a 10µF capacitor for voltage regulator mode.
52	PCS	LED Current Sink. When the BST step-up converter is in current-mode operation, connect the cathode of WLED string to PCS and the anode of the WLED string to the output capacitor. In voltage mode, PCS must be connected to GND.
53	CLSOUT	Current-Limited Switch Output. Turn on the load switch through the I²C interface to connect the switch input, CLSIN, to the load.
54	CLSIN	Current-Limited Switch Input. Connect CLSIN to the input power supply node, V_{IN}.
55	CS-	Current-Sense Amplifier Inverting Input. Connect CS- to the load side of current-sense resistor.
56	CS+	Current-Sense Amplifier Noninverting Input. Connect CS+ to the supply-side of current-sense resistor.
—	EP	Exposed Pad. Power grounds and ground plane must be star-connected to the EP. All large currents from converters flow through the exposed pad that also acts as a heat sink. A large number of vias are needed to connect EP to board power ground plane.



NOTE: 1V2, 1V8, AND ADJ OPERATE IN PHASE. 3V3 AND 5V0 OPERATE INPHASE WITH RESPECT TO EACH OTHER, BUT ARE DELAYED BY 300ns WITH RESPECT TO 1V2, 1V8, AND ADJ.

Figure 1. Typical Application Circuit and Function Diagram

Detailed Description

The MAX8904 power-management ICs provide a complete power-supply solution for 2-cell Li+ handheld/Li-Poly applications such as point-of-sale terminals, digital SLR cameras, digital video cameras, and ultra-mobile PCs.

The MAX8904 include five step-down converters (1V2-0.6A, 1V8-0.975A, 3V3-1.25A, 5V0-0.8A, and ADJ-1.5A) with internal MOSFETs and +1%/-3% accurate output voltages for processor core, memory, I/O, and other system power rail requirements. The ADJ converter provides an adjustable output voltage that is 6-bit programmable through the I²C interface from 3.0V to 5.1V, in 33.3mV steps.

LCD backlighting is supported by a WLED boost converter that can provide 35mA for up to 8 WLEDs while operating in the current regulator mode. This boost converter is also configurable as a 6 bit programmable voltage source that can provide up to 63mA of output current. In this voltage mode, the output voltage is 6-bit programmable through the I²C interface from 12.5V to 18.7V, in 100mV steps.

System input current monitoring for power management is facilitated by an on-board Current Sense Amplifier (CSA) with differential inputs and a 1.2V full scale ground referenced analog output. The CSA has an I²C programmable gain of 20V/V and 40V/V for full-scale outputs of 4A and 2A, respectively, when used with a 15mΩ current-sense resistor.

A 400kHz, I²C interface supports output voltage setting of ADJ power rail and boost regulator (voltage source mode), WLED current setting for the boost regulator (WLED current regulator mode), enable/disable of ADJ, 5V0, boost regulator, CSA and GPIO control. The I²C interface also enables the host processor to read on-board fault status registers when interrupted by the MAX8904 $\overline{\text{FLT}}$ pin under system fault conditions. An emergency shutdown input, $\overline{\text{SHDN}}$ allows converters preselected through I²C to turn off immediately, thus saving valuable firmware execution time under power fail conditions.

The MAX8904 features an 8-bit GPIO port controller with PWM capability. The GPIO port pins power up as Schmitt-trigger CMOS inputs. Programmable configurations are:

- Schmitt-trigger input with internal 1MΩ pullup to GPIOPWR
- Open-drain output, with internal 10kΩ pullup resistor off-state, capable of sinking up to 20mA current from GPIOPWR
- Open-drain output with high-impedance state, capable of sinking up to 20mA current from GPIOPWR
- High-impedance output

GPIO0 can be used to set the I²C slave address of the MAX8904 to either CEh or 8Eh (see Table 1).

A current-limited switch (CLS) is provided, with a minimum output current of 425mA, which allows system designers to control input power to external peripheral devices.

The MAX8904 supports input overvoltage protection (OVP) at 13.5V (typ) by controlling an external n-MOSFET and reverse polarity protection (down to -28V) of downstream circuits by controlling an external p-MOSFET.

An uncommitted, active-low, high voltage open-drain comparator (CMP) with a 1.25V internal reference and 20mA sink current capability that can function as a buzzer driver or can be used for power fail sensing is also provided.

The MAX8904's PWREN logic input turns on 1V2, 1V8, 3V3, and 5V0 default power rails. An internal 5V low-voltage linear regulator powered from the input power source provides power for the internal drive and control blocks. When the input is below 5V, the regulator output follows the input down to 3.4V. When the input voltage drops below 3.4V (UVLO), all circuitry except the overvoltage protection block are turned off. When the input voltage drops below 2.85V (OVPWR UVLO), the overvoltage protection block is turned off.

I²C Interface

The MAX8904 internal I²C serial interface provides flexible control setup, including ON/OFF control of all power converters (except 1V2, 1V8, and 3V3), CLS, CSA and CMP, the ADJ output voltage, the BST output voltage or output current, and the 8-bit GPIO port functionality. The MAX8904 internal control and fault status registers are also accessed through the standard bi-directional, 2-wire I²C serial interface. The I²C serial interface consists of a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between the master and the slave. The MAX8904 is a slave-only device, relying upon a master to generate a clock signal. The master (typically a microprocessor) initiates data transfer on the bus and generates SCL to permit data transfer. The MAX8904 supports SCL clock rates up to 400kHz.

I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

I2C Slave Address

A bus master initiates communication with MAX8904 as a slave device by issuing a START condition followed by the MAX8904 address. As shown in Table 1, the MAX8904 responds to either one of two internally hard-wired slave addresses depending on the GPIO0 status when GPIOPWR powers up for the first time and exceeds its UVLO (rising) threshold. This address is latched internally and can only be changed if the LVRPWR voltage is cycled, and the GPIOPWR voltage exceeds UVLO again.

Pullup Voltage

The MAX8904 I2C interface SDA and SCL line should use the 3V3 supply as its pullup voltage.

START and STOP Conditions

Both SDA and SCL remain high when the serial interface is inactive. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the MAX8904, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2). Both START and STOP conditions are generated by the bus master.

To send a series of commands to the MAX8904, the master issues REPEATED START (Sr) commands instead of a STOP command to maintain the bus control. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the MAX8904 internally disconnect SCL from the bus until the next START condition to minimize digital noise and feedthrough.

Data Transfer

Each data bit, from the most significant bit to the least significant bit, is transferred one by one during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

Each transmit sequence is framed by a START condition and a STOP condition. Each data packet is nine bits long: eight bits of data followed by an acknowledge bit.

Acknowledge

Both the I2C bus master and the MAX8904 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A) signal, the receiving device pulls SDA low before the rising edge

Table 1. MAX8904 Slave Addresses

GPIO0 STATUS AT $V_{GPIOPWR} > V_{GPIOPWR\_UVLO}$ (RISING)	SLAVE ADDRESS READ	SLAVE ADDRESS WRITE
Logic 0 (GPIO0 pulled down by an internal 100k resistor between GPIO0 and GND)	8Fh	8Eh
Logic 1 (GPIO0 pulled up by an internal 1M resistor between GPIO0 and GPIOPWR)	CFh	CEh

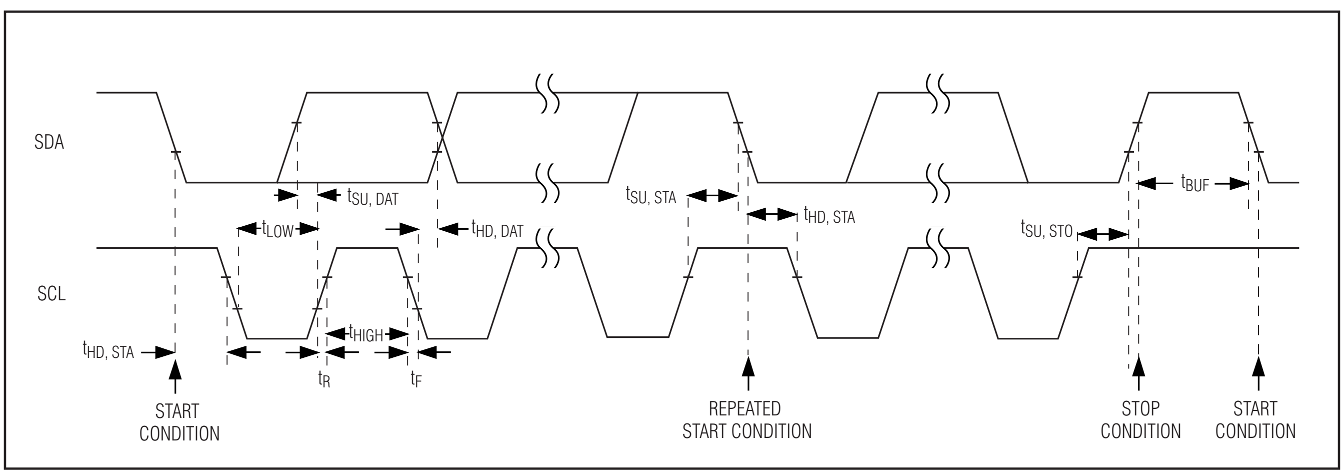


Figure 2. 2-Wire Serial Interface Timing Detail

of the acknowledge-related clock pulse (ninth pulse) and keeps it low during the high period of the clock pulse (Figure 3). To generate a not-acknowledge (NA) signal, the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Communication Protocols

The following I²C communication protocols are supported by the MAX8904:

- Writing to a single register
- Writing multiple bytes using register-data pairs
- Reading from a single register
- Reading from sequential registers

Writing to a Single Register

Figure 4 shows the protocol for the master device to write one byte of data to the MAX8904. The write byte protocol is as follows:

1) The master sends a START (S) command.
2) The master sends the 7-bit slave address followed by a write bit (low).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data
8) The slave acknowledges the data byte.
9) The master sends a STOP (P) condition.

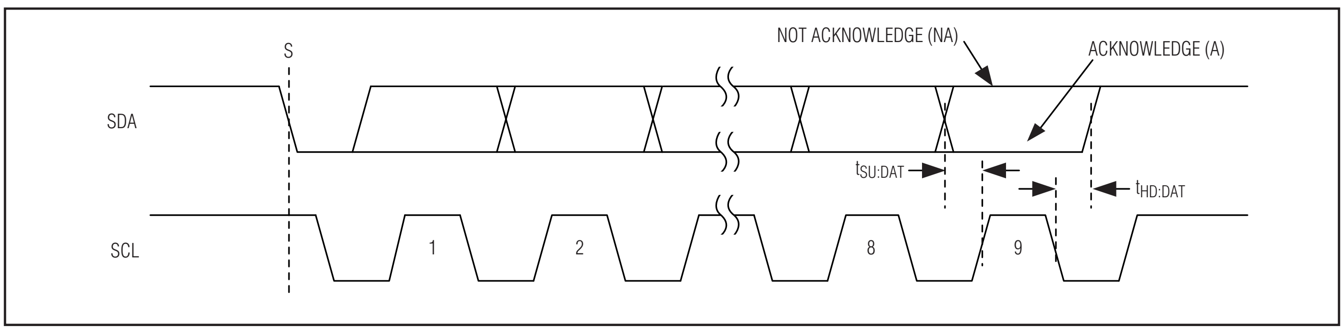


Figure 3. Acknowledge

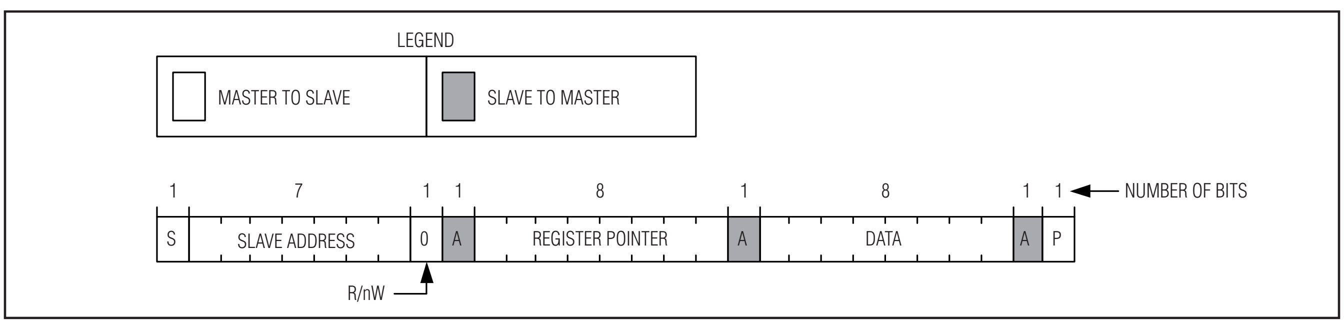


Figure 4. Write-Byte Format

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Writing Multiple Bytes Using Register-Data Pairs

Figure 5 shows the protocol for the master device to write multiple bytes to the MAX8904 using register-data pairs. It allows the master to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a STOP (P) condition. The write multiple bytes using register-data pairs protocol is as follows:

1) The master sends a START (S) command.
2) The master sends the 7-bit slave address followed by a write bit (low).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) Steps 5 to 8 are repeated as many times as the master requires. Registers may be accessed in random order.
10) The master sends a STOP (P) condition.

Reading from a Single Register

Figure 6 shows the protocol for the master device to read one byte of data from the MAX8904. The read byte protocol is as follows:

1) The master sends a START (S) command.
2) The master sends the 7-bit slave address followed by a write bit (low).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START (Sr) command.

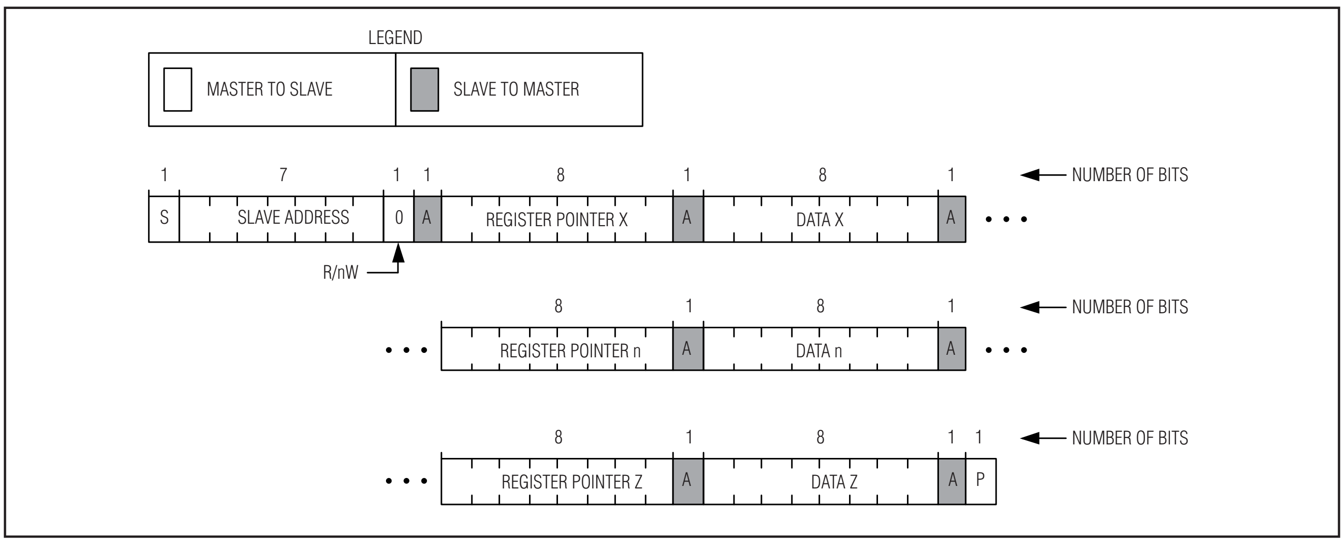


Figure 5. Multiple Bytes Register-Data Pair Format

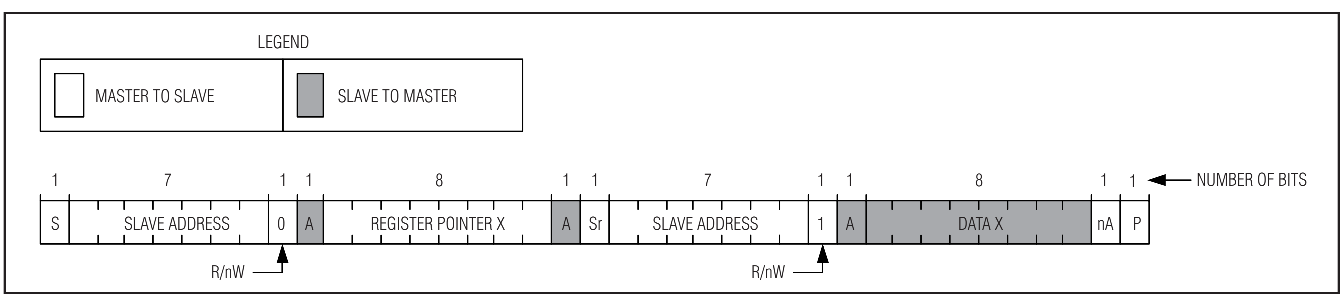


Figure 6. Read-Byte Format

7) The master sends the 7-bit slave address followed by a read bit (high).
8) The addressed slave asserts an acknowledge (A) by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master asserts a not-acknowledge on the data line to complete operations.
11) The master issues a STOP (P) condition.

Reading from Sequential Registers

Figure 7 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except that the master issues an acknowledge to signal the slave that it wants more data. When the master has all the data, it issues a not-acknowledge (NA) and a STOP condition (P) to end the transmission. The continuous read from sequential registers protocol is as follows:

1) The master sends a START (S) command.
2) The master sends the 7-bit slave address followed by a write bit (low).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START (Sr) command.
7) The master sends the 7-bit slave address followed by a read bit (high).
8) The addressed slave asserts an acknowledge by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues an acknowledge (A) signaling the slave that more data is needed.
11) Steps 9 and 10 are repeated as many times as the master requires. Following the last byte of data, the master issues a not-acknowledge (NA) to signal that it wishes to stop receiving data.
12) The master issues a STOP (P) condition.

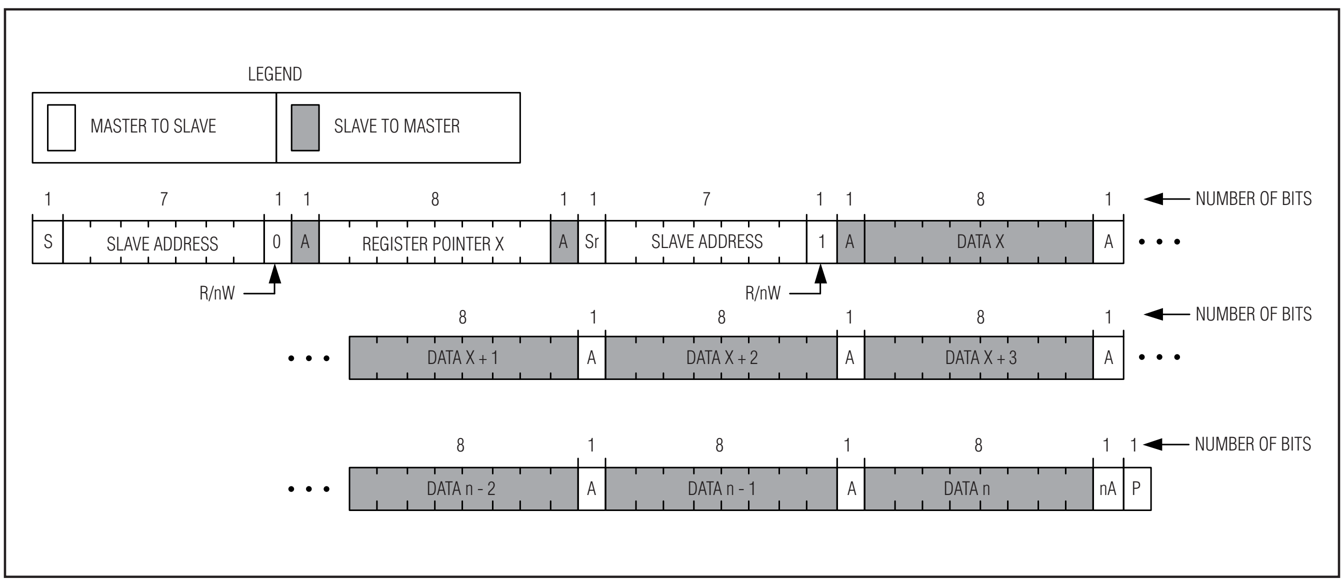


Figure 7. Read from Sequential Registers Format

I²C Accessible Registers

The I²C accessible registers are used to store all the control information from the SDA line and configure the MAX8904 for different operating conditions. Recycling power at LVRPWR causes the MAX8904 to initialize the registers to their POR values. The register assignments of the MAX8904 are in Table 2.

Table 2. Register Assignments

REGISTER ADDRESS	R/W	POR VALUE	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0
00h	R/W	00h	**GPIO-A CONFIG**	PWM enable/ disable	PWM bank select	GPIO1 configuration bits		PWM enable/ disable	PWM bank select	GPIO0 configuration bits	
01h	R/W	00h	**GPIO-B CONFIG**	PWM enable/ disable	PWM bank select	GPIO3 configuration bits		PWM enable/ disable	PWM bank select	GPIO2 configuration bits	
02h	R/W	00h	**GPIO-C CONFIG**	PWM enable/ disable	PWM bank select	GPIO5 configuration bits		PWM enable/ disable	PWM bank select	GPIO4 configuration bits	
03h	R/W	00h	**GPIO-D CONFIG**	PWM enable/ disable	PWM bank select	GPIO7 configuration bits		PWM enable/ disable	PWM bank select	GPIO6 configuration bits	
04h	R/W	00h	**GPIO-DATA**	I/O-8	I/O-7	I/O-6	I/O-5	I/O-4	I/O-2	I/O-1	I/O-0
05h	R/W	00h	**PWM-BANK0**	MSB	—	—	—	—	—	—	LSB
06h	R/W	00h	**PWM-BANK1**	MSB	—	—	—	—	—	—	LSB
07h	R/W	00h	**ENABLE**	CSAEN	X	CMPEN	BSTEN	ADJEN	5V0EN	INIT	CLSEN
08h	R/W	00h	**SHUTDOWN ($\overline{SHDN}$)**	CSA	X	CMP	BST	ADJ	5V0	X	CLS
09h	R/W	00h	**MODE**	CSAG	CSFLGEN	X	BSTIV	ADJM	X	X	OVOFF
0Ah	R/W	00h	**ADJSP**	Lockout	X	MSB	—	—	—	—	LSB
0Bh	R/W	00h	**BSTCSP**	X	X	MSB	—	—	—	—	LSB
0Ch	R/W	00h	**BSTVSP**	Lockout	X	MSB	—	—	—	—	LSB
0Dh	R	00h	**FAULTSTATUS**	BSTFLT1	BSTFLT0	VOKFLT	OLFLT	TMP120	X	OCIN	OVIN
0Eh	R	00h	**OVERLOAD**	BSTOL	ADJOL	5V0OL	3V3OL	1V8OL	1V2OL	X	CLSOL
0Fh	R	FFh	**VOK**	BSTOK	ADJOK	5V0OK	3V3OK	1V8OK	1V2OK	X	CLSOK
10h	R	—	**DEVICE ID**	Chip ID MSB	—	—	—	Chip ID LSB	Chip Rev MSB	—	Chip Rev LSB
11h	W	00h	**CLRFLTS**	Fault status and fault registers are cleared and $\overline{FLT}$ goes to high when CLRFLTS register is set to 01h. Fault detection rearms when CLRFLTS is set back to 00h.							

GPIO Configuration Register

The 00h to 03h registers allow the host processor to setup GPIO0–GPIO7 configuration through the I2C interface. Each nibble represents a physical GPIO port. These eight nibbles address all the operating requirements of the 8-bit GPIO port, including PWM dimming. LED blinking requirement is addressed by turning the LEDs on and off at the required rate through the I2C interface. The least significant two bits of each nibble define whether the particular GPIO bit is either an input or an output. If it is an output bit, the output device structure (open-drain/pullup, open-drain/high impedance, or high impedance/high impedance) is also defined by these two bits. On power-up, the eight GPIO bits are configured as inputs. See Table 3 for details.

GPIO Data Register

The GPIO Data register (04h) is a read/write (R/W) register that allows the host processor to read those GPIO bits that are programmed as inputs and write to those GPIO bits that are programmed as outputs through the I2C interface. For a read operation, all eight bits are read regardless of whether they are configured as inputs or outputs. It allows the host processor to read status of all eight bits. For a write operation, only those bits that are configured as outputs are written to, and the input bits are neglected. On power-up, all GPIO bits are configured to inputs by default. Each data bit represents a physical GPIO port and its functionality is given in Table 3.

PWM Bank Register

The PWM Bank registers PWM-BANK0 (05h) and PWM-BANK1 (06h) are used to set up two different pulse-width modulation values and switch between them by changing the value of the PWM bank select bit (D6/D2) in the GPIO Configuration registers (00h to 04h). Running at a clocking rate of 244Hz, these two registers allow the LEDs to be driven at 256 discrete levels of intensity control, from 0.0µs on/4.1ms off (0%) to 4.084ms on/16µs off (99.6%). When multiple LEDs are controlled by the GPIO ports, the use of two PWM registers allows some LEDs to be dimmed while other LEDs are simultaneously brightened. Individual LEDs can also be switched between two intensities by toggling its PWM-BANK assignment. See Table 5.

Table 3. GPIO Configuration Register (00h to 03h)

PWM ENABLE	PWM BANK	GPIO CONFIGURATION		GPIO CONFIGRUATION DESCRIPTION
D7/D3	D6/D2	D5/D1	D4/D0	DATA BITS
X	X	0	0	Input with 1MΩ pullup resistor to GPIO
		GPIO-Data (04h): 0 = low, 1 = high		
0 = Disabled 1 = Enabled	0 = BANK0 1 = BANK1	0	1	Open-drain n-device with 10kΩ pullup resistor to GPIO, and tolerant of sinking current from 5V power supply
		GPIO-Data (04h): 0 = sink, 1 = pullup		
0 = Disabled 1 = Enabled	0 = BANK0 1 = BANK1	1	0	Open-drain n-device with high-impedance state, and tolerant of sinking current from 5V power supply
		GPIO-Data (04h): 0 = pull, 1 = push		
X	X	1	1	High-impedance (Hi-Z) output
		GPIO-Data (04h): 0 = Hi-Z, 1 = Hi-Z		
0	0	0	0	Reset value = 0h

Table 4. GPIO Data Register (04h)

D7	D6	D5	D4	D3	D2	D1	D0	DATA BITS
IO8	IO7	IO6	IO5	IO4	IO3	IO2	IO1	Reset value = 00h

Table 5. GPIO PWM Bank Register (05h, 06h)

D7	D6	D5	D4	D3	D2	D1	D0	DATA BITS
MSB	—	—	—	—	—	—	LSB	PWM-BANK0
MSB	—	—	—	—	—	—	LSB	PWM-BANK1
0	0	0	0	0	0	0	0	Reset value = 00h

High-Efficiency Power-Management IC with I^2C Control for 2-Cell Li+ Battery Operated Devices

Enable Register

With the exception of the 1V2, 1V8, and 3V3 power converters, the Enable register (Table 6) allows the host processor to enable/disable the individual channel when needed. If a bit is programmed to 1, the corresponding power converter is enabled; otherwise, with a value of 0, the corresponding power converter remains disabled, even if valid data has been programmed in the associated set point register (0Ah, 0Bh, or 0Ch) for the ADJ or BST power converter. Conversely, if the ADJEN bit for ADJ or the BSTEN bit for BST is set to 1, with a set point register (0Ah, 0Bh, or 0Ch) value of 00h, the ADJ or BST power converter remains disabled. When the MAX8904 turns off a particular power converter under a fault condition, it sets the corresponding Enable register bit to 0.

Note that the 1V2, 1V8, 3V3, and 5V0 converters are turned on when PWREN is pulled high, but the 5V0 converter can be turned on/off by the Enable register bits once it is above its VOK thresholds. The 1V2, 1V8, and 3V3 converters can be turned off only by pulling PWREN low.

Firmware Initialization at Power-Up

The MAX8904 requires a mandatory firmware procedure to be executed by the host processor at power-up to initialize the part correctly. The following register writes should be executed before responding to an interrupt on the $\overline{FLT}$ pin of the MAX8904.

- 04(h) ➔ Register 07(h) (Sets the INIT bit to 0)
- 01(h) ➔ Register 11(h)
- 00(h) ➔ Register 11(h)

Note that the firmware should keep the INIT bit set to 0 under all operating conditions.

Firmware Initialization for CLS Operation

The MAX8904 requires a mandatory firmware procedure to be executed by the host processor after turning ON the CLS block to initialize the CLS block correctly. The following firmware steps should be executed after turning ON the CLS block before responding to an interrupt on the $\overline{FLT}$ pin of the MAX8904:

- Execute a 300ms (min) delay.
- After the 300ms delay, execute the following register writes:
  01(h) ➔ Register 11(h)
  00(h) ➔ Register 11(h)

Shutdown Register

The Shutdown register works in conjunction with $\overline{SHDN}$ to program which converters are turned off in the event of a power failure. $\overline{SHDN}$ is connected to the midpoint of a resistor-divider from LVRIN5V to GND, and is nominally at 3.3V (see Table 7).

Upon receiving a power-fail signal, the host processor asserts the active-low $\overline{SHDN}$, and only those power converters whose corresponding bits are programmed to 0 in the Shutdown register are turned off, and their associated Enable bits in the Enable register, if currently programmed to 1, are set to 0. The power converters whose bits in the Shutdown register are programmed to 1 remain enabled.

If a power failure occurs, where the external power source voltage falls below the 3.4V, the MAX8904 enters the UVLO state. It powers up with default settings when it subsequently comes out of UVLO. Note that the host processor can still hold $\overline{SHDN}$ low at this point and it does not cause any action on the MAX8904. The MAX8904 performs the shutdown operation only when it detects a high-to-low transition on $\overline{SHDN}$.

Note that the 1V2, 1V8, and 3V3 power controllers are always ON and can not be turned off through the Shutdown register.

Table 6. Enable Register (07h)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
CSAEN	X	CMPEN	BSTEN	ADJEN	5V0EN	INIT	CLSEN	00h

Table 7. Shutdown Register (08h)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
CSA	X	CMP	BST	ADJ	5V0	X	CLS	00h

Mode Register

The Mode register is used to configure the operating mode of various functional blocks. See Table 8.

CSAG (Bit 7): The MAX8904 provides a programmable gain current-sense amplifier. The CSAG bit is used to determine the gain setting for CSA. If it is programmed to 0, the amplifier gain is set to 20V/V. If it is programmed to 1, the amplifier gain is set to 40V/V.

CSFLGEN (Bit 6): The CSFLGEN bit is used to enable/disable the CSA input over-current fault detection feature. If the CSFLGEN bit is high, the MAX8904 sets the OCIN (D1) bit in the FAULT STATUS register, and asserts $\overline{FLT}$ when an input overcurrent is sensed at CSOUT. The input overcurrent fault detection is disabled if CSFLGEN is set to 0.

BSTIV (Bit 4): The BST step-up converter supports voltage mode or current mode operation and the mode selection is realized by the BSTIV bit. If it is programmed to 0, the converter operates in the current mode with the BSTCSP register setting. If it is programmed to 1, the converter operates in the voltage mode with the BSTVSP register setting.

ADJM (Bit 3): The MAX8904 supports automatic switching from pulse-width modulation (PWM) to pulse-skipping modulation (PSM) to improve power supply efficiency at light loads for all of the power converters except the ADJ step-down converter that must be set by the ADJM bit. Because the pulse-skipping mode has inherently larger voltage ripple, it may be necessary for the ADJ supply to remain in pulse-width modulation mode when powering noise sensitive loads such as a GPRS radio module. ADJM bit allows the host processor to force the ADJ controller to remain in PWM mode, if desired. When it is programmed to 0, the ADJ power converter automatically switches between PSM and PWM modes. When it is programmed to 1, the power controller is forced to remain in PWM mode.

OVOFF (Bit 0): The OVOFF bit is used to turn off the external overvoltage protection n-MOSFET, for the purpose of battery pack conditioning. When it is programmed to 0, the overvoltage protection circuit determines the state of the external overvoltage protection n-MOSFET. When it is programmed to 1, the overvoltage protection n-MOSFET is turned off.

ADJSP Register

The MAX8904 uses the I2C interface to set the output voltage of ADJ power controller. A 6-bit value adjusts the ADJ output voltage from 3V to 5.067V, in 33.3mV increments (see Table 10). It is an invalid setting if the ADJSP register is set as 00h (2.967V). The first valid setting is 01h (3V). See Table 9 for the ADJSP register definition.

Table 10 shows hex codes for various output voltage settings of the ADJ power controller.

Bit 7 (LOCKOUT) of the ADJSP register allows the voltage setting to be programmed only one time after power-up. After power-up, the host processor sets the ADJSP value only once. When the host processor changes the 00h setting to a valid number, the MAX8904 sets the LOCKOUT bit to 1. Once it is set to 1, subsequent changes to the 6-bit ADJSP value are locked out. Only by recycling power, the LOCKOUT bit can be restored to 0. Note that the ADJSP register is an R/W register, and it allows the user to read the lockout bit and determine whether the MAX8904 had already been set to a valid output voltage.

When the MAX8904 detects that the ADJEN bit is 1, and recognizes valid data in the ADJSP register, the ADJ controller is enabled and soft-starts to the target output voltage. When the Enable bit for the ADJ power converter is set to 1 with an ADJSP register value of 00h, the ADJ stays in the off condition. Conversely, with the ADJEN bit set to 0, the regulator remains disabled, even if valid data has been programmed in the ADJSP register. Neither of these two conditions generates a $\overline{FLT}$ assertion, since the power converter is considered to be in the off state. Fault detection is enabled only if the ADJEN bit is high, and valid data has been programmed in the ADJSP register. See Table 11.

Table 8. Mode Register (09h)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
CSAG	CSFLGEN	X	BSTIV	ADJM	X	X	OVOFF	00h

Table 9. ADJSP Register (0Ah)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
LOCKOUT	X	MSB	—	—	—	—	LSB	00h
0	0	0	0	0	0	0	0	00h

Table 10. ADJ Output Voltage Settings

ADJ VOLTAGE	HEX CODE	ADJ VOLTAGE	HEX CODE
3.000	1	4.066	21
3.033	2	4.099	22
3.066	3	4.133	23
3.099	4	4.166	24
3.133	5	4.199	25
3.166	6	4.233	26
3.199	7	4.266	27
3.233	8	4.299	28
3.266	9	4.333	29
3.299	A	4.366	2A
3.333	B	4.399	2B
3.366	C	4.433	2C
3.399	D	4.466	2D
3.433	E	4.499	2E
3.466	F	4.533	2F
3.499	10	4.566	30
3.533	11	4.599	31
3.566	12	4.633	32
3.599	13	4.666	33
3.633	14	4.699	34
3.666	15	4.733	35
3.699	16	4.766	36
3.733	17	4.799	37
3.766	18	4.833	38
3.799	19	4.866	39
3.833	1A	4.899	3A
3.866	1B	4.933	3B
3.899	1C	4.966	3C
3.933	1D	4.999	3D
3.966	1E	5.033	3E
3.999	1F	5.066	3F
4.033	20	—	—

Table 11. ADJEN/ADJSP Truth Table

ADJEN BIT	ADJSP VALID SET POINT	ADJ ENABLED	FAULT DETECTION ENABLED
0	00h	No	No
0	> 00h	No	No
1	00h	No	No
1	> 00h	Yes	Yes

Table 12. BSTCSP Register (0Bh)

D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE
Reserved	Reserved	MSB	—	—	—	—	LSB	00h
X	X	0	0	0	0	0	0	00h

BST Current Set Point Register

The BST step-up converter has two modes of operation: current and voltage. The current-mode operation is used to drive a WLED string, while the voltage-mode operation provides a regulated DC voltage for TFT or OLED panels.

In the current mode, the WLED string is connected from the BST output to PCS and the control loop regulates the LED current to the value set in the BSTCSP register through the I2C interface. The BSTCSP register (0Bh) is defined in Table 12. A 6-bit value allows the host processor to adjust the current from 1mA to 63mA, in 1mA minimum increments. The maximum recommended increment is 16mA per I2C command. It is an invalid setting if the BSTCSP register is set to 00h (0mA). The first valid number is 01h (1mA). The 3Fh setting corresponds to 63mA (see Table 13 for WLED current settings and corresponding hex codes).

The host processor can change the dimming levels as many times as desired during normal operation.

In current mode, the value programmed in the BSTVSP register (0Ch) is used as an overvoltage threshold. When the output voltage in current mode reaches the threshold, the converter is immediately latched off, and it requires either the host processor to issue either a CLRFLTS command and drive BSTEN high, or recycling input power to start up again. Recommended overvoltage threshold settings for the LED strings are provided in Table 14. The overvoltage threshold is programmable from 13.4V to 32V in 300mV increments. A 00h setting in the BSTVSP register corresponds to 13.1V and is an invalid setting. A 01h value corresponds to a valid 13.4V overvoltage setting. The host processor can only program this overvoltage setting in the BSTVSP register once, after which the lockout bit is set to 1 to prevent subsequent programming attempts. The one-time programmability of the BSTVSP register applies to overvoltage setting in both current mode and voltage mode.

Table 13. BSTCSP LED Current Settings

LED CURRENT (mA)	HEX CODE	LED CURRENT (mA)	HEX CODE
1	01	33	21
2	02	34	22
3	03	35	23
4	04	36	24
5	05	37	25
6	06	38	26
7	07	39	27
8	08	40	28
9	09	41	29
10	0A	42	2A
11	0B	43	2B
12	0C	44	2C
13	0D	45	2D
14	0E	46	2E
15	0F	47	2F
16	10	48	30
17	11	49	31
18	12	50	32
19	13	51	33
20	14	52	34
21	15	53	35
22	16	54	36
23	17	55	37
24	18	56	38
25	19	57	39
26	1A	58	3A
27	1B	59	3B
28	1C	60	3C
29	1D	61	3D
30	1E	62	3E
31	1F	63	3F
32	20	—	—

Table 14. Overvoltage Threshold Settings for BST Regulator Current-Mode Operation

NO. OF SERIES WLEDs	BSTVSP SETTING (V)	CODE IN BSTVSP REGISTER (0Ch)
4	18.3	04h
5	22.5	12h
6	26.7	20h
7	30.9	2Eh
8	35.1	3Ch

BST Voltage Set Point Register

When the BST operates in voltage mode, a device such as a TFT or OLED display panel can be connected between the BST output and power ground. PCS is connected to GND in this application to disable the current sink function. In this mode, the BST acts as a voltage source with current limit functionality and regulate its output to the value set in the BSTVSP register (see Table 15). A 6-bit value adjusts the voltage from 12.5V to 18.7V in 100mV increments (see Table 16). It is an invalid setting if the BSTVSP register is set to 00h (12.4V). The first valid number is 01h (12.5V). Note that with an output of 12.5V, the converter may be operating in dropout for an input voltage of 12.6V.

Table 15. BSTVSP Register (0Ch)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
Lockout	Reserved	MSB	—	—	—	—	LSB	—
0	X	0	0	0	0	0	0	00h

Table 16. BSTVSP Voltage Settings and Hex Codes

OUPUT VOLTAGE (V)	HEX CODE	OUTPUT VOLTAGE (V)	HEX CODE
12.5	01	15.7	21
12.6	02	15.8	22
12.7	03	15.9	23
12.8	04	16	24
12.9	05	16.1	25
13	06	16.2	26
13.1	07	16.3	27
13.2	08	16.4	28
13.3	09	16.5	29
13.4	0A	16.6	2A
13.5	0B	16.7	2B
13.6	0C	16.8	2C
13.7	0D	16.9	2D
13.8	0E	17	2E
13.9	0F	17.1	2F
14	10	17.2	30
14.1	11	17.3	31
14.2	12	17.4	32
14.3	13	17.5	33
14.4	14	17.6	34
14.5	15	17.7	35
14.6	16	17.8	36
14.7	17	17.9	37
14.8	18	18	38
14.9	19	18.1	39
15	1A	18.2	3A
15.1	1B	18.3	3B
15.2	1C	18.4	3C
15.3	1D	18.5	3D

Table 16. BSTVSP Voltage Settings and Hex Codes (Voltage Mode) (continued)

OUPUT VOLTAGE (V)	HEX CODE	OUTPUT VOLTAGE (V)	HEX CODE
15.4	1E	18.6	3E
15.5	1F	18.7	3F
15.6	20	—	—

Table 17. BSTEN/BST_SP Truth Table

BSTEN BIT	BST_SP VALID SET POINT	BST ENABLED	FAULT DETECTION ENABLED
0	00h	No	No
0	> 00h	No	No
1	00h	No	No
1	> 00h	Yes	Yes

Bit 7 (LOCKOUT) of the BSTVSP register allows the voltage setting to be programmed only one time after power-up. After power-up, the host processor sets the BSTVSP value only once. When the host processor changes the 00h setting to a valid number, the MAX8904 sets LOCKOUT bit to 1. Once it is set to 1, subsequent changes to the 6-bit BSTVSP value are locked out. Only by recycling power, the LOCKOUT bit can be restored to 0. Note that the BSTVSP register is an R/W register, and it allows the user to check the lockout bit.

In voltage mode, when the MAX8904 detects that the BSTEN bit is 1 and recognizes valid data in the BSTVSP register, the BST regulator is enabled and soft-starts to the target output voltage. When the BSTEN is set to 1 with a BSTVSP register value of 00h, the BST regulator stays in the off condition. Conversely, with the BSTEN bit set to 0, the regulator remains disabled, even if the valid data has been programmed in the BSTVSP register. Neither of these two conditions generates a $\overline{FLT}$ assertion, since the regulator is considered to be in the off state. Fault detection is enabled only if the BSTEN bit is high, and valid data has been programmed in the BSTVSP register. See Table 17.

Fault Handling

The MAX8904 has two fault registers (VOK and OVERLOAD) and a fault status register (FAULTSTATUS). See Tables 18, 20, and 21 for details about these register bits.

Table 18. Fault Status Register (0Dh)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
BSTFLT1	BSTFLT0	VOKFLT	OLFLT	TMP120	X	OCIN	OVIN	00h

Table 19. BST Fault Bit Description

BSTFLT1	BSTFLT0	FAULT DESCRIPTION
0	0	No fault.
0	1	Overvoltage (current mode only).
1	0	Open or reverse output diode, or open BSTFB connection (detected at startup before BSTLX switching).
1	1	PCS short to GND fault, or BST output short to PCS fault (current mode only, detected at startup before BSTLX switching).

Table 20. Overload Register (0Eh)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
BSTOL	VADJOL	5V0OL	3V3OL	1V8OL	1V2OL	X	CLSOL	00h

Table 21. VOK Register (0Fh)

D7	D6	D5	D4	D3	D2	D1	D0	RESET
BSTOK	VADJOK	5V0OK	3V3OK	1V8OK	1V2OK	X	CLSOK	11h

The MAX8904 handles faults as outlined in Tables 22 and 23.

The FAULTSTATUS register indicates the type of system fault that has occurred. The BSTFLT0, BSTFLT1 bits are set based on the type of fault that has occurred in the BST step-up converter (see Table 19). The VOKFLT bit is set when a VOK fault has occurred on any one of the power converters.

A VOK fault occurs either when a converter fails to soft-start or due to overload/short-circuit conditions on the output under normal operation, causing the output voltage to fall below its VOK threshold. The _OK bits in the VOK register are set to 1 at power up. When a VOK fault occurs, the _OK bit corresponding to the faulty converter is set to 0, indicating a VOK fault in the particular converter.

The OLFLT bit is set when the output current on a converter exceeds its overload threshold. The _OL bit in the OVERLOAD register corresponding to the faulty converter is set to 1 indicating an overload fault in the particular converter.

The TMP120 bit is set when the internal die temperature exceeds +120°C. With the current sense resistor across CS+, CS- pins of the MAX8904 connected in series with the input power source, the OCIN bit is set when the CSOUT voltage exceeds its CSFLAG threshold, indicating an input overcurrent condition. The OVIN bit is set when the input voltage sensed at the OVPWR pin exceeds the overvoltage threshold.

Table 22. Fault Handling

FAULT TYPE	FAULT RESPONSE AND RECOVERY
• Overload on 1V2, 1V8, 3V3 • VOK fault on 1V2, 1V8, 3V3 (detected after internal soft-start time plus a 2ms delay).	• $\overline{\text{FLT}}$ goes to low, all regulators are turned off immediately after fault detection, and the corresponding bits in FAULTSTATUS, OVERLOAD, and VOK registers are set. • Fault detection is enabled for a regulator only if CLRFLTS=00h, and PWREN is high. • Toggling PWREN (high→low→high) if PWREN is still high, or driving PWREN from low to high resets all fault status and fault registers, pulls $\overline{\text{FLT}}$ to high, and causes the MAX8904 to restart the 1V2, 1V8, 3V3, and 5V0 supplies. • Recycling power to the LVRPWR input of the internal linear regulator causes the MAX8904 to power up and remain in standby mode if PWREN is low. If PWREN is high, the MAX8904 attempts to start the 1V2, 1V8, 3V3, and 5V0 supplies.
• V_{CLSIN}-V_{CLSOUT} > 1V, VOK fault on the current limited switch at the end of 250ms soft-start time • Overvoltage, open LED fault on LED step-up converter (current mode only) • LED cathode (PCS) short to ground detected before BSTLX switching (current mode only) • LED cathode (PCS) short to LED boost output, detected before BSTLX switching (current mode only) • Missing or reversed output diode, open BSTFB connection, detected before BSTLX switching.	• $\overline{\text{FLT}}$ goes to low and the regulator turns off immediately after fault detection. The corresponding bits in FAULTSTATUS, OVERLOAD, and VOK registers are set. • Setting CLRFLTS to 01h followed by CLRFLTS to 00h at any time clears all fault registers bits, pulls $\overline{\text{FLT}}$ to high, and rearms the MAX8904 for subsequent fault detection. • Fault detection is enabled for a regulator only if CLRFLTS=00h, and _EN=1 (The ADJ and BST step-up regulators also require valid data to be programmed in the ADJSP and BSTCSP/BSTVSP registers). • The regulator restarts, fault registers are cleared, $\overline{\text{FLT}}$ goes to high, if the _EN bit is toggled from 0 to 1. • Toggling PWREN (high→low→high) if PWREN is still high, or driving PWREN from low to high resets all fault status and fault registers, pulls $\overline{\text{FLT}}$ to high, and causes the MAX8904 to restart the 1V2, 1V8, 3V3, and 5V0 supplies. • Recycling power to the LVRPWR input of the internal linear regulator causes the MAX8904 to power up and remain in standby mode if PWREN is low. If PWREN is high, the MAX8904 attempts to start the 1V2, 1V8, 3V3, and 5V0 supplies.

Table 22. Fault Handling (continued)

FAULT TYPE	FAULT RESPONSE AND RECOVERY
• BSTFB or LED anode shorted to ground (an external 40V-rated Schottky diode must be connected from power ground to BSTFB, as close as possible to the BSTFB capacitor)	• $\overline{FLT}$ goes to low and BSTLX switching stop immediately after fault detection. The corresponding bits in FAULTSTATUS, OVERLOAD registers are set. The BST regulator turns off 250ms after the fault. • Setting CLRFLTS to 01h followed by CLRFLTS to 00h at any time clears all fault registers bits, pulls $\overline{FLT}$ to high, and rearms the MAX8904 for subsequent fault detection. • Fault detection is enabled for a regulator only if CLRFLTS = 00h, and BSTEN = 1. Valid data must be programmed in the BSTCSP/BSTVSP registers). • The regulator restarts, fault registers are cleared, $\overline{FLT}$ goes to high, if the BSTEN bit is toggled from 0 to 1. • Toggling PWREN (high→low→high) if PWREN is still high, or driving PWREN from low to high resets all fault status and fault registers, pulls $\overline{FLT}$ to high, and causes the MAX8904 to restart the 1V2, 1V8, 3V3, and 5V0 supplies. • Recycling power to the LVRPWR input of the internal linear regulator causes the MAX8904 to power up and remain in standby mode if PWREN is low. If PWREN is high, the MAX8904 attempts to start the 1V2, 1V8, 3V3, and 5V0 supplies.
• Overload on 5V0, ADJ, BST. V_{CLSIN}-V_{CLSOUT} > 1V, VOK fault on the current limiter in normal operation. • Output voltage < VOK falling threshold on 5V0, ADJ, BST (voltage mode only), (detected after soft-start time plus 2ms delay for 5V0, ADJ, and 1.024ms for BST.	• $\overline{FLT}$ goes to low immediately after fault detection, and fault status and fault registers are set. • For $t_{\overline{FLT}} \geq 250ms$, the _EN bit is set to 0, and the regulator turns off. • Setting CLRFLTS to 01h followed by CLRFLTS to 00h at any time clears all fault status and fault register bits, pulls $\overline{FLT}$ to high, and rearms the MAX8904 for subsequent fault detection. • $\overline{FLT}$ goes to low, fault status and fault register information of a $t_{\overline{FLT}} < 250ms$ momentary fault event is latched until the command of setting CLRFLTS to 01h is issued. • Momentary $t_{\overline{FLT}} < 250ms$ faults do not cause the regulator to turn off. • Fault detection is enabled for a regulator only if CLRFLTS = 00h, and _EN = 1. The ADJ and LED boost regulators also require valid data to be programmed in the ADJSP and BSTCSP or BSTVSP registers. • Regulator restarts and fault register and fault status register are cleared, $\overline{FLT}$ goes to high, if the _EN bit is toggled (0 to 1). • Toggling PWREN (high→low→high) if PWREN is still high, or driving PWREN from low to high resets all fault status and fault registers, pulls $\overline{FLT}$ to high, and causes the MAX8904 to restart the 1V2, 1V8, 3V3, and 5V0 supplies. • Recycling power to the LVRPWR input of the internal linear regulator causes the MAX8904 to power up and remain in standby mode if PWREN is low. If PWREN is high, the MAX8904 attempts to start the 1V2, 1V8, 3V3, and 5V0 supplies.
• Input overvoltage at OVPWR	• If an overvoltage event occurs in normal operation, the MAX8904 turns off the external n-MOSFET through OVGATE immediately. • $\overline{FLT}$ goes to low and OVIN goes to 1 in fault status register immediately after fault detection. • If the input voltage falls below the voltage of $V_{OV} - V_{HYS\_OV}$, the OVP n-MOSFET turns back on. However, $\overline{FLT}$ stays low and OVIN stays high until the MAX8904 receives the command setting CLRFLTS to 01h. • Setting CLRFLTS to 01h followed by CLRFLTS to 00h at any time clears all fault status and fault register bits, pulls $\overline{FLT}$ to high, and rearms the MAX8904 for subsequent fault detection. • If overvoltage persists, the OV n-MOSFET remains off, and the MAX8904 regulator input supply decays to 2.85V, and the MAX8904 turns off at this point. • If an overvoltage condition occurs at startup, the external OVP n-MOSFET does not turn on and the MAX8904 does not startup. Therefore no fault information is stored.

High-Efficiency Power-Management IC with I²C Control for 2-Cell Li+ Battery Operated Devices

Table 22. Fault Handling (continued)

FAULT TYPE	FAULT RESPONSE AND RECOVERY
• 120°C Overtemperature Flag	• The MAX8904 sets the TMP120 bit in fault status register and pulls FLT low if the internal temperature reaches +120°C (typ). All converters latch off when the temperature reaches +150°C (typ), and the MAX8904 goes into standby mode. In this mode, the internal linear regulator is turned off and the I²C interface is no longer powered. Note that PWREN may still be held high in this mode. • Toggling PWREN (high→low→high) or recycling MAX8904 power at LVRPWR allows the MAX8904 to come out of thermal shutdown.
• Input Overcurrent	• If CSFLGEN is high, then the OCIN bit in the fault status register is set to 1 in the fault status register, and FLT goes high. If CSFLGEN is low, no action is taken. • Setting CLRFLTS to 01h followed by CLRFLTS to 00h at any time clears all fault status and fault register bits, pulls FLT to high, and rearms the MAX8904 for subsequent fault detection.

Table 23. Summary of MAX8904 Fault Status Register and Fault Register Actions

FAULT TYPE	ACTIONS
Overload or short circuit on 1V2, 1V8, 3V3, 5V0, ADJ, and BST	OLFLT is set to 1 in the FAULTSTATUS register, and corresponding _OL is set to 1 in the OVERLOAD register.
VOK fault on 1V2, 1V8, 3V3, 5V0, ADJ, BST (voltage mode only), and current limiter	VOKFLT is set to 1 in the FAULTSTATUS register, and corresponding _OK is set to 0 in the VOK register.
Overvoltage on BST, open or reversed output diode, open BSTFB connection, PCS shorted to ground, PCS shorted to BST output	**FAULTSTATUS register:** BSTFLT1 and BSTFLT0 are set to 00 if none of the listed faults has occurred. BSTFLT1 and BSTFLT0 are set to 01 for overvoltage on BST step-up converter (current mode only). BSTFLT1 and BSTFLT0 are set to 10 for open or reversed output diode, or open BSTFB connection (detected at startup before BSTLX switching). BSTFLT1 and BSTFLT0 are set to 11 for PCS shorted to ground or PCS shorted to BST output (current mode only, detected at startup before BSTLX switching).
Input overvoltage fault	OVIN is set to 1 in the FAULTSTATUS register.
Input overcurrent fault	OCIN is set to 1 in the FAULTSTATUS register for CSFLGEN = 1.
+120°C overtemperature flag	TMP120 is set to 1 in the FAULTSTATUS register.

Table 24. Device Identification Register (10h)

D7	D6	D5	D4	D3	D2	D1	D0	—
Chip ID MSB	—	—	—	Chip ID LSB	Chip Rev MSB	—	Chip Rev LSB	Read only

Device Identification Register

Device identification register (10h) identifies the chip ID and revision, and is shown in Table 24. It is a read-only register.

CLRFLTS Register

The MAX8904 clears all fault registers when the CLRFLTS register (11h) is set to 01h, to allow the processor to reset the fault and restart the system. When a fault occurs, the host processor is interrupted and enters its interrupt service routine (ISR). It masks the interrupt, services the fault by reading the MAX8904 registers, and may clear the fault(s) to recheck for fault(s) or immediately act upon the faults, and unmasks the interrupt. If the fault is still present, the FLT signal goes low and the host processor enters its ISR again. CLRFLTS must be set to 00h to rearm fault detection.

Overvoltage and Reverse Polarity Protection

The MAX8904 has an overvoltage protection block as shown in Figure 8. This block has its own UVLO thresholds, linear regulator, and reference. It essentially operates as a stand-alone overvoltage protection block. Applying an external voltage greater than 4V (typ) to OVPWR causes the overvoltage protection block to commence operation. At this time, the external n-MOSFET has not yet been turned on. After a 30ms delay, if the OVPWR voltage is less than 13.65V (typ), the overvoltage charge pump gate drive is powered up and OVGATE turns on the external n-MOSFET. Otherwise, if the OVPWR voltage is greater than 13.65V, OVGATE holds the n-MOSFET off.

After the OVP n-MOSFET (Q1) powers up, the system voltage V_{INT} comes up and powers the internal LVR linear regulator and all power inputs (_IN). When V_{IN} exceeds the UVLO (rising), the MAX8904 waits for a logic-high signal on PWREN to start up the 1V2, 1V8, 3V3 and 5V0 supplies, provided V_{IN} is greater than 5.6V (typ).

Reverse polarity protection down to -28V is provided by use of an external p-MOSFET (Q2) to protect downstream circuitry. When the input voltage goes negative, RPGATE goes high to turn off the external p-MOSFET. When the input voltage rises in the positive direction to a maximum of +30V, RPGATE pulls low and turns on the p-MOSFET. When an overvoltage event of up to +30V occurs, an internal clamp protects the gate of the p-MOSFET from excessive voltage such that the $V_{GATE\text{-}SOURCE}$ voltage of the external p-MOSFET (Q2) does not exceed 16V (typ).

Current Limited Switch

The current limited switch (CLS) allows the MAX8904 to control the amount of current that an external device draws from the supply voltage. The CLS is connected between the input supply voltage and the target peripheral device. It provides a peripheral current of at least 425mA, and is protected under short-circuit conditions. A short-circuit condition that lasts greater than 250ms latches the CLS off. The CLS can be enabled and disabled through the Enable register and can be selected for immediate power-fail shutdown in the Shutdown register.

An internal thermal loop protects the CLS from an overload or short-circuit fault that causes excessive power dissipation across the switch. It reduces the current delivered by the CLS if the die temperature rises above a preset temperature threshold (+120°C) and thus limits the power dissipation in the CLS. The thermal loop is enabled only when $V_{CLSIN} - V_{CLSOUT} > 1V$.

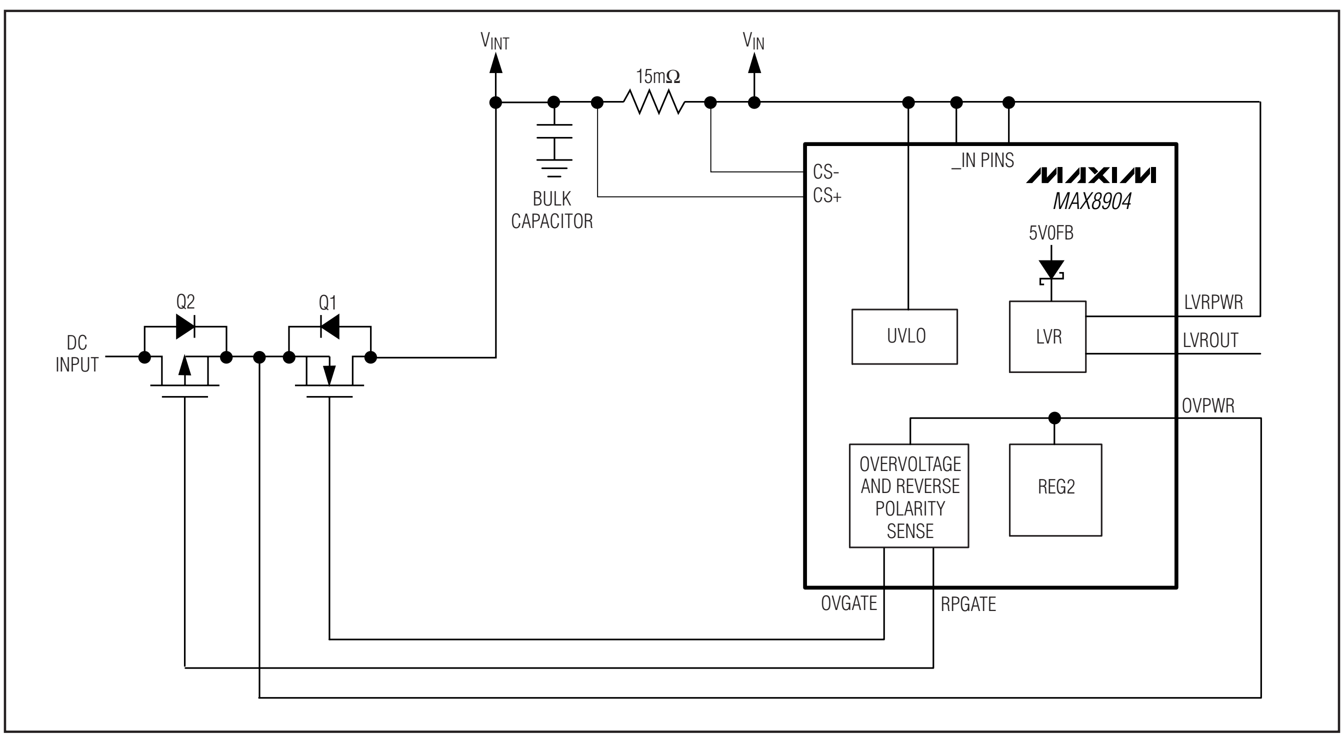


Figure 8. Overvoltage and Reverse Polarity Protection

With bit CLSEN in Enable register set to 1, the 250ms timer is activated. During normal operation, if V_{CLSIN} - V_{CLSOUT} > 1V, $\overline{FLT}$ is set, CLSOK bit is set to 0, the VOKFLT bit is set to 1, and the 250ms timer is started. If V_{CLSIN} - V_{CLSOUT} < 1V before the timer expires, the timer is reset and the IC resumes normal operation. The fault information is preserved and the status of $\overline{FLT}$, CLSOK, and VOKFLT remain unchanged until the I²C receives a CLRFLTS command. If V_{CLSIN} - V_{CLSOUT} > 1V after 250ms, the CLS is turned off, $\overline{FLT}$ is asserted, the CLSOK bit is set to 0, the VOKFLT bit is set to 1, and the CLSEN is set to 0. The MAX8904 needs a CLRFLTS command to clear the fault information in the FAULTSTATUS and VOK registers and pull $\overline{FLT}$ high.

Current-Sense Amplifier

The current-sense amplifier measures the differential voltage across a current-sense resistor and generates an analog voltage proportional to the current-sense resistor differential voltage. This voltage is clamped internally to a maximum of 1.25V. The CSA has two programmable-gain settings, 20V/V and 40V/V. When used with a 15mΩ current-sense resistor, it allows full-scale (1.2V) output for 4A and 2A currents, respectively. The CSA sets the CSAOL bit in the Overload register if the maximum current is exceeded. The CSA can be enabled and disabled through the Enable register and can be selected for immediate power-fail shutdown in the Shutdown register.

Open-Drain Comparator

The open-drain comparator (CMP) is an uncommitted, 14V open-drain output comparator with 20mA of sinking capability. The CMP can be used for various functions such as independent print-head temperature monitoring, voltage comparison, driving a Piezo Buzzer, or a 20mA load sinking. The CMP can be enabled and disabled through the Enable register and can be selected for immediate power-fail shutdown in the Shutdown register.

$\overline{FLT}$ Interrupt

The $\overline{FLT}$ interrupt is an active-low output that indicates any fault condition. The fault condition can be either internal (overtemperature) or external (overloaded output). For certain types of faults such as an overload fault, when $\overline{FLT}$ is driven low, an internal 250ms timer is started. When the timer expires the MAX8904 disables the affected power converter. During the 250ms, from the time of the interrupt until the time the converter is disabled, the host processor can respond to the interrupt and take an action such as shutting down the power converter or some other appropriate action, such as, reducing the load current. For other emergency faults such as an overvoltage fault, there is no 250ms timer related operation, $\overline{FLT}$ is asserted and the converter is immediately turned off.

ADJ Step-Down Converter

The ADJ power converter is an adjustable voltage step-down converter that can be adjusted over a 6-bit range from 3.0V to 5.067V, in 33.3mV increments. The ADJ power converter is intended to be used for powering various radio modules, such as Wi-Fi, GPRS, and CDMA.

The ADJ supply is designed to support a 2A peak and 1.414A RMS output current load. An L-C filter may be connected to the output capacitor to attenuate the switching frequency ripple component to within radio module specification.

Power-Up/Down Sequencing for 1V2, 1V8, 3V3, and 5V0 Supplies

The PWREN signal initiates power-up of the default voltage rails on the MAX8904 if LVRPWR (the input of internal linear regulator) exceeds 5.6V (typ). The default power-up rails are 1V2, 1V8, 3V3, and 5V0. If the 1V2 rail is not used, pulling 1V2FB to LVRIN5 configures the MAX8904 to operate without its 1V2 rail, with the corresponding power sequencing option. Power-down sequencing operates in the reverse sequence of power-up after PWREN goes low.

Figures 9 and 10 show the two power-up/down sequencing cases. Table 25 shows the sequencing truth table. The ADJ and BST supplies can be turned on by the host processor any time after the 3V3 supply reaches its regulation, but all rails and MAX8904 blocks are shut down when PWREN pulls low. Note that there is a fixed time delay (D5, 3.6ms, typ) between the 1V8 supply reaching its VOK threshold and the 3V3 supply start time.

Table 25. Sequencing Truth Table

STATE OF 1V2FB DURING D2	SEQUENCING MODE
0	1V2, 1V8, and 3V3 sequenced, followed by 5V0
1	1V8 and 3V3 sequenced, followed by 5V0

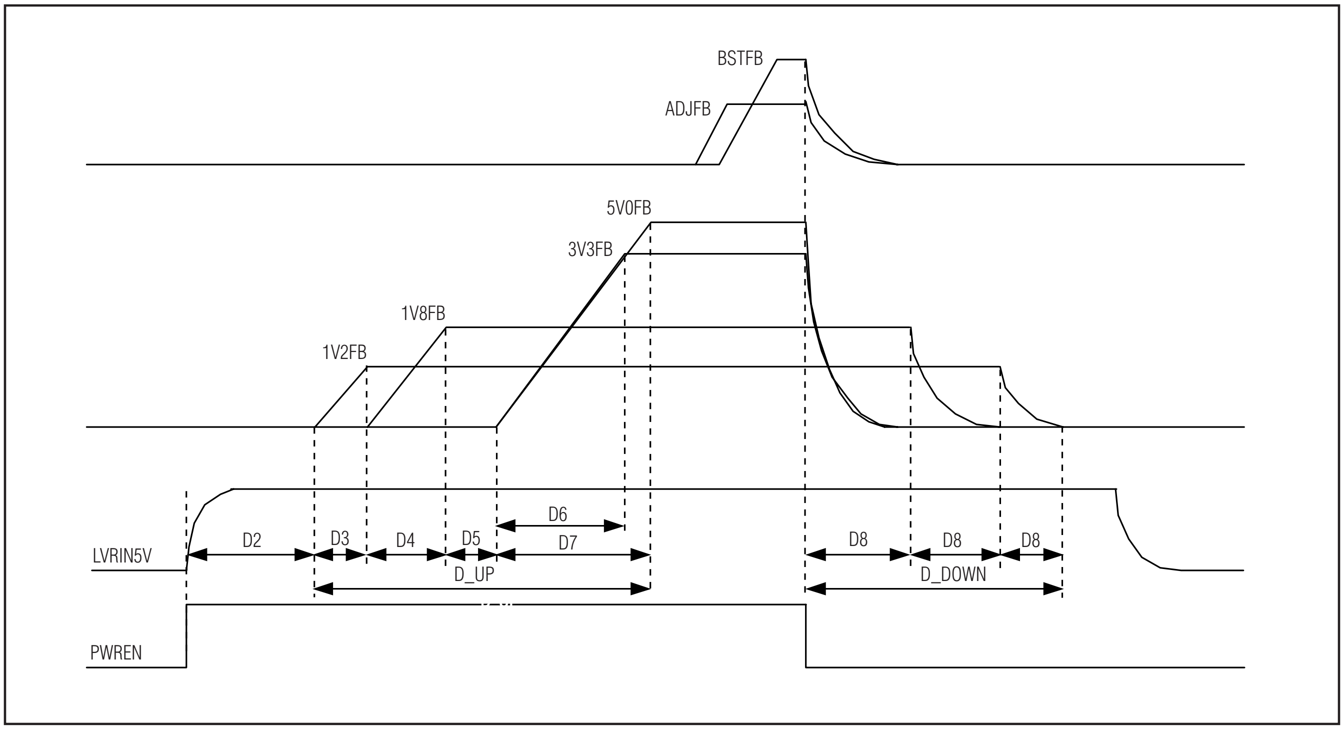


Figure 9. Power-Up/Down Sequencing with 1V2 Rail Used (See Table 26 for Timing Details)

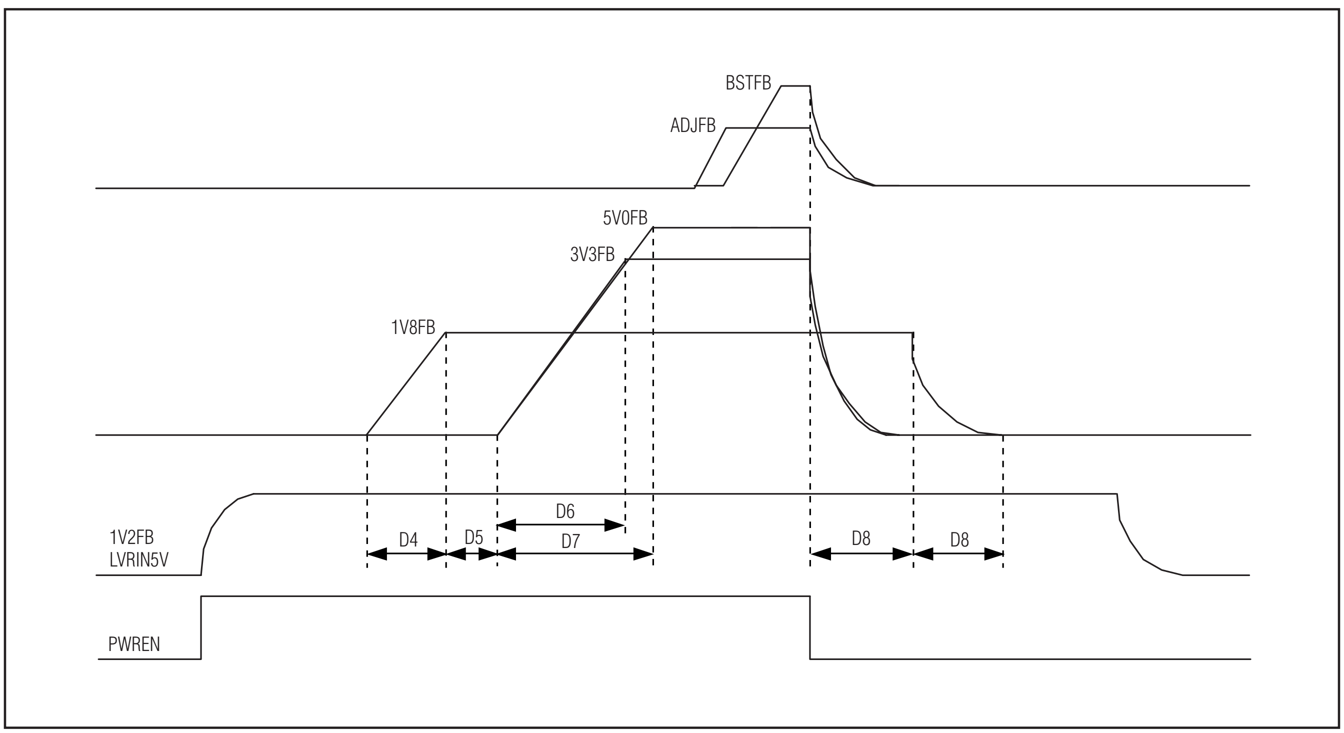


Figure 10. Power-Up/Down Sequencing Without 1V2 Rail Used (See Table 26 for Timing Details)

Table 26. Delay Time

DELAY	TIME (ms)
D2 (response time)	< 1
D3 (1V/ms ramp rate)	1.2
D4 (1V/ms ramp rate)	1.8
D5 (fixed delay)	3.6
D6 (1V/ms ramp rate)	3.4
D7 (1V/ms ramp rate)	5
D8 (estimated voltage decay time)	15
D_UP (maximum power-up sequence)	11.6 for all supplies, 10ms for 1V2, 1V8, and 3V3
D_DOWN (estimated voltage decay time)	45

Applications Information

Inductors for Step-Down and BST Converters

The MAX8904 power converters are optimized to work with specific values of inductors. Either 4.7µH or 4.3µH inductors should be used for the 1V2, 1V8, 3V3, and ADJ step-down converters. A 10µH inductor should be used for the 5V0 step-down converter. Ensure that the inductor saturation current rating exceeds the peak inductor current, and the rated maximum DC inductor current exceeds the maximum output current. For most applications, use an inductor with a DC current rating 1.25 times the maximum required output current. For maximum efficiency, the inductor DC resistance should be as low as possible. A 10µH inductor is recommended for the BST step-up converter. See Table 27 for recommended inductor specifications.

Input and Output Capacitors

The input capacitor in a DC-DC converter reduces current peaks drawn from the input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than the input source's output impedance so that high-frequency switching currents do not pass through the input source. The DC-DC converter output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are highly recommended for both input and output capacitors due to their small size, low ESR, and small temperature coefficients. It should be noted that the effective capacitance that can be obtained in ceramic capacitors should be derated based on their operating DC bias (maximum converter input voltage in the case of input capacitors and maximum converter output voltage in the case of output capacitors). See Table 27 for recommended capacitor specifications based on the considerations outlined above.

CLS Output Capacitor

To prevent the MAX8904 from sensing a startup fault condition, the maximum capacitance that should be connected to the CLSOUT pin is given by the following equation:

$$C_{CLSOUT(MAX)} \leq (425 - I_{LOAD}) \times 225/V_{CLSIN(MAX)}$$

where I_{LOAD} is the load current on CLSOUT in mA, $V_{CLSIN(MAX)}$ is the maximum input voltage at CLSIN in volts, and C_{CLSOUT} is in µF.

Bootstrap Capacitors

Connect a 0.1µF low-ESR ceramic capacitor between the _LX and _BST for all the step-down converters. The bootstrap capacitor provides the gate-drive voltage for the internal high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

Table 27. Recommended Component Specifications (See Figure 1)

COMPONENT	PART NUMBER	PART DESCRIPTION
L1	TOKO, DE3518 Series, 1127AS-100M	Inductor, SMT 10µH, 20%, 145mΩ DCR, 1.2A
L2, L4	TOKO, DE3518 Series, 1127AS-4R7M	Inductors, SMT 4.7µH, 20%, 60mΩ DCR, 1.75A
L3, L5	TOKO, DE4518 Series, 1124BS-4R3M	Inductors, SMT 4.3µH, 20%, 70mΩ DCR, 2.65A
L6	TOKO, DE4518 Series, 1124BS-100M	Inductor, SMT 10µH, 20%, 120mΩ DCR, 1.75A
C1	Murata, GRM188R71C224KA01D	Ceramic capacitor, 0.22µF, 10%, 16V, X7R, 0603
C2, C3, C10	Murata, GRM188R70J105KA01D	Ceramic capacitors, 1.0µF, 10%, 6.3V, X7R, 0603
C4	Taiyo Yuden, EMK212BJ105KG-T	Ceramic capacitor, 1.0µF, 10%, 16V, X7R, 0805
C5	Taiyo Yuden, EMK212BJ225KG-T	Ceramic capacitor, 2.2µF 10%, 16V, X7R, 0805
C6 (current mode)	Taiyo Yuden, UMK316B7105KL-T	Ceramic capacitor, 1.0µF, 10%, 50V, X7R, 1206
C6 (voltage mode)	Murata GRM32DR61E106KA12L	Ceramic capacitor, 10µF, 10%, 25V, X5R, 1210
C7, C15, C18, C21, C24	Taiyo Yuden, TMK212BJ475KG	Ceramic capacitors, 4.7µF, 10%, 25V, X7R, 0805
C8	Taiyo Yuden, AMK107BJ226MA	Ceramic capacitor, 2 x 22µF, 20%, 4V, X5R, 0603
C9, C12, C13, C16, C19, C22	Taiyo Yuden, EMK105B7104KV	Ceramic capacitors, 0.1µF, 10%, 16V, X7R, 0402
C11	Sanyo, 16CE680AX	Electrolytic capacitor, SMT 680µF, 20%, 16V
C14	Taiyo Yuden, JMK316BJ226KL	Ceramic capacitor, 2 x 22µF 10%, 6.3V, X5R, 1206
C17	Taiyo Yuden, JMK212BJ226KG	Ceramic capacitor, 22µF, 10%, 6.3V, X5R, 0805
C20	Taiyo Yuden, JMK316BJ226KL	Ceramic capacitor, 2 x 22µF, 10%, 6.3V, X5R, 1206
C23	Taiyo Yuden, JMK316BJ226KL	Ceramic capacitor, 22µF, 10%, 6.3V, X5R, 1206
C25	Taiyo Yuden, TMK105B7223KV	Ceramic capacitor, 0.022µF, 10%, 25V, X7R, 0402
D1	ON Semiconductor, MBR0540T1G	Schottky diode, 40V, 0.5A, SOD123
D2 (the MAX8904 is protected for short-circuit fault at startup, D2 required only for short-circuit protection in normal operation)	ON Semiconductor, MBR0540T1G	Schottky diode, 40V, 0.5A, SOD123
Q1, Q2	Fairchild Semiconductor, FDS8962C	Dual n-/p-MOSFETs, 30V, 8-pin SO
R1	Yageo, RC0402FR-0710RL	Resistor, SMT 10.0Ω, 1/16W, 1%, 0402
R2	Vishay, WSL1206R0150FEA	Resistor, 0.015Ω, 1/4W, 1%, 1206 SMD
R3 (the MAX8904 is protected for PCS to BSTFB short fault at startup, R3 required only for short PCS to BSTFB short-circuit protection in normal operation)	Yageo, RC0402FR-0710RL	Resistor, SMT 10.0Ω, 1/16W, 1%, 0402

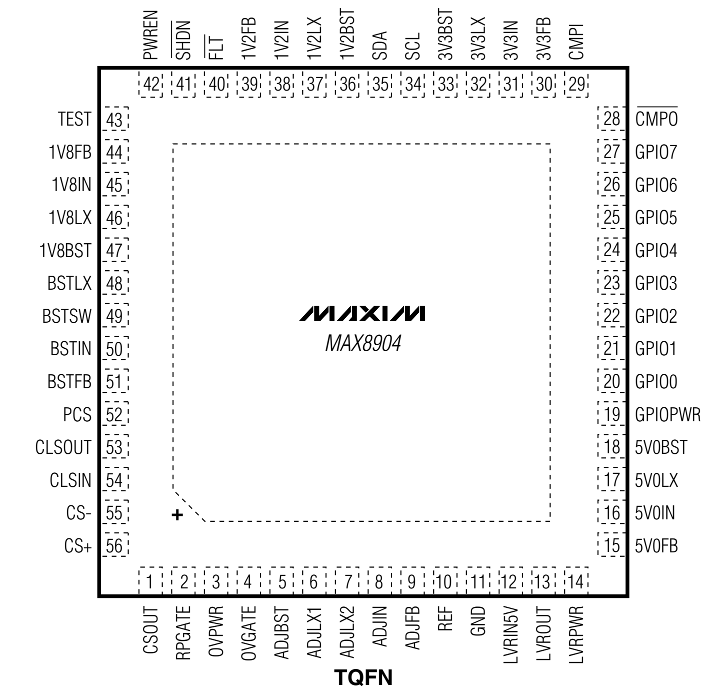
PCB Layout and Routing

High switching frequencies and relatively large peak currents make the PCB layout a very important aspect of power converter design. Good design minimizes ground bounce, excessive EMI on the feedback paths, and voltage gradients in the ground plane, which can result in instability or regulation errors.

A separate low-noise analog ground plane containing the reference, linear regulator, signal ground, and GND must connect to the power-ground plane at only one point to minimize the effects of power-ground currents. Connect GND to the exposed pad directly under the IC. Use multiple tightly spaced vias to the ground plane under the exposed pad to help cool the IC. Position the input capacitors from _IN to the power ground plane as close as possible to the IC. Connect the inductors and output capacitors as close as possible to the IC and keep the traces short, direct, and wide. Refer to the MAX8904 evaluation kit for the recommended PCB layout.

High-Efficiency Power-Management IC with I²C Control for 2-Cell Li+ Battery Operated Devices

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN-EP	T5677+2	21-0144

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