

**GigaMOS™ Trench™**  
**HiperFET™**  
**Power MOSFET**

**MMIX1F230N20T**

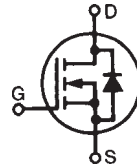
$$V_{DSS} = 200V$$

$$I_{D25} = 156A$$

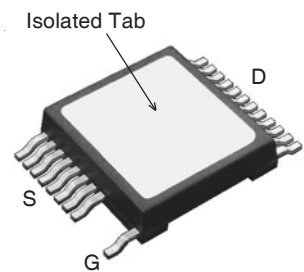
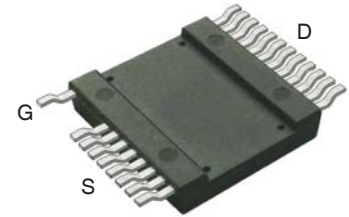
$$R_{DS(on)} \leq 8.3m\Omega$$

$$t_{rr} \leq 200ns$$

(Electrically Isolated Tab)



N-Channel Enhancement Mode  
 Avalanche Rated  
 Fast Intrinsic Diode



G = Gate      D = Drain  
 S = Source

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ C$ to $175^\circ C$	200	V
$V_{DGR}$	$T_J = 25^\circ C$ to $175^\circ C$ , $R_{GS} = 1M\Omega$	200	V
$V_{GSS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ C$	156	A
$I_{DM}$	$T_C = 25^\circ C$ , Pulse Width Limited by $T_{JM}$	630	A
$I_A$	$T_C = 25^\circ C$	100	A
$E_{AS}$	$T_C = 25^\circ C$	5	J
$P_D$	$T_C = 25^\circ C$	600	W
$dv/dt$	$I_S \leq I_{DM}$ , $V_{DD} \leq V_{DSS}$ , $T_J \leq 175^\circ C$	20	V/ns
$T_J$		-55 ... +175	$^\circ C$
$T_{JM}$		175	$^\circ C$
$T_{stg}$		-55 ... +175	$^\circ C$
$T_L$	1.6mm (0.062 in.) from Case for 10s	300	$^\circ C$
$T_{SOLD}$	Plastic Body for 10s	260	$^\circ C$
$V_{ISOL}$	50/60 Hz, 1 Minute	2500	V~
$F_C$	Mounting Force	50..200 / 11..45	N/lb.
<b>Weight</b>		8	g

Symbol	Test Conditions ( $T_J = 25^\circ C$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V$ , $I_D = 3mA$	200		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 8mA$	3.0		5.0 V
$I_{GSS}$	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			$\pm 200$ nA
$I_{DSS}$	$V_{DS} = V_{DSS}$ , $V_{GS} = 0V$ Note 2, $T_J = 150^\circ C$			50 $\mu A$ 3 mA
$R_{DS(on)}$	$V_{GS} = 10V$ , $I_D = 60A$ , Note 1			8.3 m $\Omega$

**Features**

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Substrate
  - Excellent Thermal Transfer
  - Increased Temperature and Power Cycling Capability
  - High Isolation Voltage (2500V~)
- 175 $^\circ C$  Operating Temperature
- Very High Current Handling Capability
- Fast Intrinsic Diode
- Avalanche Rated
- Very Low  $R_{DS(on)}$

**Advantages**

- Easy to Mount
- Space Savings
- High Power Density

**Applications**

- DC-DC Converters and Off-Line UPS
- Primary-Side Switch
- High Speed Power Switching Applications

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 10\text{V}, I_D = 60\text{A}$ , Note 1	90	150	S
$C_{iss}$	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		24	nF
$C_{oss}$			2440	pF
$C_{rss}$			60	pF
$R_{Gi}$	Gate Input Resistance		1.15	$\Omega$
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		58	ns
$t_r$			38	ns
$t_{d(off)}$			62	ns
$t_f$			17	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		358	nC
$Q_{gs}$			138	nC
$Q_{gd}$			60	nC
$R_{thJC}$				0.25 $^\circ\text{C/W}$
$R_{thCS}$		0.15		$^\circ\text{C/W}$
$R_{thJA}$		30		$^\circ\text{C/W}$

**Source-Drain Diode**

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$I_S$	$V_{GS} = 0\text{V}$			230 A
$I_{SM}$	Repetitive, Pulse Width Limited by $T_{JM}$			920 A
$V_{SD}$	$I_F = 60\text{A}, V_{GS} = 0\text{V}$ , Note 1			1.3 V
$t_{rr}$	$I_F = 115\text{A}, V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 75\text{V}$			200 ns
$Q_{RM}$			0.74	$\mu\text{C}$
$I_{RM}$			10.6	A

**Notes:**

1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .
2. Part must be heatsunk for high-temp Ices measurement.

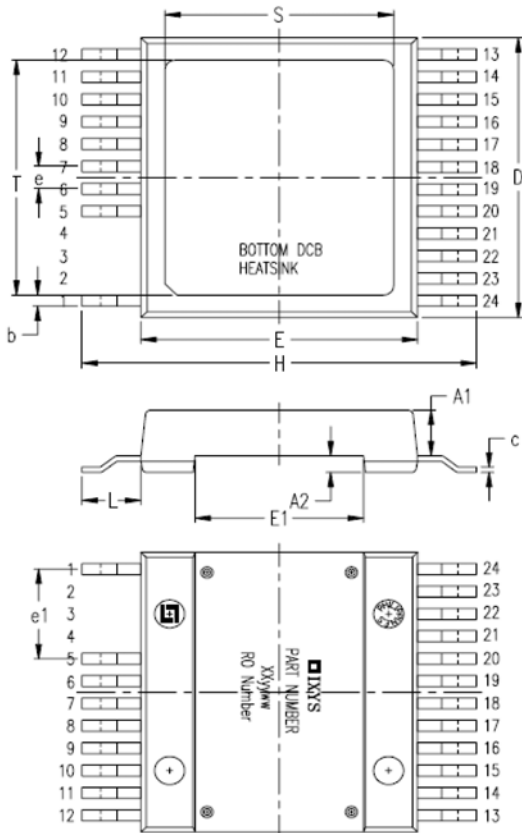
**PRELIMINARY TECHNICAL INFORMATION**

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

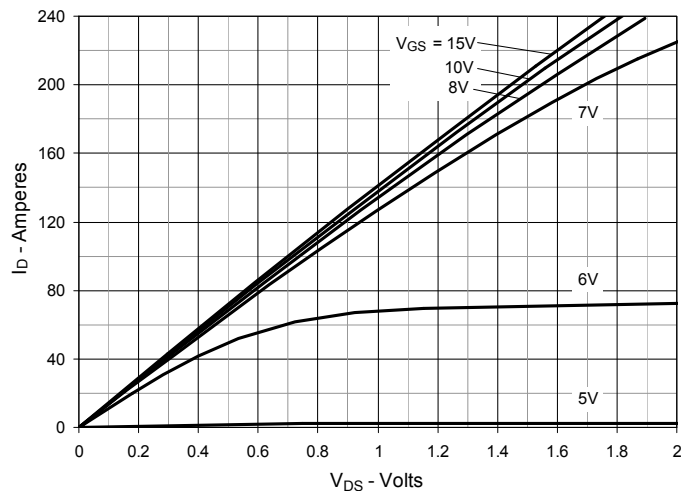
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4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

**Package Outline**


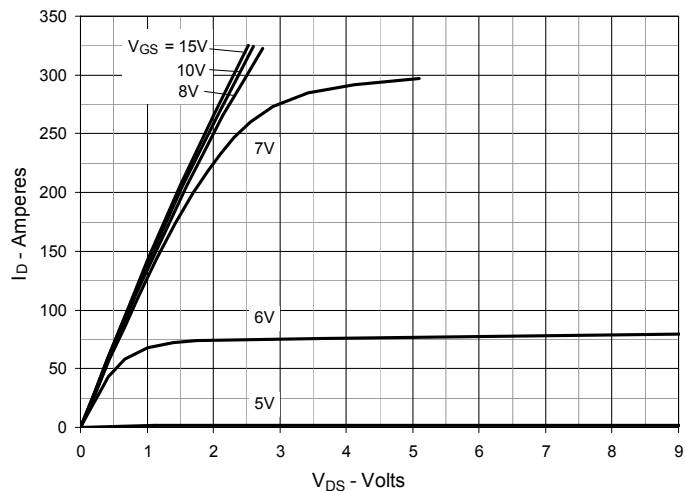
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
α	0	4°	0	4°

**PIN: 1 = Gate**  
**5-12 = Source**  
**13-24 = Drain**

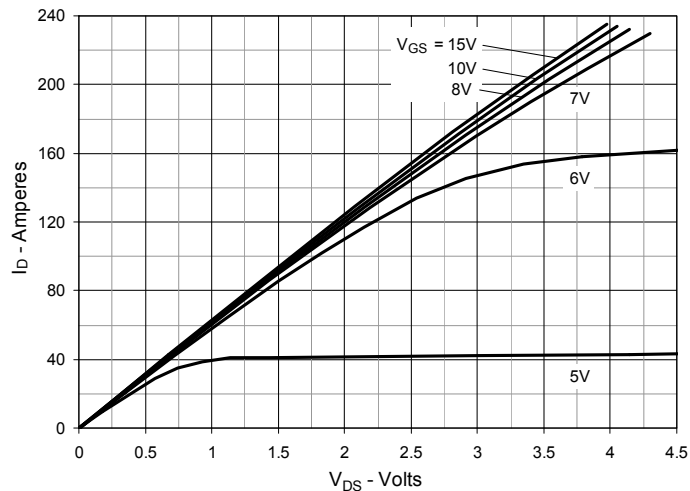
**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$**



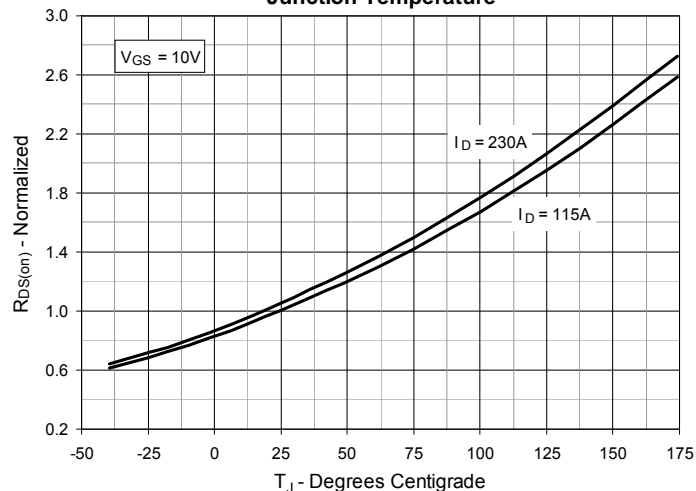
**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$**



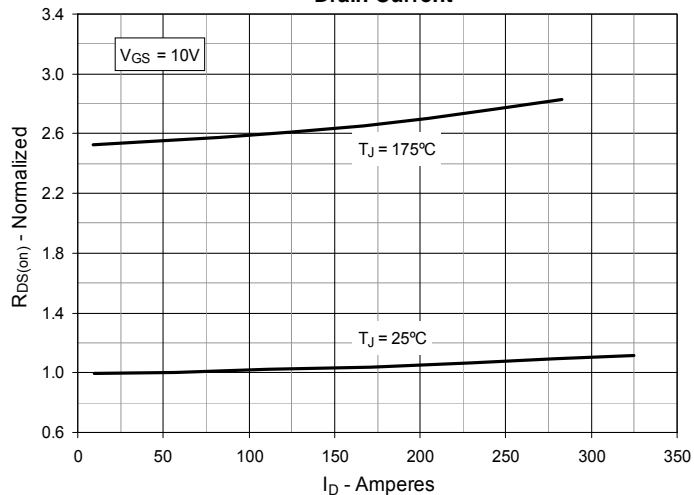
**Fig. 3. Output Characteristics @  $T_J = 150^\circ\text{C}$**



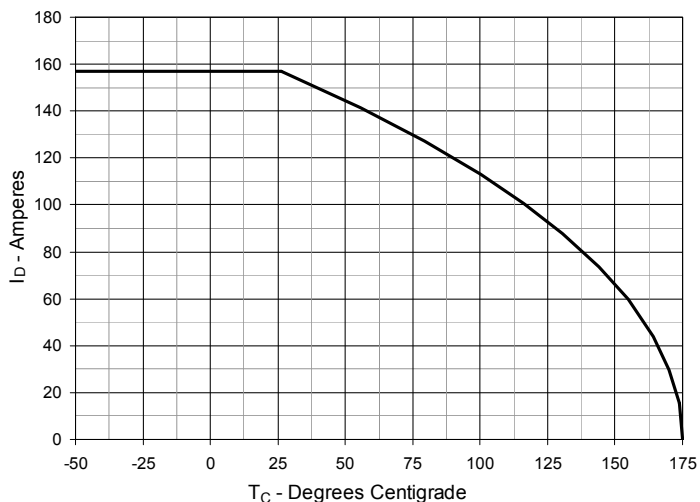
**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 115\text{A}$  Value vs. Junction Temperature**



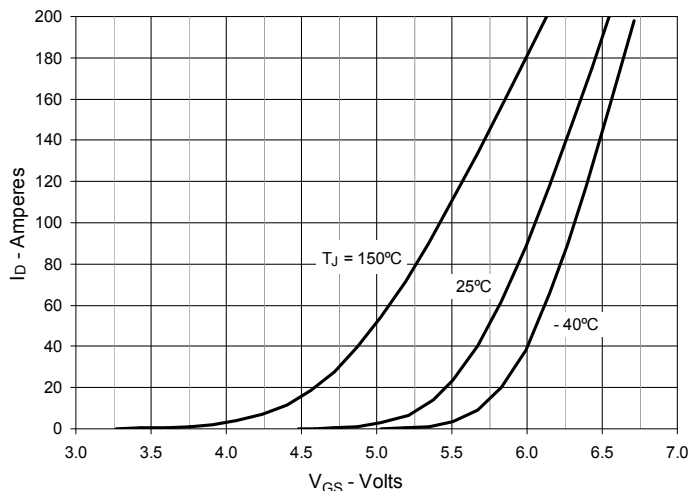
**Fig. 5.  $R_{DS(on)}$  Normalized to  $I_D = 115\text{A}$  Value vs. Drain Current**



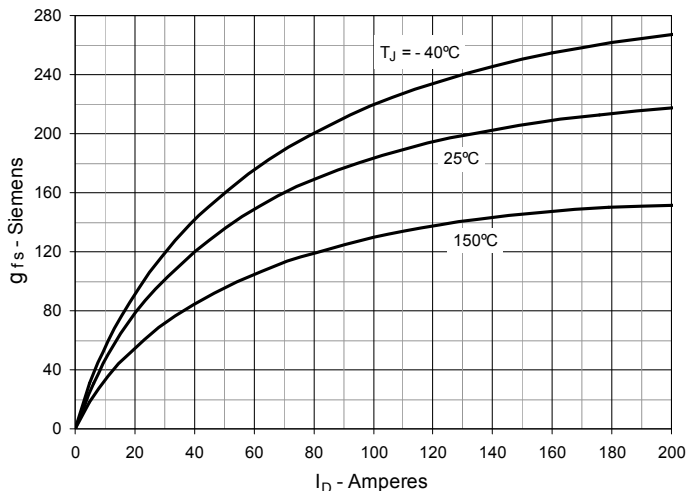
**Fig. 6. Drain Current vs. Case Temperature**



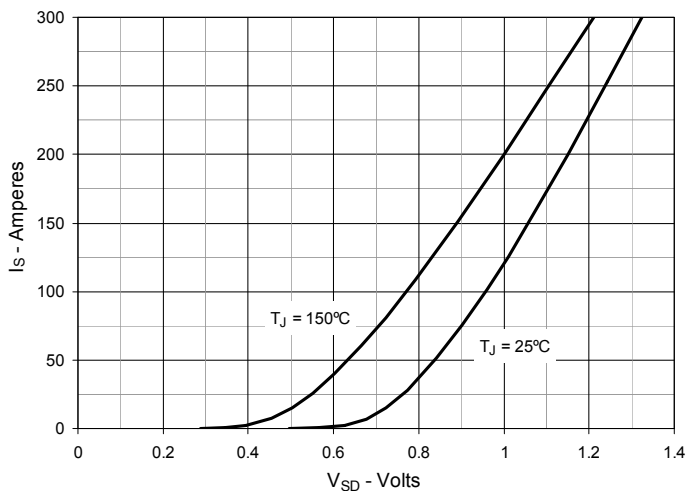
**Fig. 7. Input Admittance**



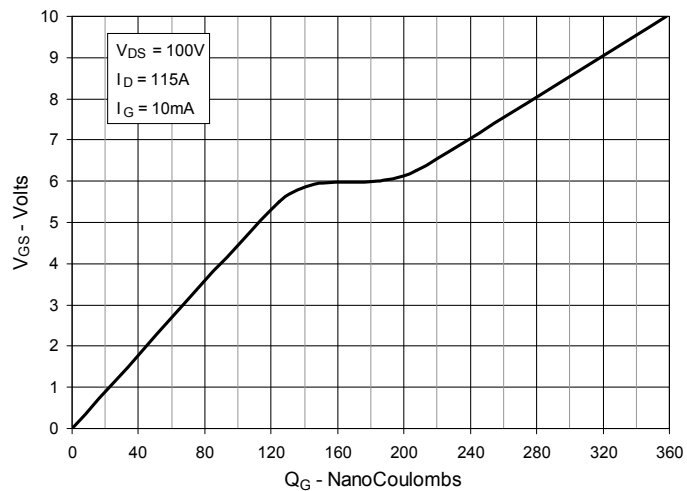
**Fig. 8. Transconductance**



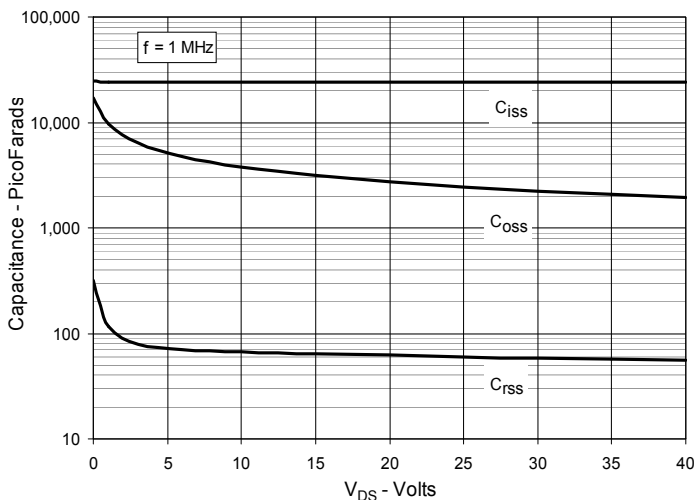
**Fig. 9. Forward Voltage Drop of Intrinsic Diode**



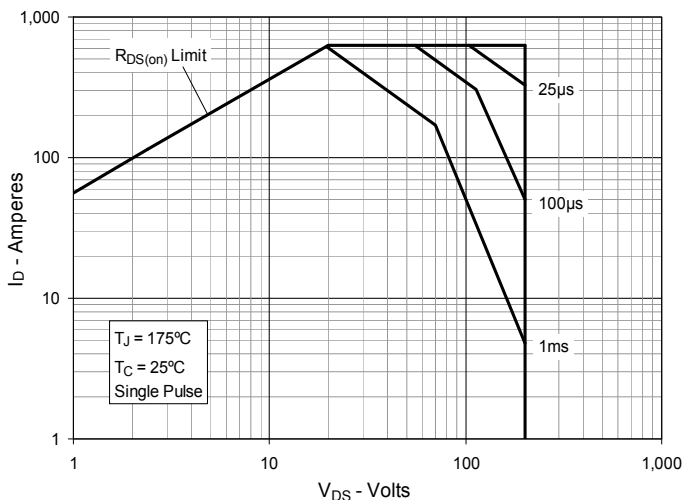
**Fig. 10. Gate Charge**



**Fig. 11. Capacitance**



**Fig. 12. Forward-Bias Safe Operating Area**



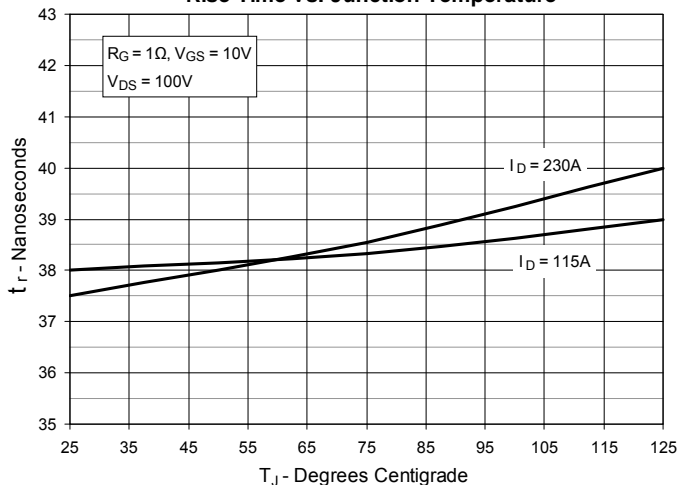
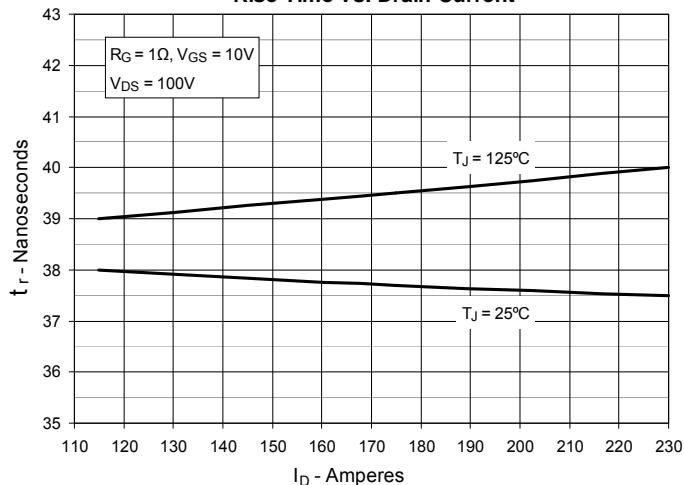
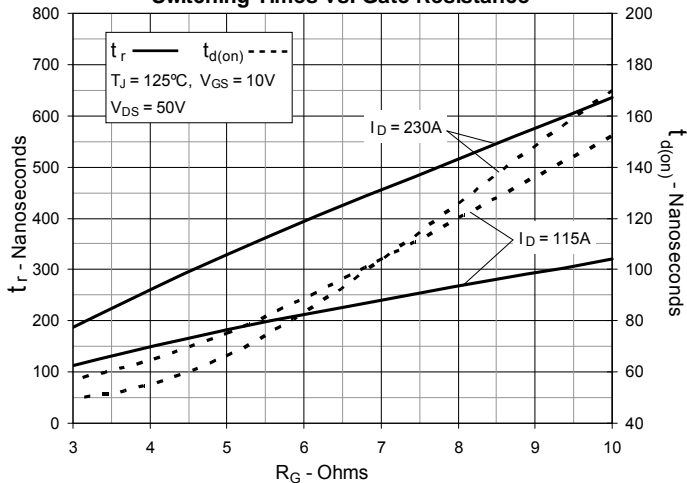
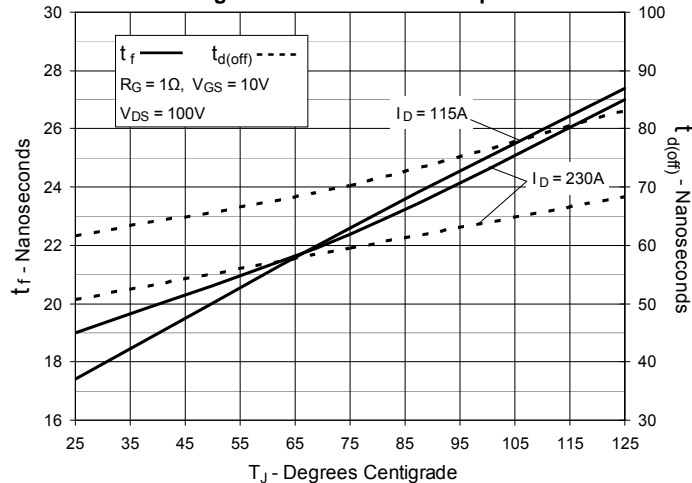
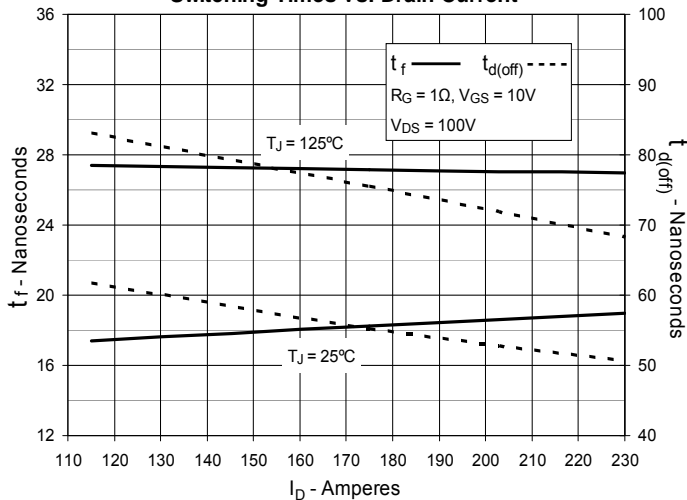
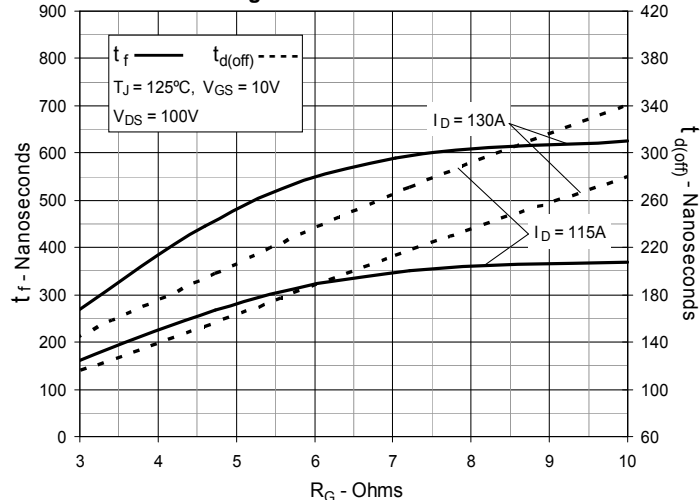
**Fig. 13. Resistive Turn-on  
Rise Time vs. Junction Temperature**

**Fig. 14. Resistive Turn-on  
Rise Time vs. Drain Current**

**Fig. 15. Resistive Turn-on  
Switching Times vs. Gate Resistance**

**Fig. 16. Resistive Turn-off  
Switching Times vs. Junction Temperature**

**Fig. 17. Resistive Turn-off  
Switching Times vs. Drain Current**

**Fig. 18. Resistive Turn-off  
Switching Times vs. Gate Resistance**


Fig. 19. Maximum Transient Thermal Impedance

