

# NP100N04PUK

R07DS0545EJ0100

Rev.1.00

Sep 23, 2011

## MOS FIELD EFFECT TRANSISTOR

### Description

The NP100N04PUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

### Features

- Super low on-state resistance  
 $R_{DS(on)} = 2.3 \text{ m}\Omega \text{ MAX. ( } V_{GS} = 10 \text{ V, } I_D = 50 \text{ A )}$
- Low  $C_{iss}$ :  $C_{iss} = 4700 \text{ pF TYP. ( } V_{DS} = 25 \text{ V )}$
- Designed for automotive application and AEC-Q101 qualified

### Ordering Information

Part No.	Lead Plating	Packing		Package
NP100N04PUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP100N04PUK-E2-AY *1			Taping (E2 type)	

Note: \*1. Pb-free (This product does not contain Pb in the external electrode.)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	40	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 100$	A
Drain Current (pulse) *1	$I_{D(pulse)}$	$\pm 400$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	176	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.8	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current *2	$I_{AR}$	43	A
Repetitive Avalanche Energy *2	$E_{AR}$	185	mJ

### Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.85	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

Notes: \*1.  $T_C = 25^\circ\text{C}$ ,  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

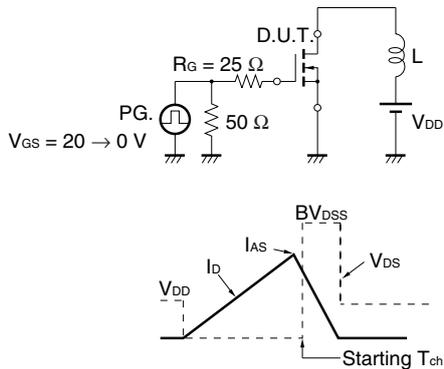
\*2.  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

**Electrical Characteristics (T<sub>A</sub> = 25°C)**

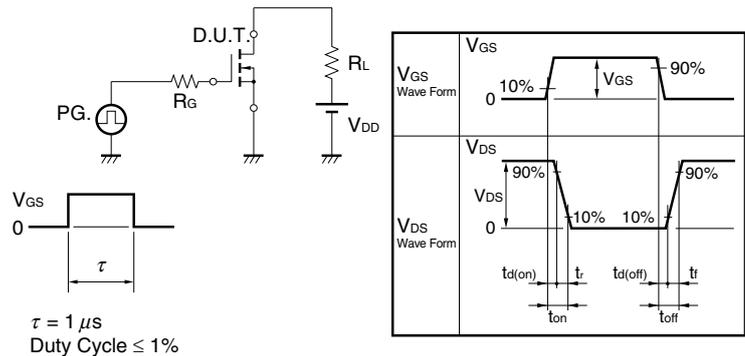
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	2.0	3.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	40	80		S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 50 A
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>		1.9	2.3	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A
Input Capacitance	C <sub>iss</sub>		4700	7050	pF	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz
Output Capacitance	C <sub>oss</sub>		660	990	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		270	490	pF	
Turn-on Delay Time	t <sub>d(on)</sub>		28	70	ns	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 50 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 0 Ω
Rise Time	t <sub>r</sub>		14	40	ns	
Turn-off Delay Time	t <sub>d(off)</sub>		70	140	ns	
Fall Time	t <sub>f</sub>		10	30	ns	
Total Gate Charge	Q <sub>G</sub>		80	120	nC	V <sub>DD</sub> = 32 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 100 A
Gate to Source Charge	Q <sub>GS</sub>		21		nC	
Gate to Drain Charge	Q <sub>GD</sub>		20		nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.9	1.5	V	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		52		ns	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Q <sub>rr</sub>		78		nC	di/dt = 100 A/μs

Note: \*1. Pulsed test

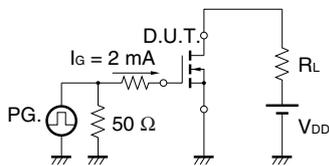
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

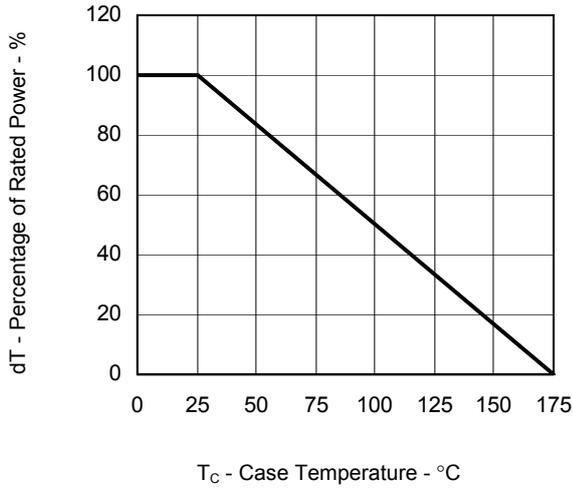


**TEST CIRCUIT 3 GATE CHARGE**

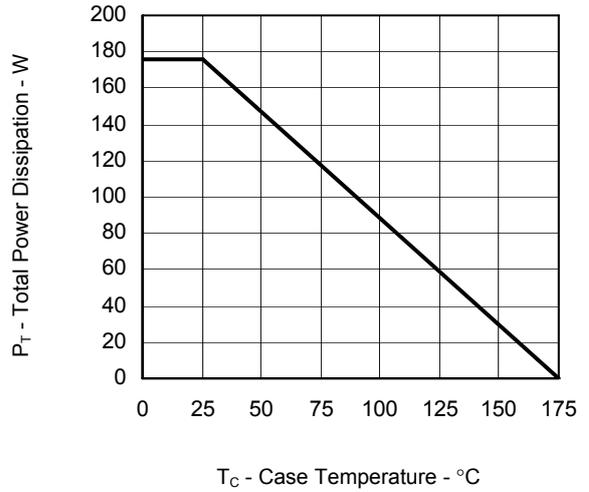


Typical Characteristics (T<sub>A</sub> = 25°C)

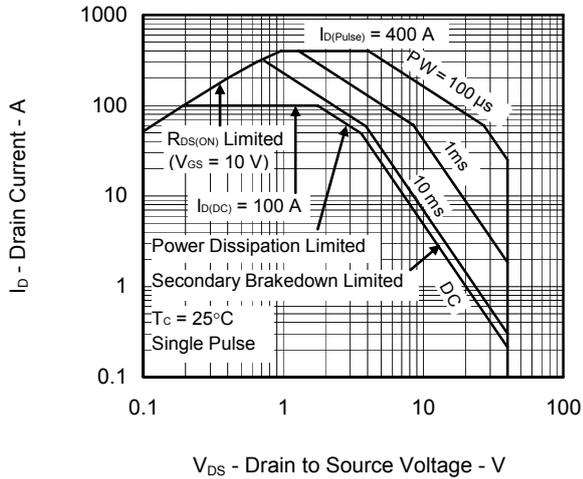
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



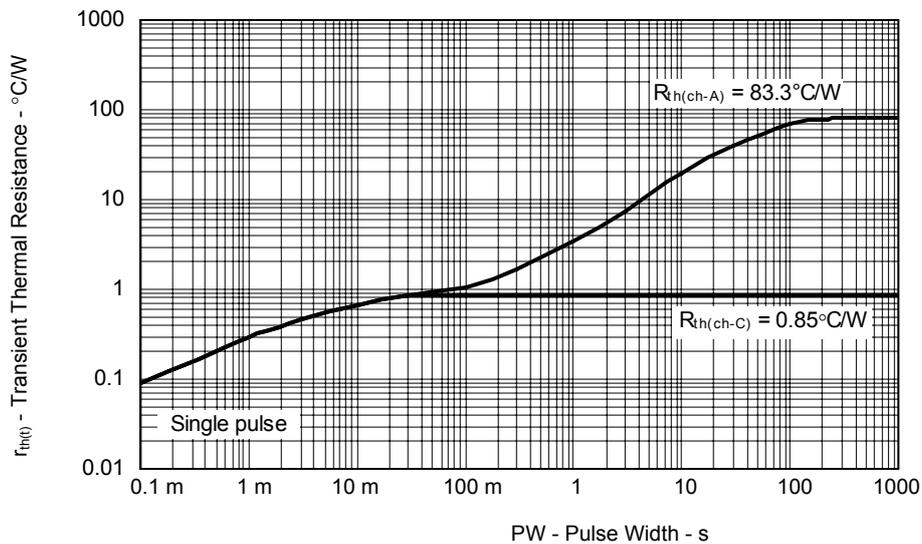
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



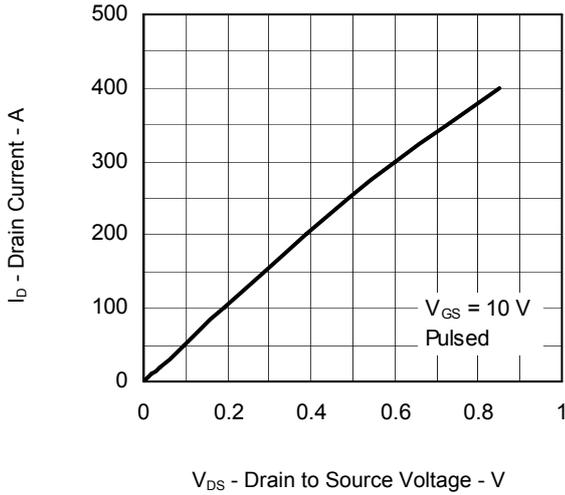
FORWARD BIAS SAFE OPERATING AREA



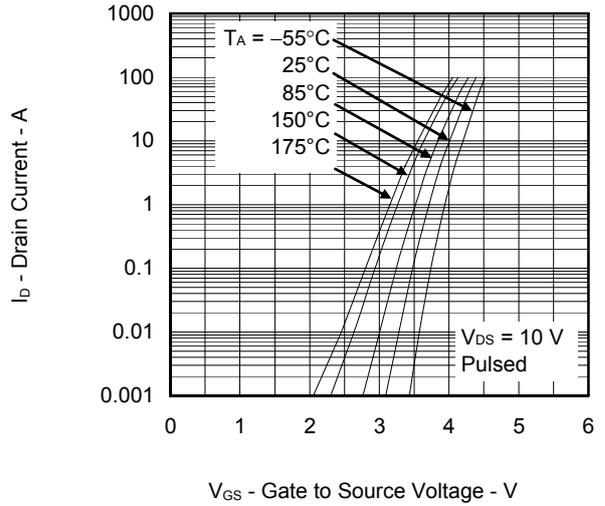
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



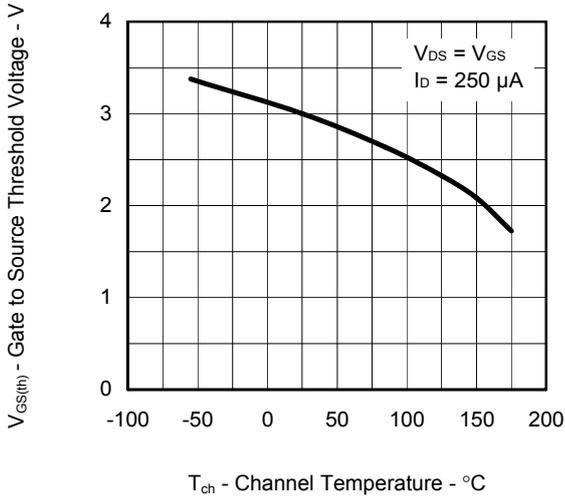
DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE



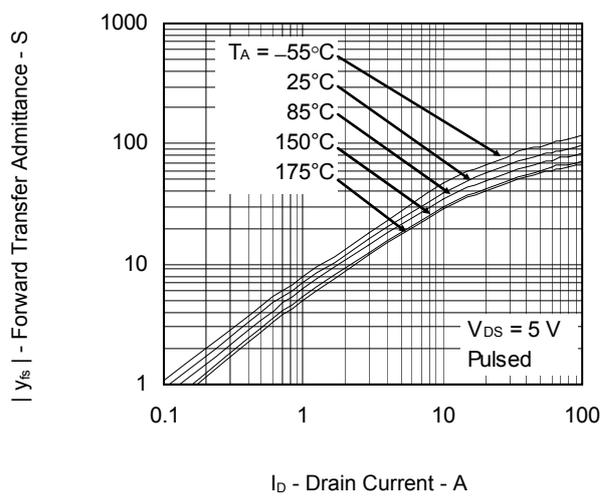
FORWARD TRANSFER CHARACTERISTICS



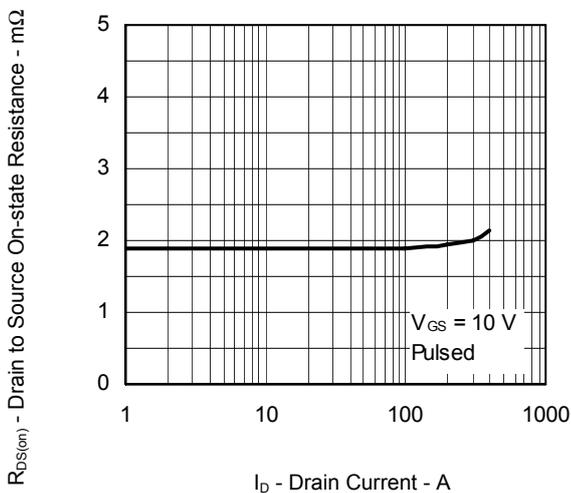
GATE TO SOURCE THRESHOLD VOLTAGE  
vs. CHANNEL TEMPERATURE



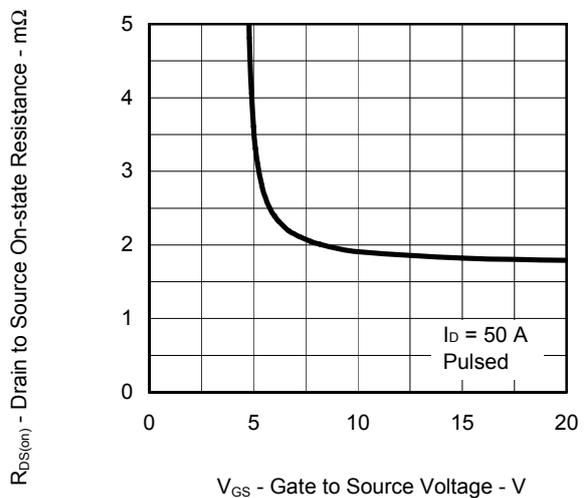
FORWARD TRANSFER ADMITTANCE vs. DRAIN  
CURRENT



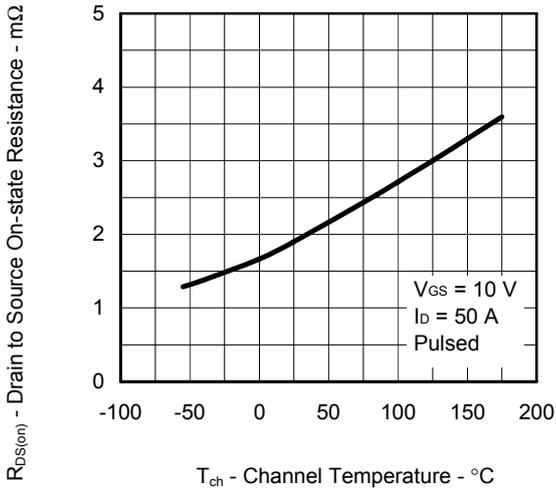
DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
DRAIN CURRENT



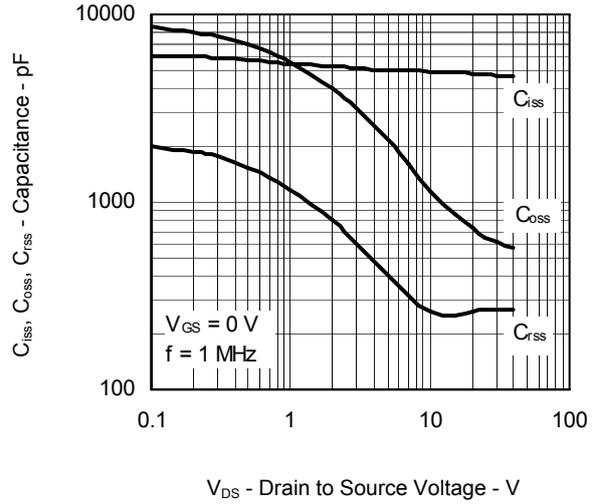
DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
GATE TO SOURCE VOLTAGE



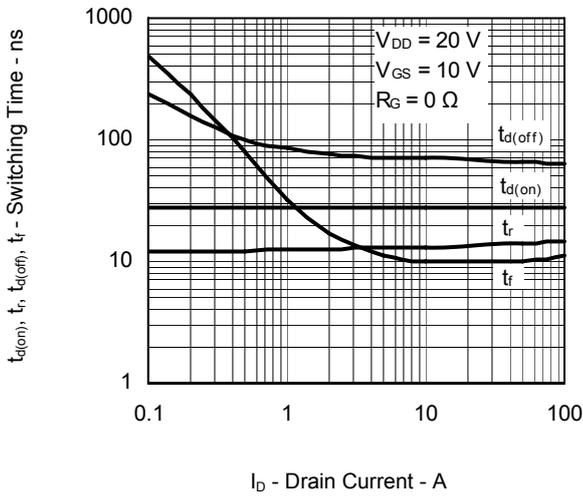
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



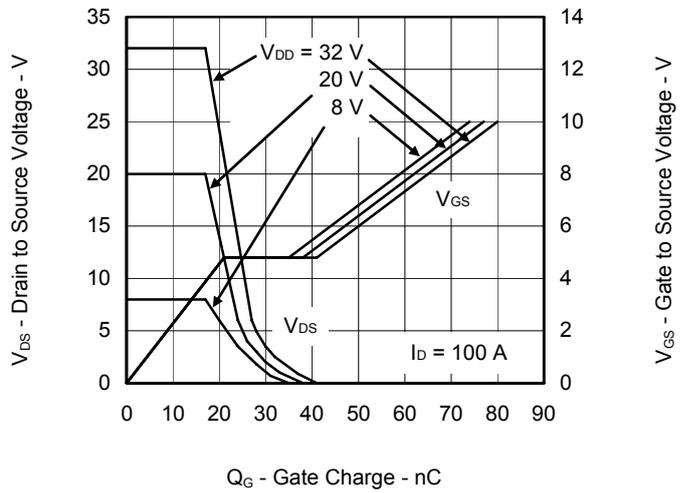
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



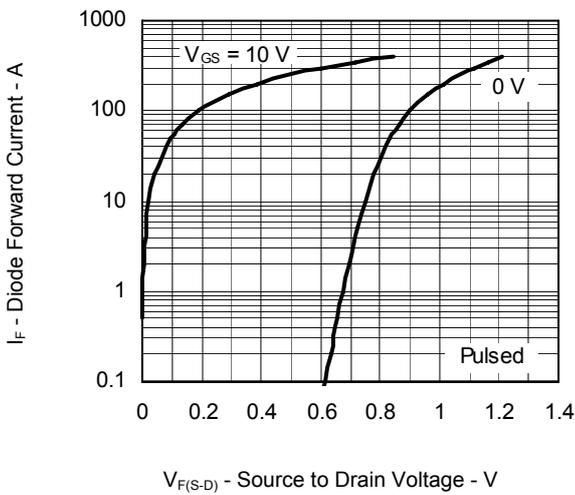
SWITCHING CHARACTERISTICS



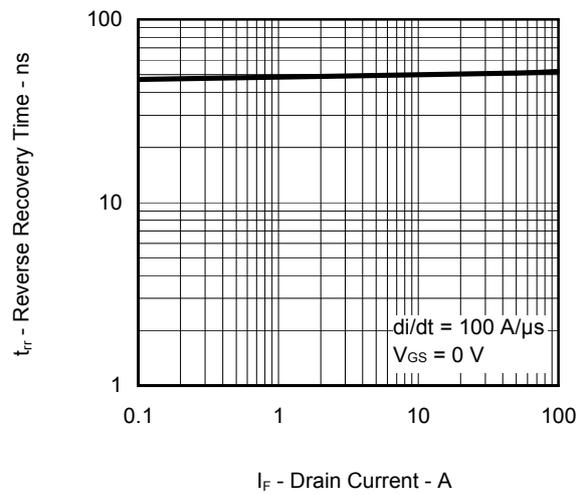
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

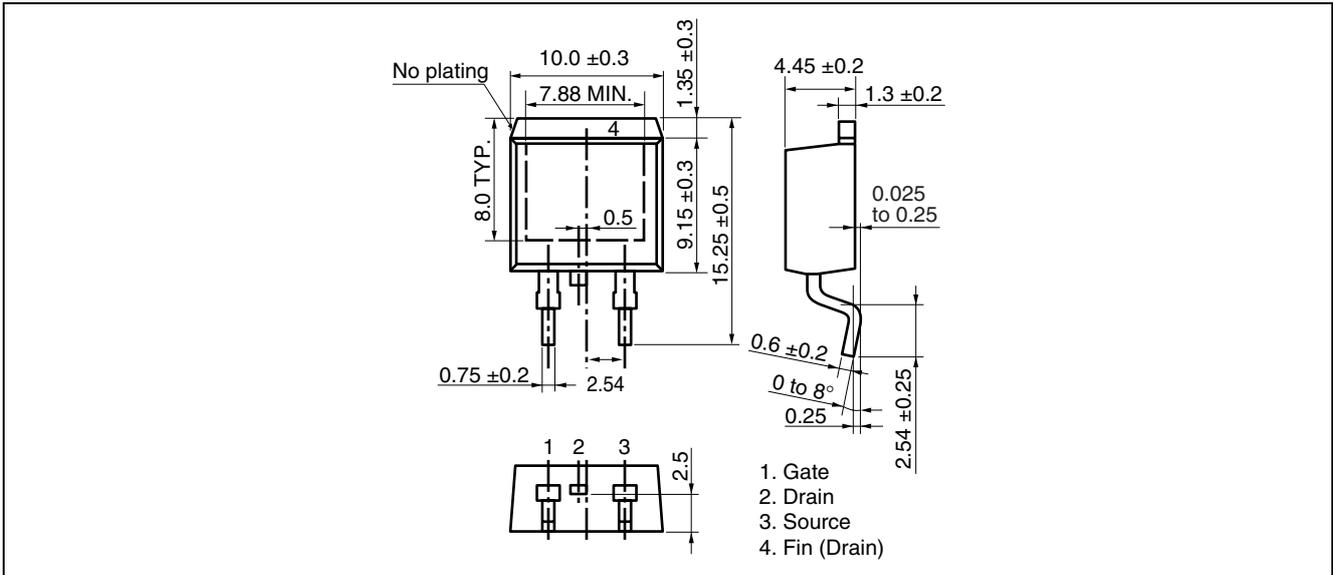


REVERSE RECOVERY TIME vs. DRAIN CURRENT

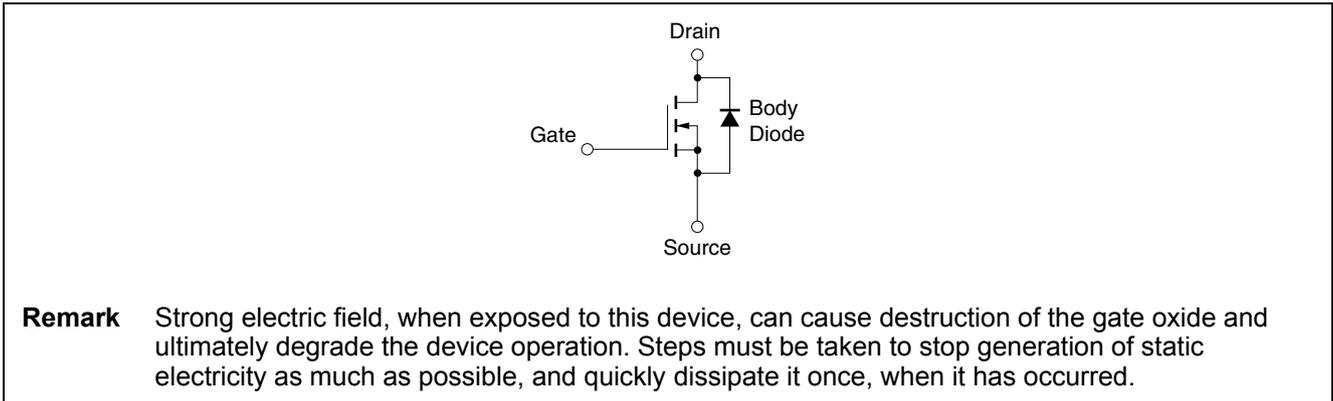


Package Drawing (Unit: mm)

TO-263 (MP-25ZP) (Mass: 1.5 g TYP.)



Equivalent Circuit



<b>Revision History</b>	<b>NP100N04PUK Data Sheet</b>
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<b>Rev.</b>	<b>Date</b>	<b>Description</b>	
		<b>Page</b>	<b>Summary</b>
1.00	Sep 23, 2011	-	First Edition Issued

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