# NTJD5121N

# Power MOSFET

## 60 V, 295 mA, Dual N−Channel with ESD Protection, SC−88

### Features

- Low $R_{DS(on)}$
- Low Gate Threshold
- Low Input Capacitance
- ESD Protected Gate
- This is a Pb−Free Device

### Applications

- Low Side Load Switch
- DC−DC Converters (Buck and Boost Circuits)

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Units |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 60 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 295 | mA |
| | | $T_A$ = 85°C | | 212 | |
| | t ≤ 5 s | $T_A$ = 25°C | | 304 | |
| | | $T_A$ = 85°C | | 219 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 250 | mW |
| | t ≤ 5 s | | | 266 | |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | 900 | mA |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) | | | $I_S$ | 210 | mA |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | $T_L$ | 260 | °C |
| Gate−Source ESD Rating (HBM, Method 3015) | | | ESD | 1400 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**THERMAL RESISTANCE RATINGS**

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Junction−to−Ambient − Steady State | $R_{\theta JA}$ | 500 | °C/W |
| Junction−to−Ambient − t ≤ 5 s | $R_{\theta JA}$ | 470 | |

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

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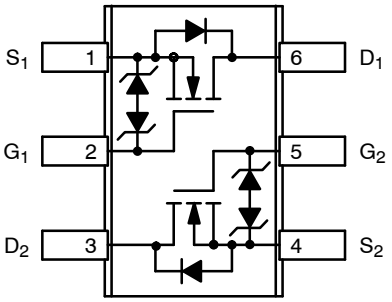
| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ Max |
|---|---|---|
| 60 V | 1.6 Ω @ 10 V | 295 mA |
| | 2.5 Ω @ 4.5 V | |

**SC−88 (SOT−363)**

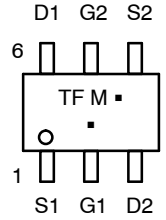



Top View

**MARKING DIAGRAM & PIN ASSIGNMENT**

1

**SC−88/SOT−363**
**CASE 419B**
**STYLE 26**




TF = Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTJD5121NT1G | SC−88 (Pb−Free) | 3000 / Tape & Reel |
| NTJD5121NT2G | SC−88 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 60 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D$ = 250 μA, ref to 25°C | | | 92 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 60 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 500 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±10 | μA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.0 | 1.7 | 2.5 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 4.0 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 500 mA | | | 1.0 | 1.6 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 200 mA | | | 1.2 | 2.5 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 5 V, $I_D$ = 200 mA | | | 80 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 20 V | | | 26 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 4.4 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 2.5 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 25 V, $I_D$ = 200 mA | | | 0.9 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 0.2 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 0.3 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 0.28 | | |
| **SWITCHING CHARACTERISTICS** (Note 3) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 4.5 V, $V_{DD}$ = 25 V, $I_D$ = 200 mA, $R_G$ = 25 Ω | | | 22 | | ns |
| Rise Time | $t_r$ | | | | 34 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 34 | | |
| Fall Time | $t_f$ | | | | 32 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 200 mA | $T_J$ = 25°C | | 0.8 | 1.2 | V |
| | | | $T_J$ = 85°C | | 0.7 | | |

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

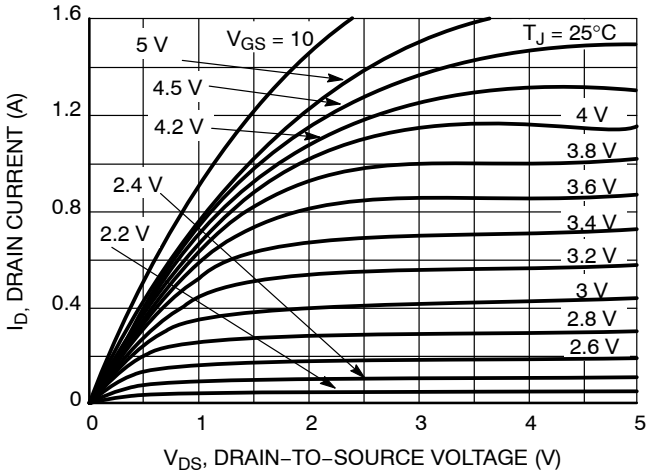



**Figure 1. On−Region Characteristics**

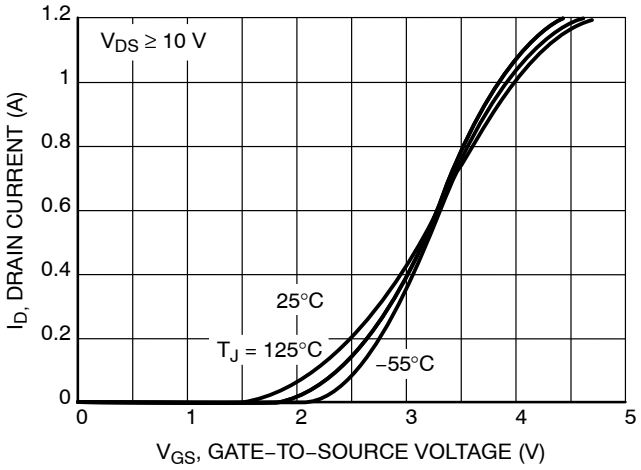



**Figure 2. Transfer Characteristics**

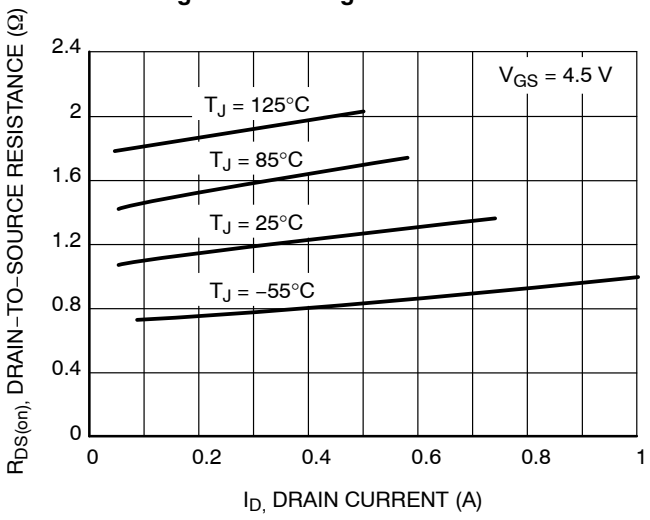



**Figure 3. On−Resistance vs. Drain Current and Temperature**

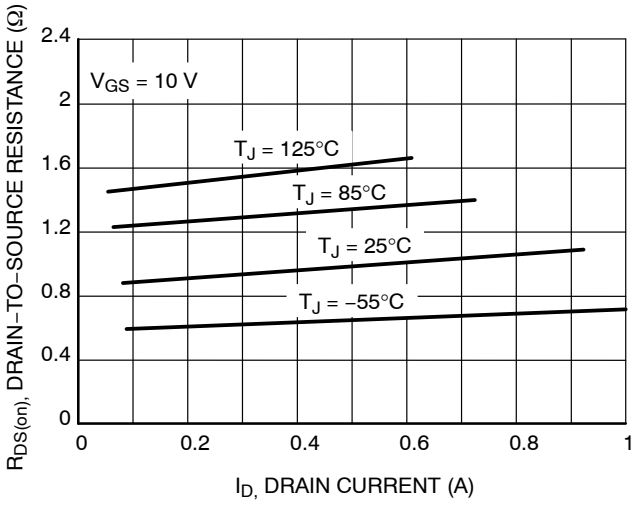



**Figure 4. On−Resistance vs. Drain Current and Temperature**

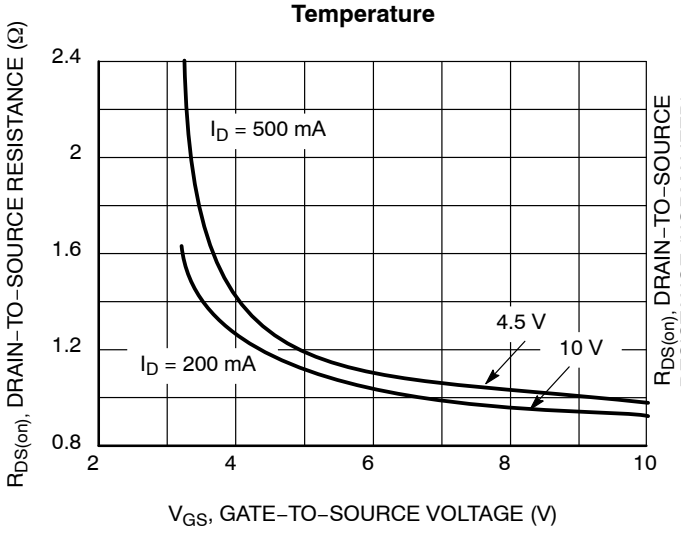



**Figure 5. On−Resistance versus Gate−to−Source Voltage**

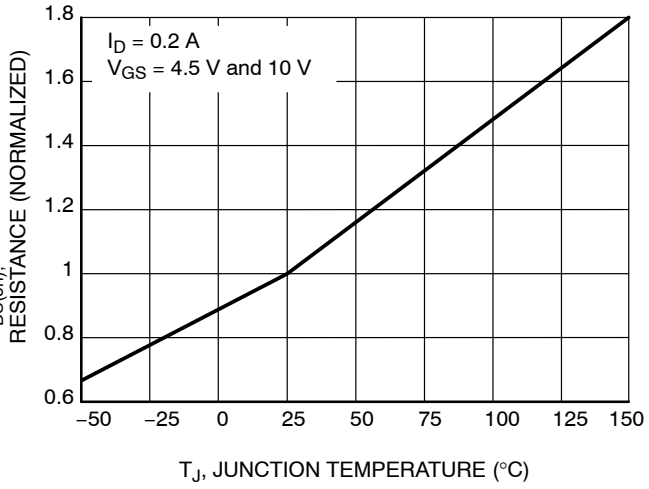



**Figure 6. On−Resistance Variation with Temperature**

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

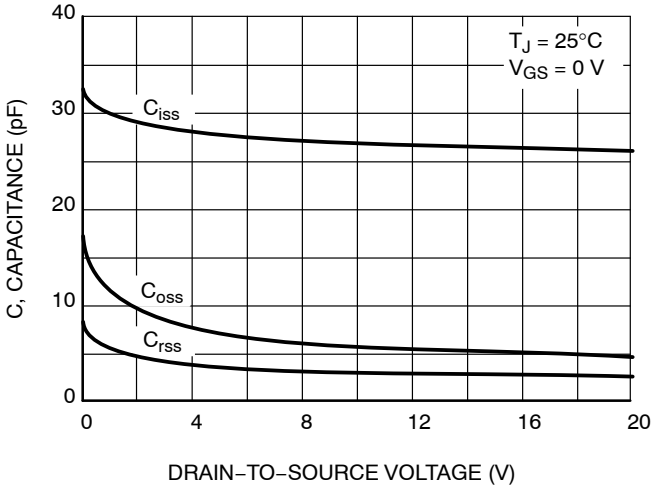



**Figure 7. Capacitance Variation**

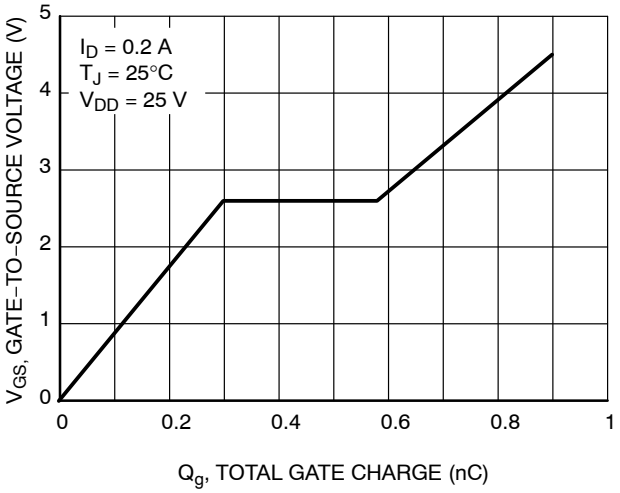



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

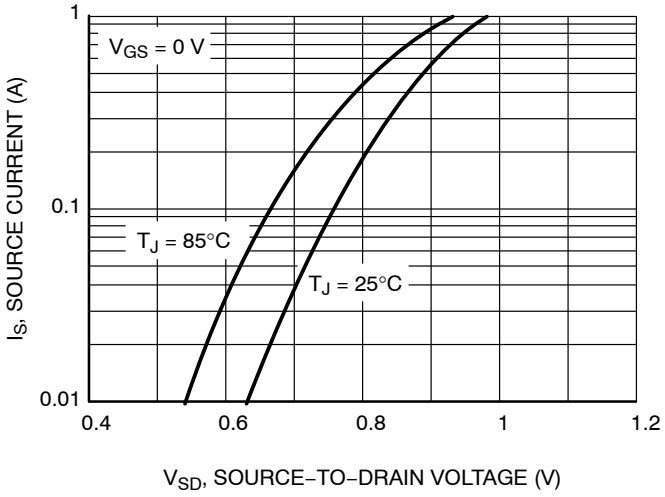
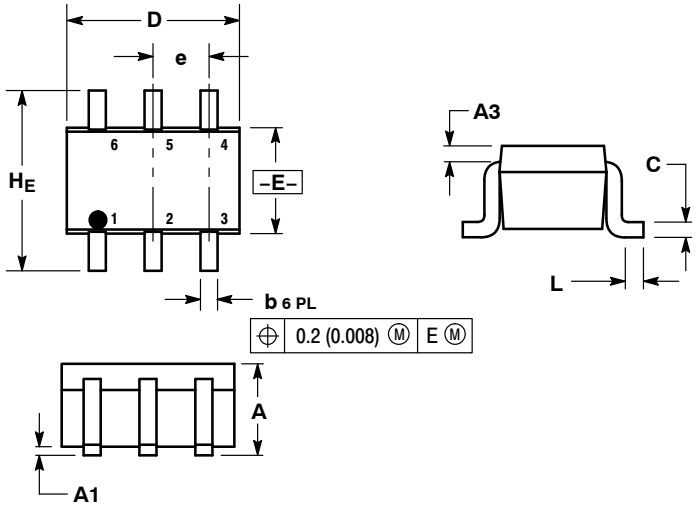



**Figure 9. Diode Forward Voltage vs. Current**

## PACKAGE DIMENSIONS

**SC−88/SC70−6/SOT−363**
CASE 419B−02
ISSUE W

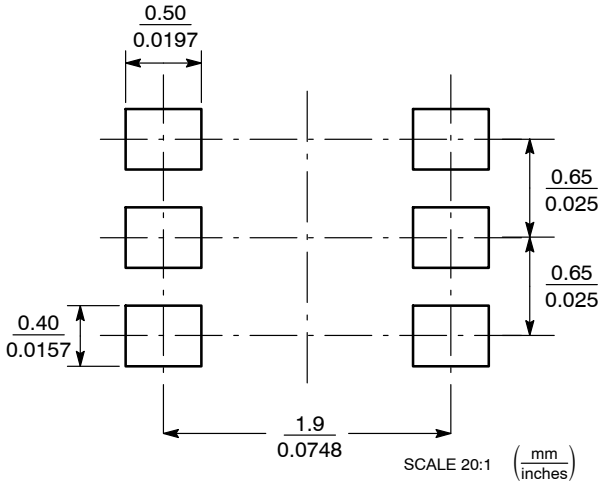



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.95 | 1.10 | 0.031 | 0.037 | 0.043 |
| A1 | 0.00 | 0.05 | 0.10 | 0.000 | 0.002 | 0.004 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.10 | 0.21 | 0.30 | 0.004 | 0.008 | 0.012 |
| C | 0.10 | 0.14 | 0.25 | 0.004 | 0.005 | 0.010 |
| D | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| E | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| $H_E$ | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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