

General Description

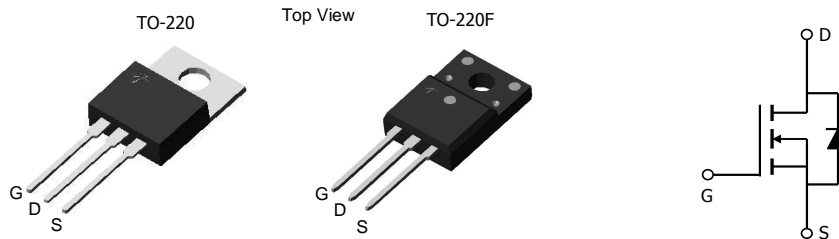
The AOT2N60 & AOTF2N60 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:
AOT2N60L & AOTF2N60L

Product Summary

V_{DS}	700V@150°C
I_D (at $V_{GS}=10V$)	2A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 4.4Ω

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	AOT2N60	AOTF2N60	Units
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	2	A
		$T_C=100^\circ\text{C}$	1.7	
Pulsed Drain Current ^C	I_{DM}	8		A
Avalanche Current ^C	I_{AR}	2		A
Repetitive avalanche energy ^C	E_{AR}	60		mJ
Single pulsed avalanche energy ^G	E_{AS}	120		mJ
Peak diode recovery dv/dt	dv/dt	5		V/ns
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	74	W
		Derate above 25°C	0.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300		°C

Thermal Characteristics

Parameter	Symbol	AOT2N60	AOTF2N60	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	°C/W
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	1.7	4	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C I _D =250μA, V _{GS} =0V, T _J =150°C	600			V
BV _{DSS} /ΔT _J	Zero Gate Voltage Drain Current	I _D =250μA, V _{GS} =0V		0.56		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V V _{DS} =480V, T _J =125°C			1 10	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3	4	4.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =1A		3.6	4.4	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =1A		3.5		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.79	1	V
I _S	Maximum Body-Diode Continuous Current				2	A
I _{SM}	Maximum Body-Diode Pulsed Current				8	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	215	270	325	pF
C _{oss}	Output Capacitance		23	29	35	pF
C _{rss}	Reverse Transfer Capacitance		2.2	2.8	3.4	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	3.5	4.4	6.6	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =2A		9.5	11.4	nC
Q _{gs}	Gate Source Charge		1.9	2.3	nC	
Q _{gd}	Gate Drain Charge		4.7	5.6	nC	
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =300V, I _D =2A, R _G =25Ω		17.2		ns
t _r	Turn-On Rise Time		14.3		ns	
t _{D(off)}	Turn-Off DelayTime		27		ns	
t _f	Turn-Off Fall Time		17		ns	
t _{rr}	Body Diode Reverse Recovery Time		I _F =2A, di/dt=100A/μs, V _{DS} =100V		154	185
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =2A, di/dt=100A/μs, V _{DS} =100V		0.80	1	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C, Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=2A, V_{DD}=150V, R_G=25Ω, Starting T_J=25°C

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

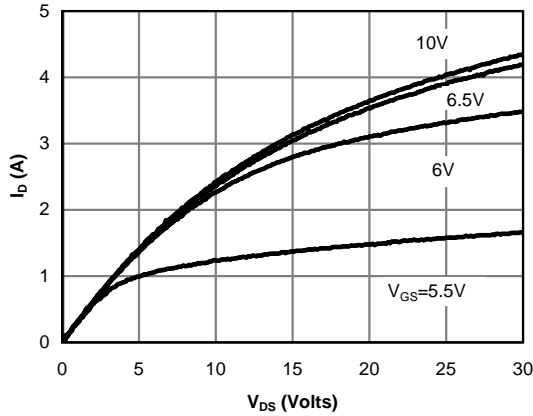


Figure 1: On-Region Characteristics

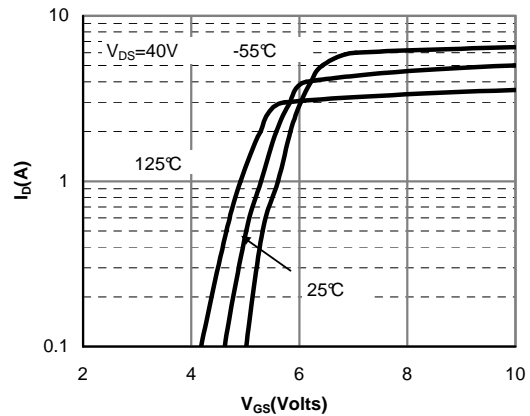


Figure 2: Transfer Characteristics

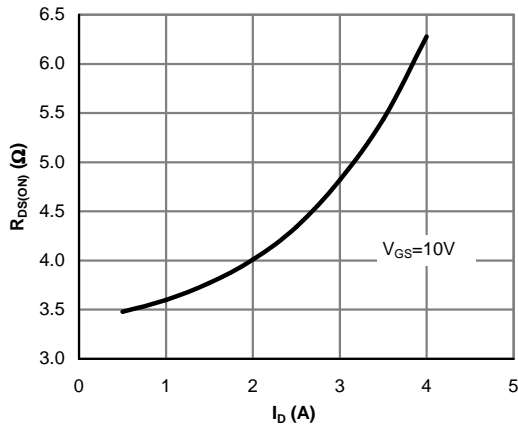


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

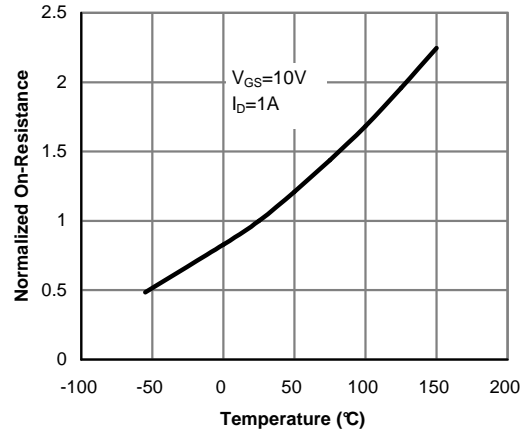


Figure 4: On-Resistance vs. Junction Temperature

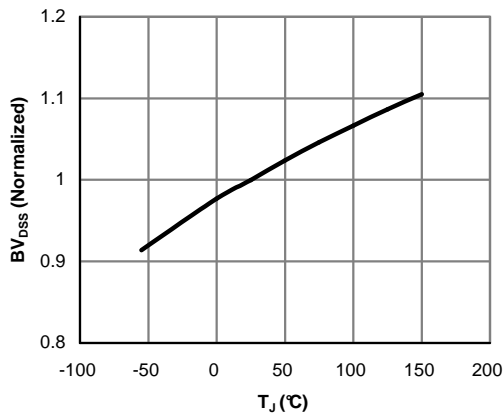


Figure 5: Break Down vs. Junction Temperature

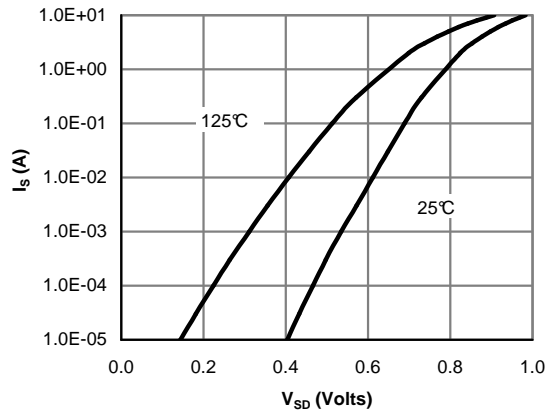


Figure 6: Body-Diode Characteristics (Note E)

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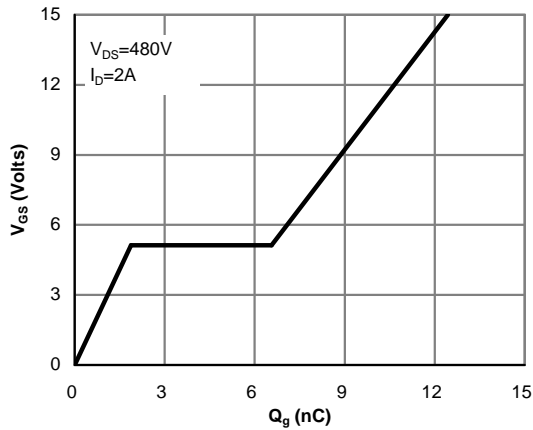


Figure 7: Gate-Charge Characteristics

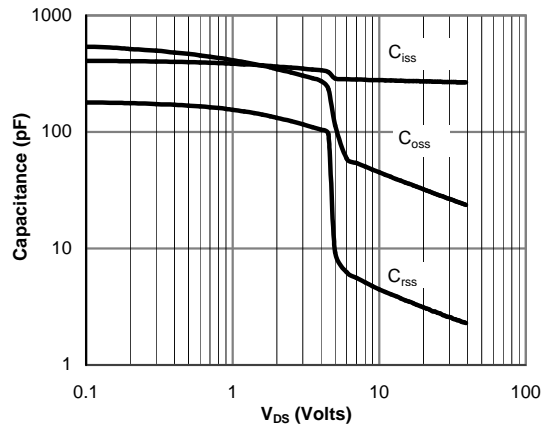


Figure 8: Capacitance Characteristics

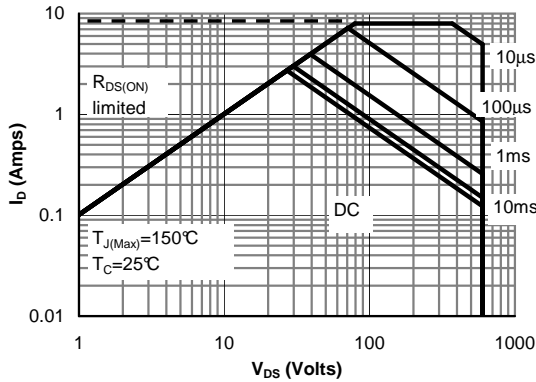


Figure 9: Maximum Forward Biased Safe Operating Area for AOT2N60 (Note F)

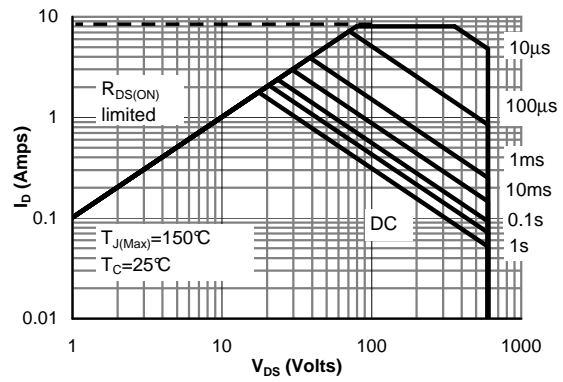


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF2N60 (Note F)

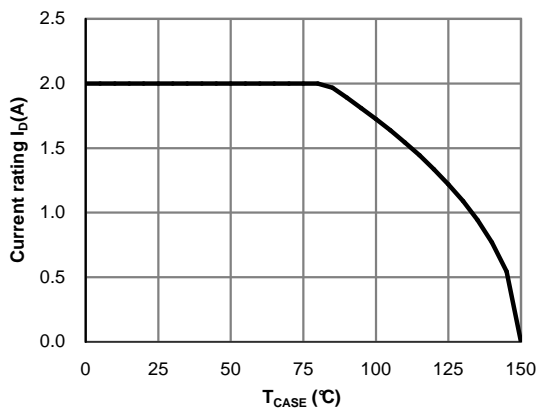


Figure 11: Current De-rating (Note B)

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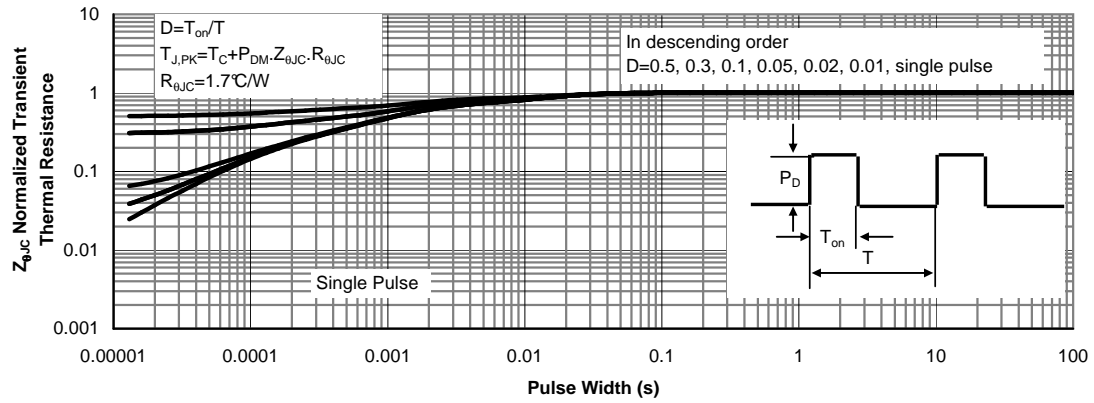


Figure 12: Normalized Maximum Transient Thermal Impedance for AOT2N60 (Note F)

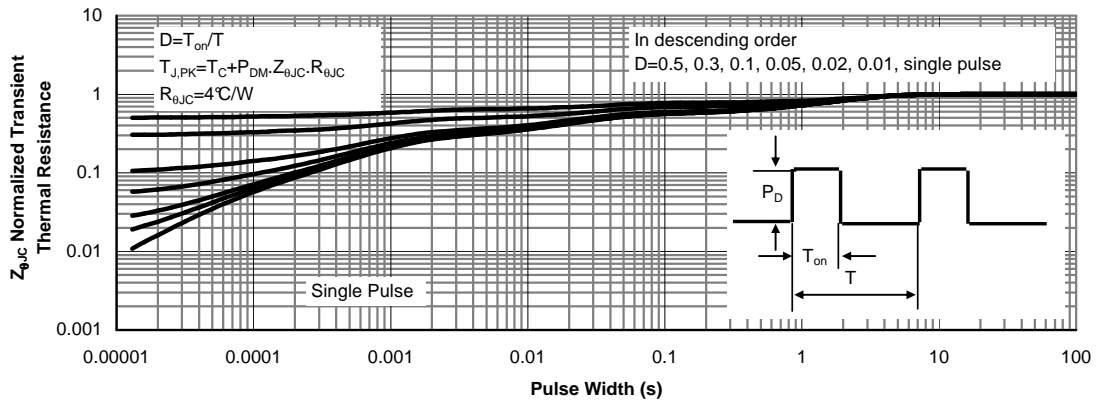
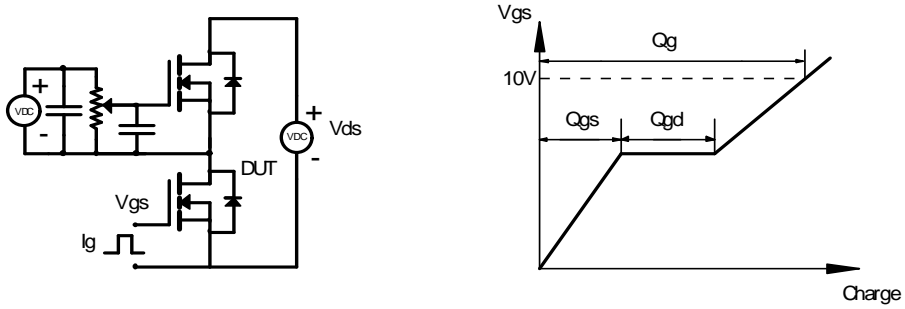


Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF2N60 (Note F)

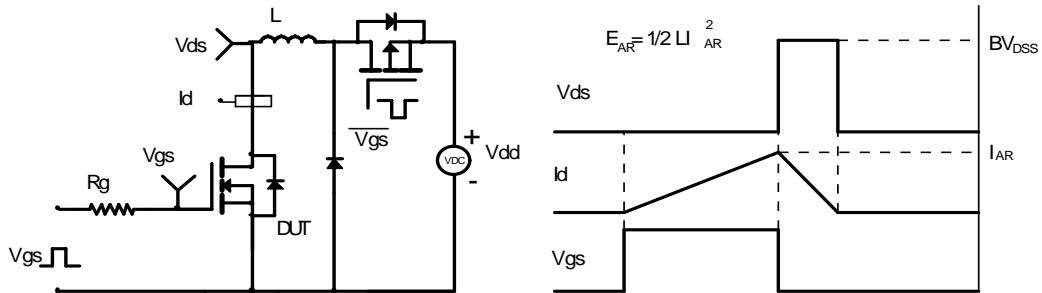
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

