

DS21Q348DK

3.3V E1/T1/J1 Line Interface Design Kit Daughter Card

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GENERAL DESCRIPTION

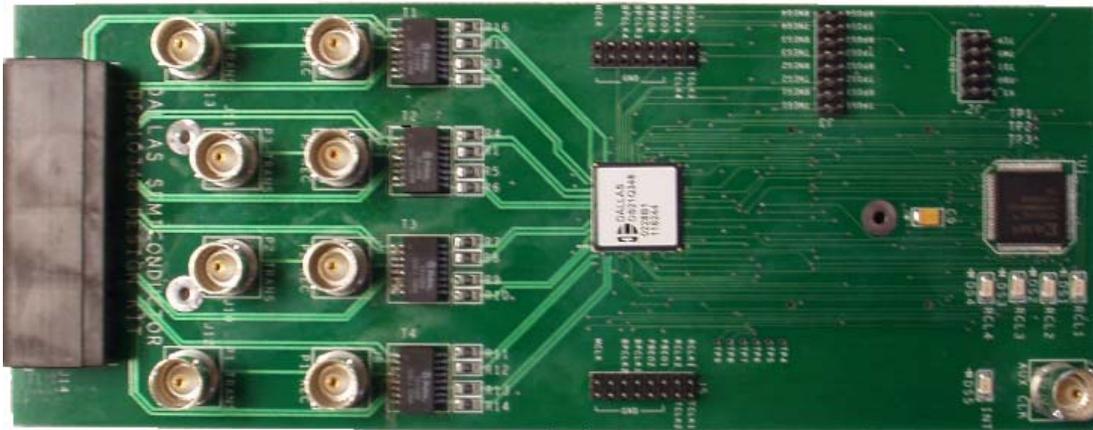
The DS21Q348 design kit is an evaluation board for the DS21Q348 3.3V E1/T1/J1 line interface. The DS21Q348DK is intended to be used as a daughter card with either the DK2000 or the DK101 motherboards. The board comes complete with a line interface unit (LIU), transformers, termination resistors, configuration switches, network connectors, and an interface to the motherboard.

ORDERING INFORMATION

PART	DESCRIPTION
DS21Q348DK	DS21Q348 (Quad BGA) Design Kit

FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Interfaces Directly to the DK101 or DK2000 Motherboards
- Demonstrates Key Functions of the DS21Q348
- High-Level Software Provides Visual Access to Registers
- Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- BNC Connections for 75Ω E1
- Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1
- Multitap Transformer Facilitates True Impedance Matching for 75Ω and 120Ω/100Ω Paths



COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
1	1	3.3V E1/T1/J1 line interface, 0°C to +70°C, 144-pin BGA	Dallas Semiconductor	DS21Q348
C1, C2, C6, C10, C12, C22, C24	7	0.47µF 10%, 25V ceramic capacitors (1206)	Digi-Key	PCC1891CT-ND
C13–C16	4	0.1µF 10%, 25V ceramic capacitors (1206)	Digi-Key	PCC1883CT-ND
C17–C20	4	1µF 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C3–C5, C7, C8, C11, C21, C23, C25, C26	10	0.1µF 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C9	1	10µF 20%, 16V tantalum capacitors (B case)	Digi-Key	PCS3106CT-ND
DS1–DS5	5	LED, red, SMD	Digi-Key	P500CT-ND
J1, J6–J13	9	Right-angle, 5-pin BNC connectors	Kruvand	UCBJR220
J14	1	Right-angle RJ45, 8-pin, 4-port jack	Molex	43223-8140
J15, J16	2	50-pin, dual row, vertical SMD sockets	Samtec	TFM-125-02-S-D-LC
J2	1	10-pin, dual row, vertical connector	Digi-Key	S2012-05-ND
J3–J5	—	8-row by 2-column pin strip, 0.1" centers, 0.025" post	NA	Lab Stock
R17, R20, R21, R25, R28–R36, R53	14	10kΩ 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R18, R19, R22–R24, R26, R27	7	51.1Ω 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R1–R16, R37–R41, R54–R57	25	0Ω 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R42, R43	2	1.0kΩ 1%, 1/10W resistors (0805)	Digi-Key	P1.00KCCT-ND
R44–R51	8	61.9Ω 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
T1–T4	4	XFMR, dual, 16-pin SMT	Pulse Engineering	TX1099
U1	1	Xilinx CPLD 72 macrocell, 100-pin TQFP, 3.3V	Avnet	XC95142XL-10TQ100C

BASIC OPERATION

Hardware Configuration

Using the DK101 Processor Board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V. (The external 5V connector is unused. Additionally, the TIM 5V supply headers are unused.)
- All processor-board DIP switch settings should be in the ON position with the exception of the flash-programming switch, which should be OFF.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation in options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

Using the DK2000 Processor Board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation in options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

General:

- Upon power-up, the RCL LEDs are lit, and the INT LED is off.
- After power-up, the RCL LEDs extinguish upon external loopback.
- Due to the dual winding transformer, only the 120 Ω line build-out configuration setting is needed to cover 75 Ω E1 and 120 Ω E1.

Quick Setup (Register View)

- The PC loads the program, offering a choice between DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program requests a definition file. Select DS21Q348DK02A0_CPLD.DEF.
- The Register View Screen appears, showing the register names, acronyms, and values. Note the CPLD def file contains a link such that the def file for the DS21Q348 is also loaded. Selection among the def files is accomplished using the drop-down box on the right-hand side of the program window.
- From the drop-down box select the DS21Q348 def file and configure register CCR3 of ports 1 through 4 with a 90h.
 - The device begins transmitting a pseudorandom bit sequence. Upon external loopback, the RCL LED extinguishes, denoting that the device has found a carrier and has successfully decoded the pseudorandom bit sequence. For more advanced configurations, please refer to the DS21Q348 data sheet.

Miscellaneous:

- Clock frequencies are provided by a register-mapped CPLD, which is on the DS21Q348 daughter card.
- The definition file for this CPLD is named *DS21Q348DK02A0_CPLD.def*. See *CPLD Register Map* definitions.

ADDRESS MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets in the *Daughter Card Address Map* table are relative to the beginning of the daughter card address space.

Daughter Card Address Map

OFFSET	DEVICE	FUNCTION
0X0000 to 0X0015	CPLD	Board ID, clock and signal routing
0X2000 to 0X2015	LIU Port 1	Board is populated with either the DS21Q348 or the DS21448. Please see the factory data sheet for details.
0X3000 to 0X3015	LIU Port 2	
0X4000 to 0X4015	LIU Port 3	
0X5000 to 0X5015	LIU Port 4	

Registers in the CPLD can be easily modified using ChipView, a host-based user-interface software, with the definition file named *ds21q348dk02A0_cpld.def*. This file is included as part of the design kit documentation download (accessed through the DS21Q348's quick view data sheet). The definition file for the LIU is named *DS21Q348.def*.

CPLD Register Map

OFFSET	REGISTER	TYPE	FUNCTION
0X0000	BID	Read-Only	Board ID
0X0001	—	—	Unused
0X0002	XBIDH	Read-Only	High Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	MCLK_SRC	Read-Write	MCLK Source Register
0X0012	TCLK1_SRC	Read-Write	TCLK1 Source Register
0X0013	TCLK2_SRC	Read-Write	TCLK2 Source Register
0X0014	TCLK3_SRC	Read-Write	TCLK3 Source Register
0X0015	TCLK4_SRC	Read-Write	TCLK4 Source Register

ID Registers

OFFSET	NAME	FUNCTION
0X0000	BID	Board ID. BID is read-only with a value of 0xD.
0X0002	XBIDH	High Nibble Extended Board ID. XBIDH is read-only with a value of 0x00.
0X0003	XBIDM	Middle Nibble Extended Board ID. XBIDM is read-only with a value of 0x02.
0X0004	XBIDL	Low Nibble Extended Board ID. XBIDL is read-only with a value of 0x00.
0X0005	BREV	Board FAB Revision. BREV is read-only and displays the current fab revision.
0X0006	AREV	Board Assembly Revision. AREV is read-only and displays the assembly revision.
0X0007	PREV	PLD Revision. PREV is read-only and displays the current PLD firmware revision.

Control Registers

The control registers are used set the clock frequency on the MCLK and TCLK pins. Options are 1.544MHz, 2.048MHz, external source (through AUX CLK BNC), and tri-state.

MCLK_SRC: MCLK SOURCE (OFFSET = 0x0011) INITIAL VALUE = 0x1

(MSB)					(LSB)		
—	—	—	—	HI_Z	EXTOSC	2048MHZ	1544MHZ

NAME	POSITION	FUNCTION
HI_Z	MCLK_SRC.3	1 = Tri-state MCLK.
EXTOSC	MCLK_SRC.2	1 = Connect MCLK to the external oscillator.
2048MHZ	MCLK_SRC.1	1 = Connect MCLK to the 2.048MHz clock.
1544MHZ	MCLK_SRC.0	1 = Connect MCLK to the 1.544MHz clock.

TCLK1_SRC: TCLK SOURCE (OFFSET = 0x0012) INITIAL VALUE = 0x1

(MSB)					(LSB)		
—	—	—	—	HI_Z	EXTOSC	2048MHZ	1544MHZ

NAME	POSITION	FUNCTION
HI_Z	TCLK1_SRC.3	1 = Tri-state TCLK1.
EXTOSC	TCLK1_SRC.2	1 = Connect TCLK1 to the external oscillator.
2048MHZ	TCLK1_SRC.1	1 = Connect TCLK1 to the 2.048MHz clock.
1544MHZ	TCLK1_SRC.0	1 = Connect TCLK1 to the 1.544MHz clock.

TCLK2_SRC: TCLK SOURCE (OFFSET = 0x0013) INITIAL VALUE = 0x1

(MSB)					(LSB)		
—	—	—	—	HI_Z	EXTOSC	2048MHZ	1544MHZ

NAME	POSITION	FUNCTION
HI_Z	TCLK2_SRC.3	1 = Tri-state TCLK2.
EXTOSC	TCLK2_SRC.2	1 = Connect TCLK2 to the external oscillator.
2048MHZ	TCLK2_SRC.1	1 = Connect TCLK2 to the 2.048MHz clock.
1544MHZ	TCLK2_SRC.0	1 = Connect TCLK2 to the 1.544MHz clock.

TCLK3_SRC: TCLK SOURCE (OFFSET = 0x0014) INITIAL VALUE = 0x1

(MSB)					(LSB)		
—	—	—	—	HI_Z	EXTOSC	2048MHZ	1544MHZ

NAME	POSITION	FUNCTION
HI_Z	TCLK3_SRC.3	1 = Tri-state TCLK3.
EXTOSC	TCLK3_SRC.2	1 = Connect TCLK3 to the external oscillator.
2048MHZ	TCLK3_SRC.1	1 = Connect TCLK3 to the 2.048MHz clock.
1544MHZ	TCLK3_SRC.0	1 = Connect TCLK3 to the 1.544MHz clock.

TCLK4_SRC: TCLK SOURCE (OFFSET = 0x0015) INITIAL VALUE = 0x1

(MSB)							(LSB)
—	—	—	—	HI_Z	EXTOSC	2048MHZ	1544MHZ

NAME	POSITION	FUNCTION
HI_Z	TCLK4_SRC.3	1 = Tri-state TCLK4.
EXTOSC	TCLK4_SRC.2	1 = Connect TCLK4 to the external oscillator.
2048MHZ	TCLK4_SRC.1	1 = Connect TCLK4 to the 2.048MHz clock.
1544MHZ	TCLK4_SRC.0	1 = Connect TCLK4 to the 1.544MHz clock.

DS21Q348 INFORMATION

For more information about the DS21Q348, please consult the DS21Q348 data sheet available on our website, www.maxim-ic.com/DS21Q348.

DS21Q348DK INFORMATION

For more information about the DS21Q348DK, including software downloads, please consult the DS21Q348DK data sheet available on our website at www.maxim-ic.com/DS21Q348DK.

TECHNICAL SUPPORT

For additional technical support, please email your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS21Q348 schematics are featured in the following 11 pages.

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DS21Q348 DESIGN KIT
DS21Q348DK02A0

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11. PART CROSS REFERENCE

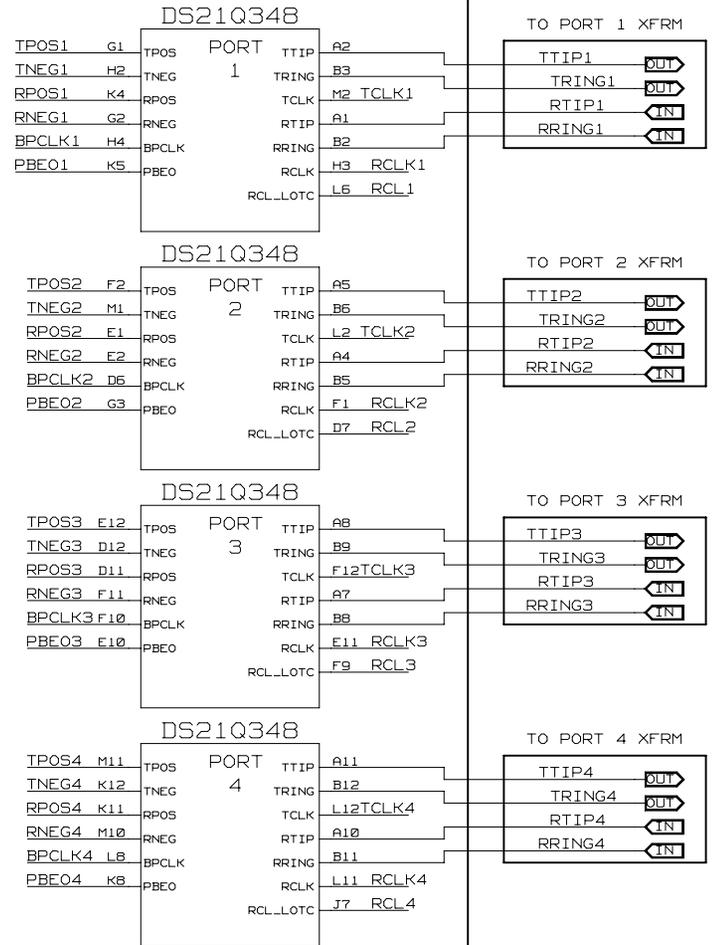
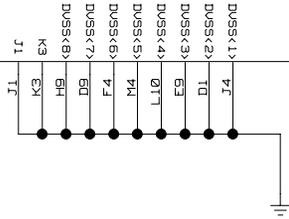
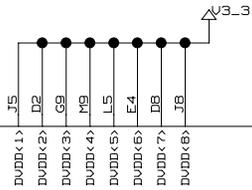
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DS21Q48 3.3V E1/T1/J1 LINE INTERFACE. 100 PIN MULTI-CHIP MODULE (BGA)

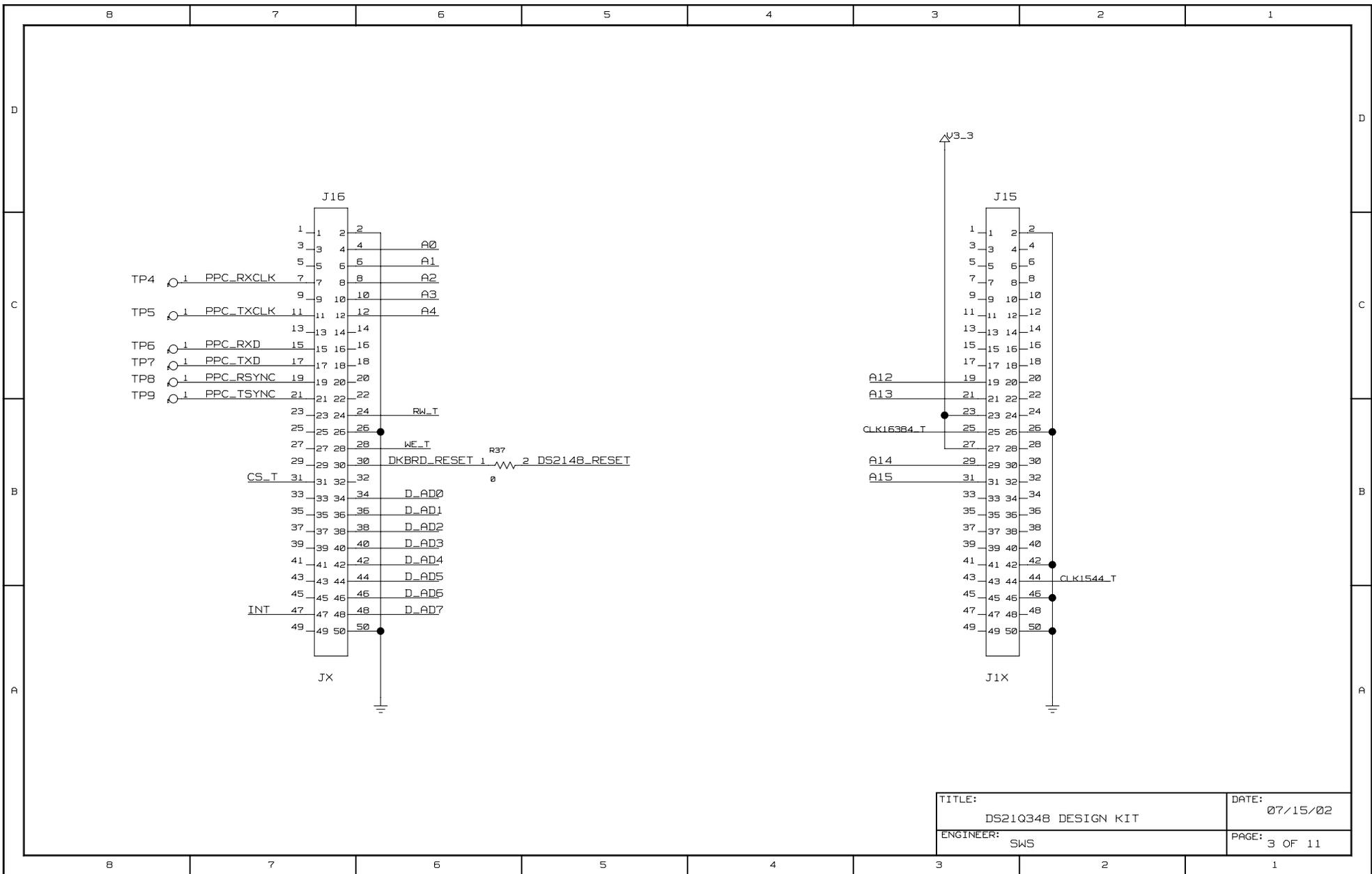
CS1	J3	CS<1>
CS2	D3	CS<2>
CS3	D10	CS<3>
CS4	K10	CS<4>
ALE	K2	ALE_AS
RD	J2	RD_DS
WR	H1	WR_R/W
D_AD0	D5	AD<0>
D_AD1	F3	AD<1>
D_AD2	D4	AD<2>
D_AD3	E3	AD<3>
D_AD4	J9	AD<4>
D_AD5	G11	AD<5>
D_AD6	H10	AD<6>
D_AD7	J10	AD<7>

DS21Q348
CONTROL

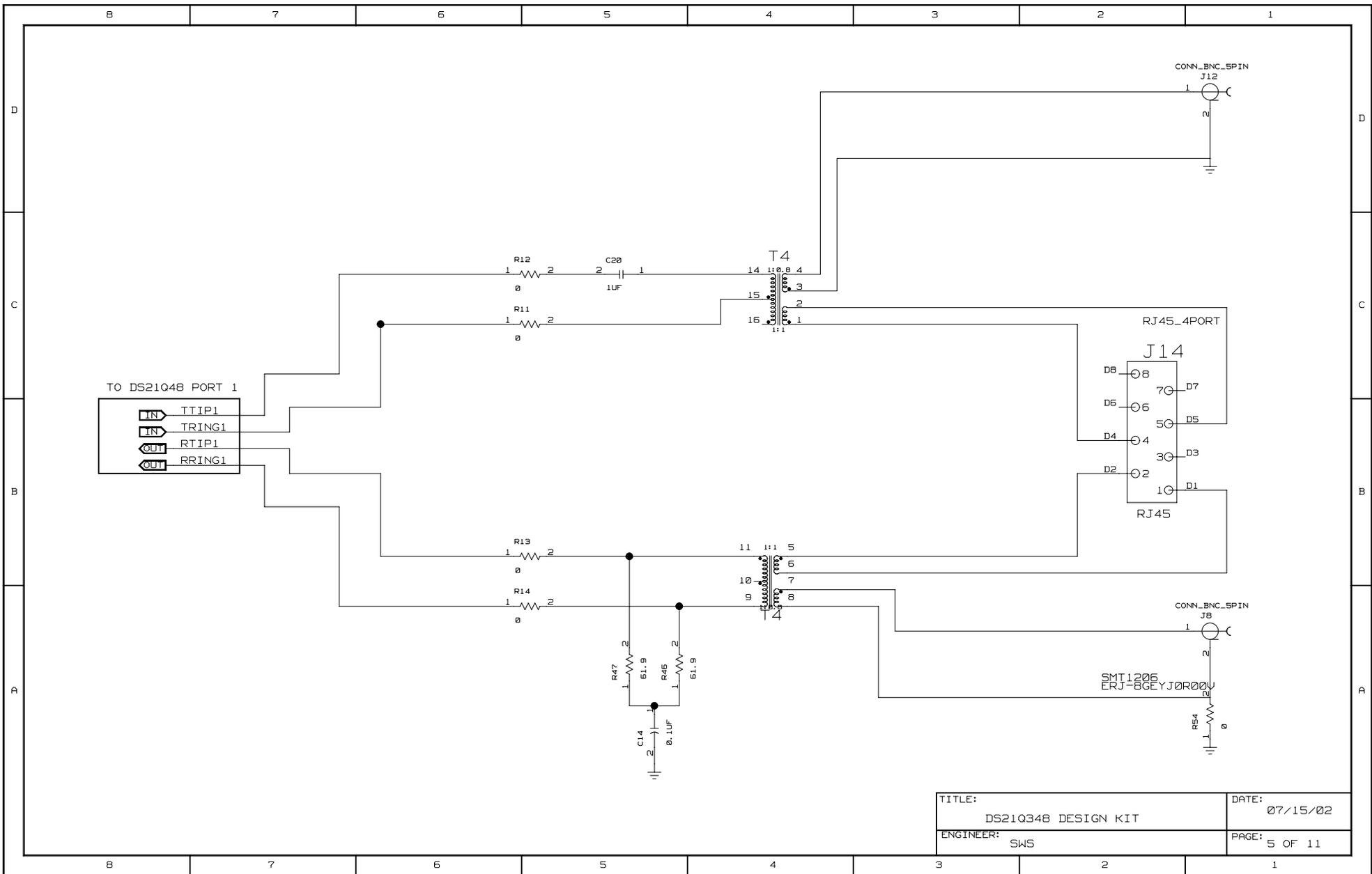
TEST	K7	TEST
MCLK	J6	MCLK
VSM	G4	VSM
HRST	L9	DS214B_RESET
BIS0	L7	BIS0
BIS1	M8	BIS1
PBTS	M12	PBTS
INT	K9	INT
A<0>	G12	A0
A<1>	H12	A1
A<2>	H11	A2
A<3>	L11	A3
A<4>	K11	A4



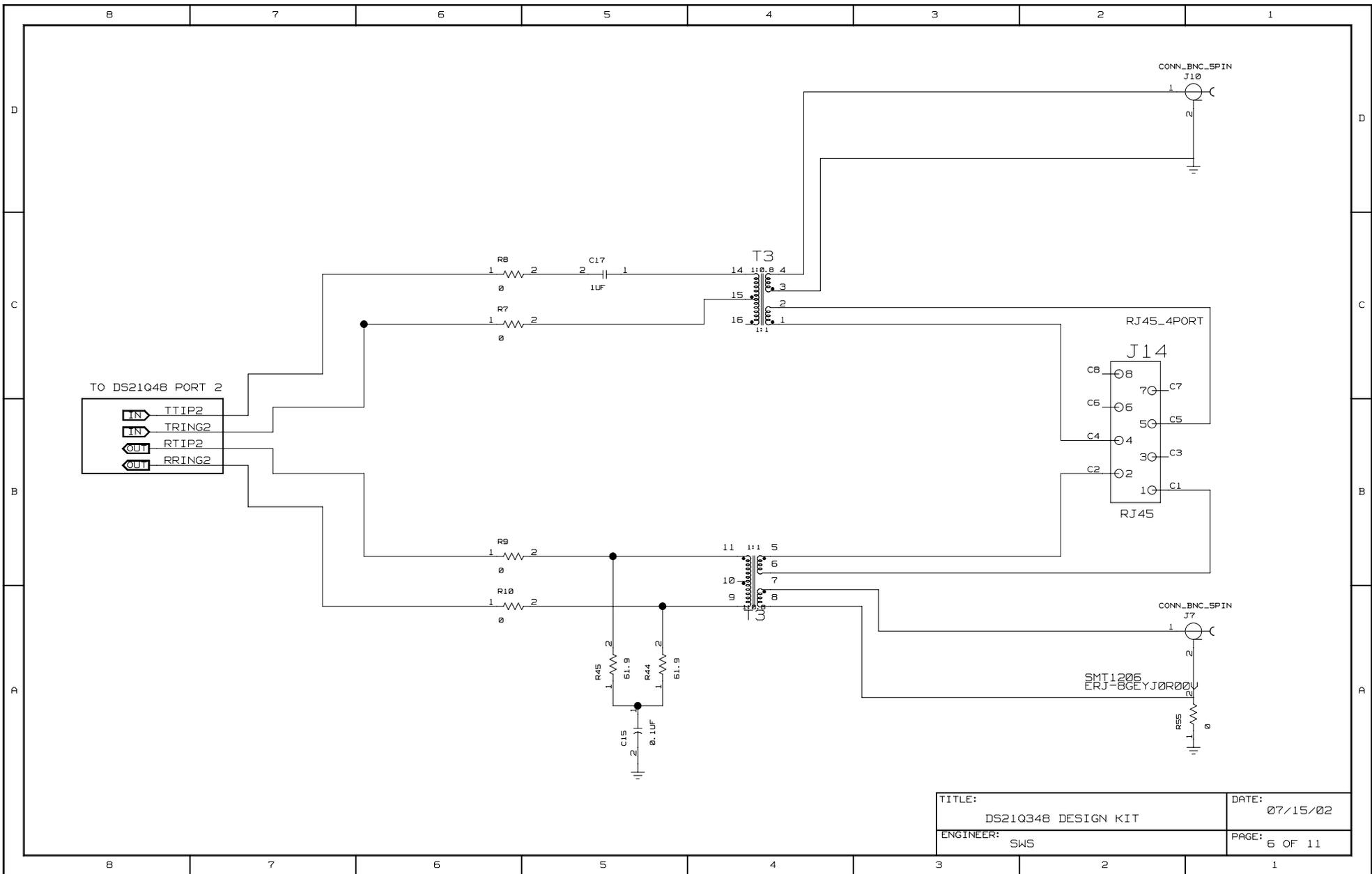
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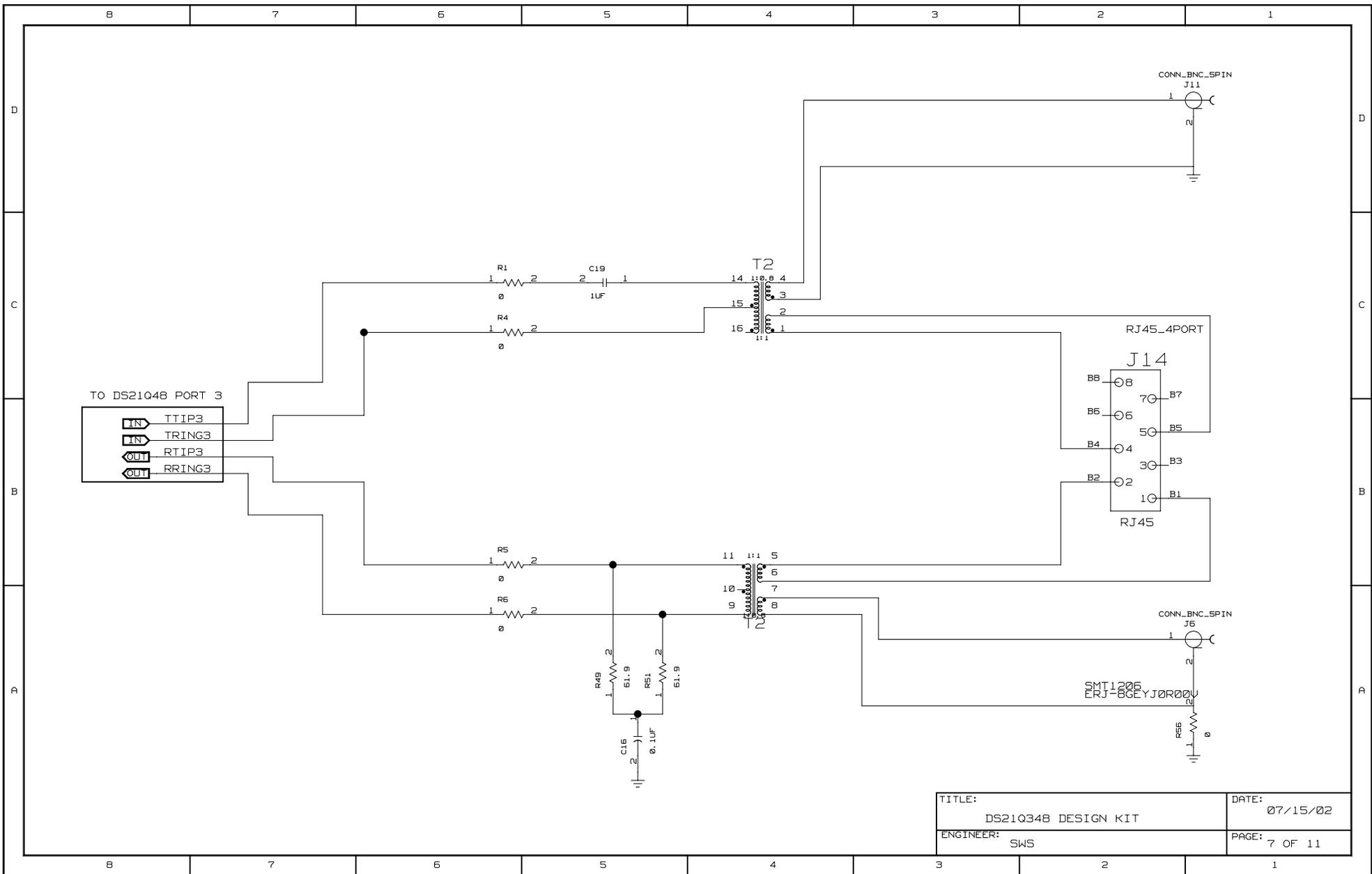
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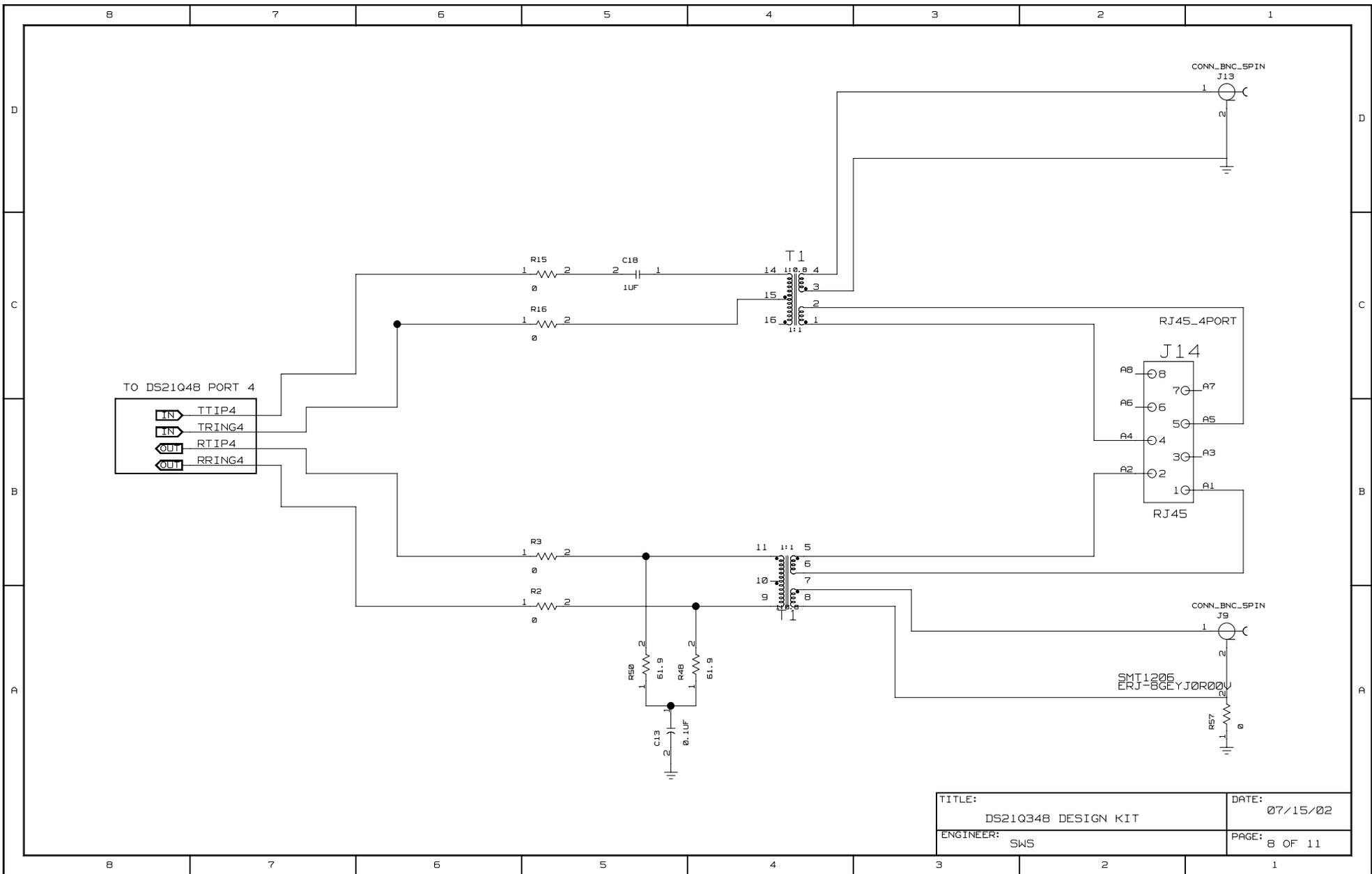
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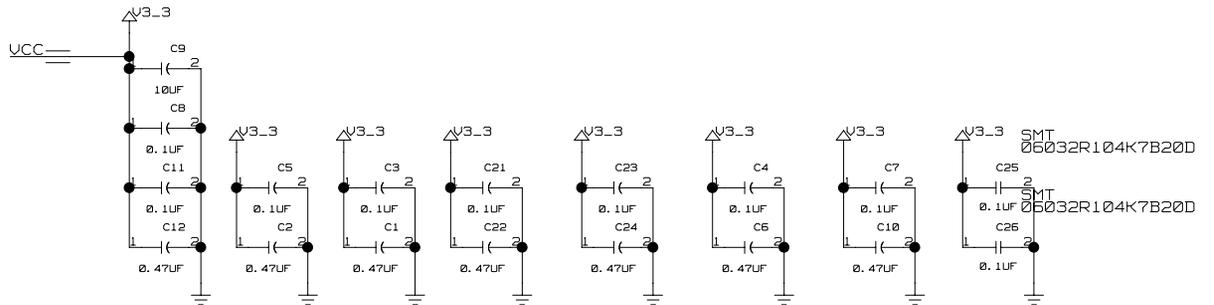
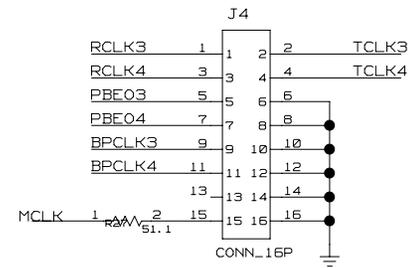
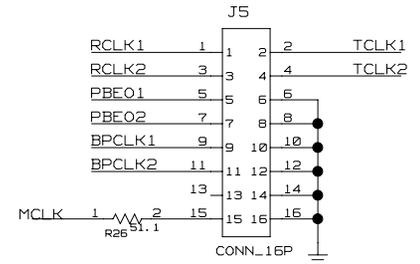
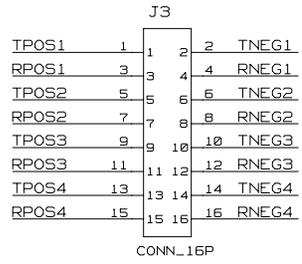
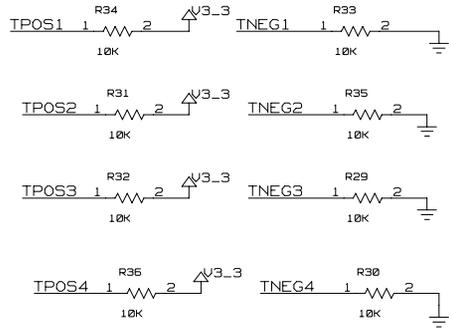
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D	<p>*** Signal Cross-Reference for the entire design ***</p> <pre> A0 3C6< 4C4< 2B4< A1 3C6< 4C4< 2B4< A2 3C6< 4C4< 2B4< A3 3C6< 4C4< 2B4< A4 2B4< 3C5< 4C4< A12 3C3< 4B4< A13 3B3< 4B4< A14 3B3< 4B4< A15 3B3< 4B4< ALE 2C8< 4A6< B1S0 2C4< 4A6< B1S1 2B4< 4A6< BPCLK1 2D4< 9C2< BPCLK2 2C4< 9C2< BPCLK3 2B4< 9B2< BPCLK4 2A4< 9B2< CLK1544_T 3B2< 4D3< CLK163B4_T 3B3< 4D4< CS1 4C4< 2C8< CS2 4C4< 2C8< CS3 4B4< 2C8< CS4 4B4< 2C8< CS_T 3B7< 4B1< DKBRD_RESET 3B6< 4B1< DS214B_RESET 2C4< 3B5< D_AD0 2B8< 3B6< 4C1< D_AD1 2B8< 3B6< 4C1< D_AD2 2B8< 3B6< 4C1< D_AD3 2B8< 3B6< 4C1< D_AD4 2B8< 3B6< 4C1< D_AD5 2B8< 3B6< 4C1< D_AD6 2B8< 3A6< 4C1< D_AD7 2B8< 3A6< 4C1< INT 2B4< 3A7< 4A2< 4A8< MCLK 4D3< 2C4< 9B3< 9C3< PBEO1 2D4< 9D2< PBEO2 2C4< 9C2< PBEO3 2B4< 9B2< PBEO4 2A4< 9B2< PBT5 2B4< 4A6< PPC_RSYNC 3C7< PPC_RXCLK 3C7< PPC_RXD 3C7< PPC_TSYNC 3B7< PPC_TXCLK 3C7< PPC_TXD 3C7< RCL1 2C2< 4B2< RCL2 2C2< 4B2< RCL3 2B2< 4B2< RCL4 2A2< 4A2< RCLK1 2D2< 9D2< RCLK2 2C2< 9D2< RCLK3 2B2< 9C2< RCLK4 2A2< 9C2< RD 4C4< 2C8< RNEG1 2D4< 9D4< RNEG2 2C4< 9C4< RNEG3 2B4< 9C4< RNEG4 2A4< 9C4< RPOS1 2D4< 9D5< RPOS2 2C4< 9C5< RPOS3 2B4< 9C5< RPOS4 2A4< 9C5< RRING1 5B8< 2D1< RRING2 6B8< 2C1< RRING3 7B8< 2B1< RRING4 8B8< 2A1< RTIP1 5B8< 2D1< RTIP2 6B8< 2C1< RTIP3 7B8< 2B1< RTIP4 8B8< 2A1< RW_T 3B6< 4B1< TCK 4B8< 4D8< TCLK1 4D3< 9D1< 2D2< TCLK2 4D3< 9D1< 2C2< </pre>		<pre> TCLK3 4D3< 9C1< 2B2< TCLK4 4D3< 9C1< 2A2< TDI 4B8< 4C8< TD0 4B8< 4C7< TEST 2C4< 4A6< TMS 4B8< 4C7< TNEG1 9D4< 2D4< 9D7< TNEG2 9D4< 2C4< 9C7< TNEG3 9C4< 2B4< 9C7< TNEG4 9C4< 2A4< 9C7< TPOS1 9D5< 2D4< 9DB< TPOS2 9D5< 2C4< 9CB< TPOS3 9C5< 2B4< 9CB< TPOS4 9C5< 2A4< 9CB< TRING1 2D1< 5B8< TRING2 2C1< 5B8< TRING3 2B1< 7B8< TRING4 2A1< 8B8< TTIP1 2D1< 5B8< TTIP2 2C1< 5B8< TTIP3 2B1< 7B8< TTIP4 2A1< 8B8< VSM 2C4< 4A6< WE_T 3B6< 4B1< WR 4C4< 2B8< </pre>													
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*** Part Cross-Reference for the entire design ***

1 DS21Q348 2A3 2B3 2B6 2C3 2D3
 C1 CAP 9A4
 C2 CAP 9A5
 C3 CAP 9A4
 C4 CAP 9A3
 C5 CAP 9A5
 C6 CAP 9A3
 C7 CAP 9A2
 C8 CAP 9A5
 C9 CAP 9B5
 C10 CAP 9A2
 C11 CAP 9A5
 C12 CAP 9A5
 C13 CAP 8A5
 C14 CAP 5A5
 C15 CAP 6A5
 C16 CAP 7A5
 C17 CAP 6C5
 C18 CAP 8C5
 C19 CAP 7C5
 C20 CAP 5C5
 C21 CAP 9A4
 C22 CAP 9A4
 C23 CAP 9A3
 C24 CAP 9A3
 C25 CAP 9A2
 C26 CAP 9A2
 DS1 LED 4A2
 DS2 LED 4A2
 DS3 LED 4A3
 DS4 LED 4A3
 DS5 LED 4A2
 J1 CONN_BNC_SPIN 4A4
 J2 CONN_10P 4C8
 J3 CONN_16P 9D4
 J4 CONN_16P 9C2
 J5 CONN_16P 9D2
 J6 CONN_BNC_SPIN 7A2
 J7 CONN_BNC_SPIN 6A2
 J8 CONN_BNC_SPIN 5A1
 J9 CONN_BNC_SPIN 8A1
 J10 CONN_BNC_SPIN 6D2
 J11 CONN_BNC_SPIN 7D2
 J12 CONN_BNC_SPIN 5D1
 J13 CONN_BNC_SPIN 8D1
 J14 RJ45_B 5C2 6C2 7C2 8C2
 J15 CONN_S0P2 3D3
 J16 CONN_S0P2 3D7
 R1 RES 7C6
 R2 RES 8A5
 R3 RES 8B5
 R4 RES 7C6
 R5 RES 7B6
 R6 RES 7A6
 R7 RES 6C6
 R8 RES 6C6
 R9 RES 6B6
 R10 RES 6A6
 R11 RES 5C6
 R12 RES 5C6
 R13 RES 5B6
 R14 RES 5A6
 R15 RES 8C5
 R16 RES 8C5
 R17 RES 4A8
 R18 RES 4A3
 R19 RES 4A3
 R20 RES 4D8
 R21 RES 4D8
 R22 RES 4A3
 R23 RES 4A3
 R24 RES 4A2
 R25 RES 4D8
 R26 RES 9C2
 R27 RES 9B2

R28 RES 4B8
 R29 RES 9C7
 R30 RES 9C6
 R31 RES 9D8
 R32 RES 9C8
 R33 RES 9D7
 R34 RES 9D8
 R35 RES 9D7
 R36 RES 9C7
 R37 RES 3B6
 R38 RES 4A6
 R39 RES 4A8
 R40 RES 4A8
 R41 RES 4A6
 R42 RES 4A6
 R43 RES 4A6
 R44 RES 6A5
 R45 RES 6A5
 R46 RES 5A5
 R47 RES 5A5
 R48 RES 8A5
 R49 RES 7A5
 R50 RES 8A5
 R51 RES 7A5
 R53 RES 4A4
 R54 RES 5A1
 R55 RES 6A2
 R56 RES 7A2
 R57 RES 9A1
 T1 XFMR_2IN_4OUT 8A4 8C4
 T2 XFMR_2IN_4OUT 7A4 7C4
 T3 XFMR_2IN_4OUT 6A4 6C4
 T4 XFMR_2IN_4OUT 5A4 5C4
 TP1 TSTPNT_SNG 4D2
 TP2 TSTPNT_SNG 4D2
 TP3 TSTPNT_SNG 4D2
 TP4 TSTPNT_SNG 3C8
 TP5 TSTPNT_SNG 3C8
 TP6 TSTPNT_SNG 3C8
 TP7 TSTPNT_SNG 3C8
 TP8 TSTPNT_SNG 3C8
 TP9 TSTPNT_SNG 3B8
 U1 XILINX_XC9572XL 4D4 4D7

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