

# Set-top Box Clock Generator with VCXO

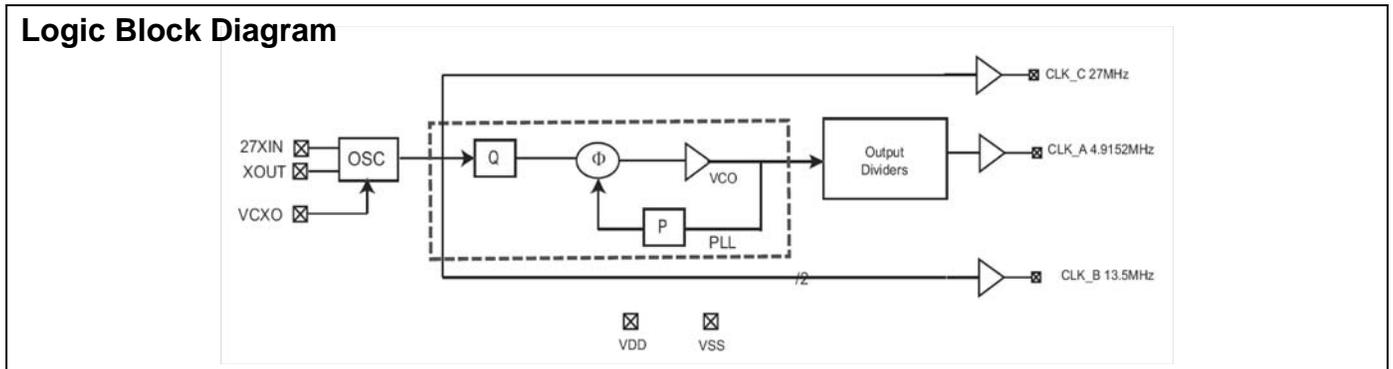
## Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V Operation
- 8-pin SOIC

## Benefits

- High-performance PLL tailored for Set Top Box applications
- Meets critical timing requirements in complex system designs
- Large  $\pm 150$ -ppm range, better linearity
- Meet industry standard voltage platforms
- Industry standard packaging saves on board space

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24713	3	27-MHz pullable crystal input per Cypress specification	4.9152 MHz, 13.5 MHz, 27 MHz



## Pin Configuration

Figure 1. CY24713, 8-Pin SOIC

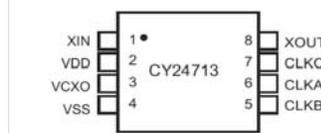


Table 1. Pin Definition

Name	Number	Description
XIN	1	Reference Crystal Input
VDD	2	3.3V Voltage Supply
VCXO	3	Input Analog Control for VCXO
VSS	4	Ground
CLK_B	5	13.5-MHz Clock Output
CLK_A	6	4.9152-MHz Clock Output
CLK_C	7	27-MHz Clock Output
XOUT <sup>[1]</sup>	8	Reference Crystal Output

### Note

1. Float X<sub>OUT</sub> if X<sub>IN</sub> is externally driven.

## Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
T <sub>S</sub>	Storage Temperature <sup>[2]</sup>	-65	125	°C
T <sub>J</sub>	Junction Temperature	-	125	°C
	Digital Inputs	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Digital Outputs referred to V <sub>DD</sub>	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Electrostatic Discharge	-	2000	V
	Analog Input	-0.5	7.0	V

## Pullable Crystal Specifications

Parameter	Description	Condition	Min	Typ.	Max	Unit
F <sub>NOM</sub>	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	-	27	-	MHz
C <sub>LNOM</sub>	Nominal load capacitance		-	14	-	pF
R <sub>1</sub>	Equivalent series resistance (ESR)	Fundamental mode	-	-	25	Ω
R <sub>3</sub> /R <sub>1</sub>	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R <sub>1</sub> values are much less than the maximum spec.	3	-	-	
DL	Crystal drive level	No external series resistor assumed	-	0.5	2.0	mW
F <sub>3SEPHI</sub>	Third overtone separation from 3*F <sub>NOM</sub>	High side	300	-	-	ppm
F <sub>3SEPLO</sub>	Third overtone separation from 3*F <sub>NOM</sub>	Low side	-	-	-150	ppm
C <sub>0</sub>	Crystal shunt capacitance		-	-	7	pF
C <sub>0</sub> /C <sub>1</sub>	Ratio of shunt to motional capacitance		180	-	250	
C <sub>1</sub>	Crystal motional capacitance		14.4	18	21.6	pF

## Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V <sub>DD</sub>	Operating Voltage	3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Temperature	0	-	70	°C
C <sub>LOAD</sub>	Max. Load Capacitance	-	-	15	pF
t <sub>PU</sub>	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	-	500	ms

## DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> = 3.3V	12	24	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V	12	24	-	mA
C <sub>IN</sub>	Input Capacitance		-	-	7	pF
I <sub>Iz</sub>	Input Leakage Current		-	5	-	μA
f <sub>ΔXO</sub>	VCXO pullability range		±150	-	-	ppm
V <sub>VCXO</sub>	VCXO input range		0	-	V <sub>DD</sub>	V
I <sub>VDD</sub>	Supply Current		-	25	30	mA

**Note**

2. Rated for 10 years

**AC Electrical Characteristics** ( $V_{DD} = 3.3V$ )

Parameter <sup>[3]</sup>	Description	Conditions	Min	Typ.	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <a href="#">Figure 3</a> 50% of $V_{DD}$	45	50	55	%
$ER_0$	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$ , $C_{LOAD} = 15\text{ pF}$ <a href="#">Figure 4</a> .	0.8	1.4	–	V/ns
$EF_1$	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$ , $C_{LOAD} = 15\text{ pF}$ <a href="#">Figure 4</a> .	0.8	1.4	–	V/ns
$t_9$	Clock Jitter	Peak-Peak period jitter maximum absolute jitter	–	200	250	ps
$t_{10}$	PLL Lock Time		–	–	3	ms

Figure 2. Test Circuit

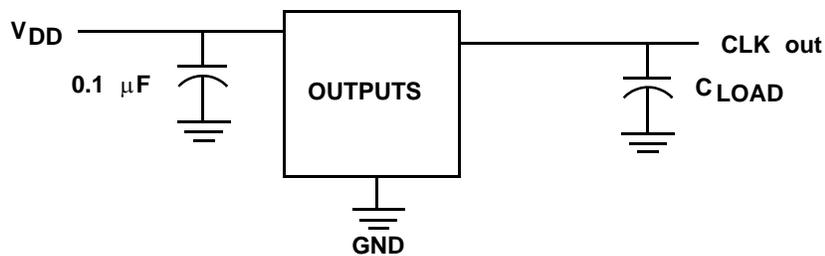


Figure 3. Duty Cycle Definition;  $DC = t_2/t_1$

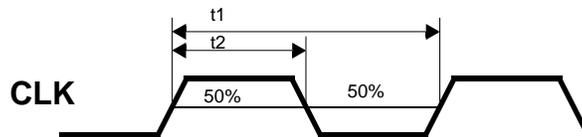
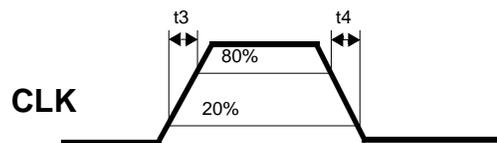


Figure 4. Rise and Fall Time Definitions:  $ER = 0.6 \times V_{DD}/t_3$ ,  $EF = 0.6 \times V_{DD}/t_4$



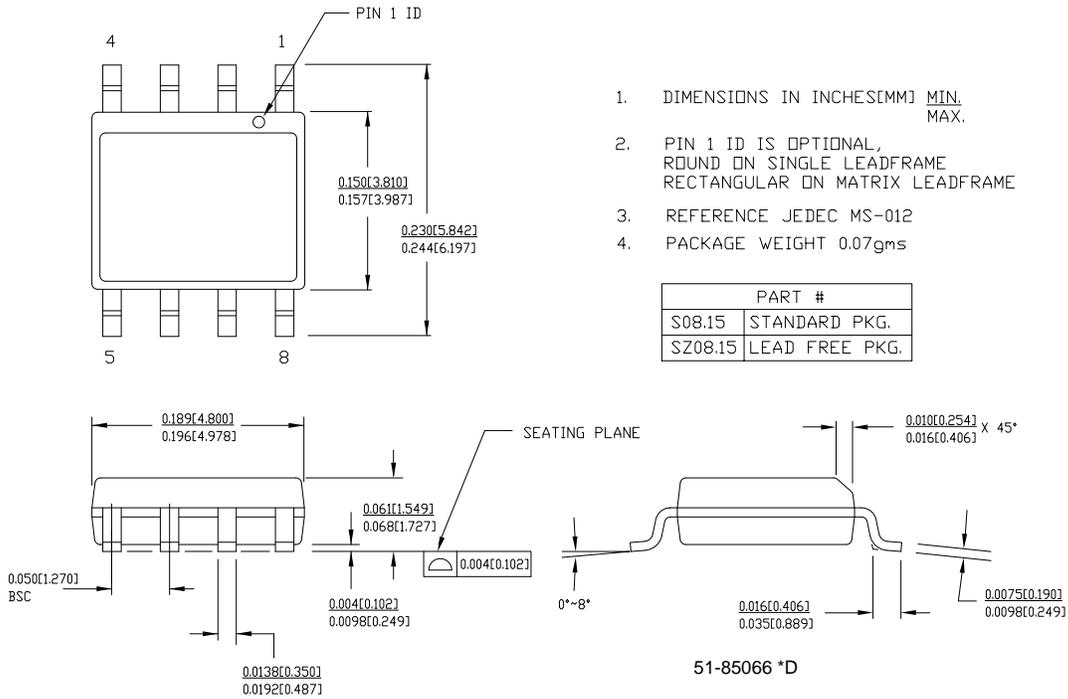
**Note**  
3. Not 100% tested

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
<b>Pb-free</b>			
CY24713KSXC	8-pin SOIC	Commercial	3.3V
CY24713KSXCT	8-pin SOIC-Tape and Reel	Commercial	3.3V

Package Diagram

Figure 5. 8-Pin (150-Mil) SOIC S8



## Document History Page

Document Title: CY24713 Set-top Box Clock Generator with VCXO Document Number: 38-07396				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	333175	RGL	See ECN	New Data Sheet
*A	2440886	AESA	See ECN	Updated template. Added Note "Not recommended for new designs." Added part number CY24713KSXC, and CY24713KSXCT in ordering information table. Replaced Lead-Free with Pb-Free.
*B	2899683	CXQ	03/26/10	Removed inactive parts from ordering information table Updated package diagram

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