3.5V to 11V, Integrated 2.5A MOSFET 1ch Boost Converter

BD8311NUV

General Description

BD8311NUV is a high-efficiency step-up switching regulator with built-in power MOSFET that can output 8V or 10V from a 4-battery voltage supply such as Li2cell or a 5V fixed power supply line. The built-in 80mΩ N-Channel FET switch is capable of handling output current up to 2.5A. This IC has a flexible phase compensation system and a switching frequency of 1.2MHz allowing the use of smaller external output inductor and capacitor making the construction of a compact power supply really easy.

Features

- Built-In 2.5A/14V N-Channel FET Switch
- On-Chip Phase Compensation Between Input and Output of ERROR AMP.
- Output Current:
  - 600mA at 10V (3.5V to 10V input)
  - 800mA at 8V (3.5V to 8V input)
- Built-In Soft-Start Function.
- Built-In Timer Latch System for Short Circuit Protection Function.

Application

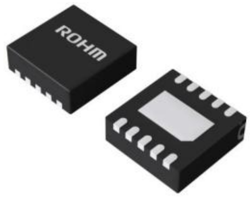
General Portable Equipment like DSC/DVC Powered by 4 dry Batteries or Li2cell

Key Specification

- Input Voltage Range: +3.5V to +11.0V
- Output Voltage Range: +4.0V to +11.0V
- FET Maximum Current: 2.5A
- Switching Frequency: 1.2MHz(Typ)
- Nch FET ON-Resistance: 80mΩ(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -25°C to +85°C

Package

W (Typ) x D (Typ) x H (Max)



VSON010V3030
3.00mm x 3.00mm x 1.00mm

Typical Application Circuit

Input: 3.5V to 10V, Output: 10V / 500 mA

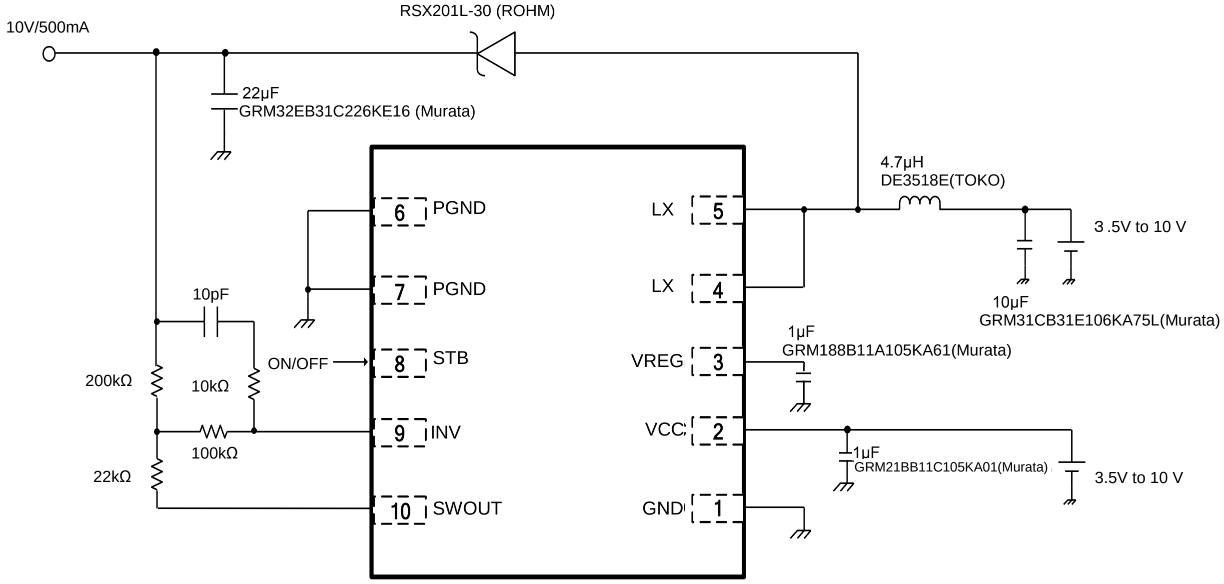


Figure 1. Typical Application Circuit

○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

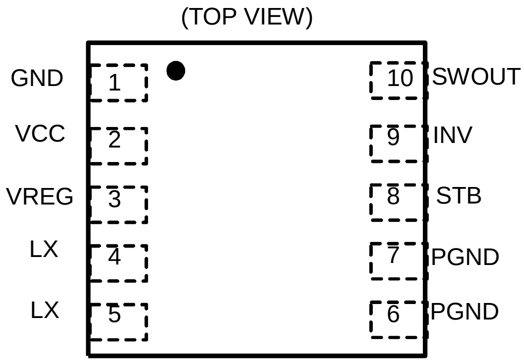


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	GND	Ground pin
2	VCC	Supply voltage input pin
3	VREG	5V output terminal of regulator for internal circuit
4 , 5	LX	Power switch terminal for coil
6 , 7	PGND	Power transistor ground pin
8	STB	ON/OFF terminal
9	INV	ERROR AMP input pin
10	SWOUT	STBSW for split resistance

Block Diagram

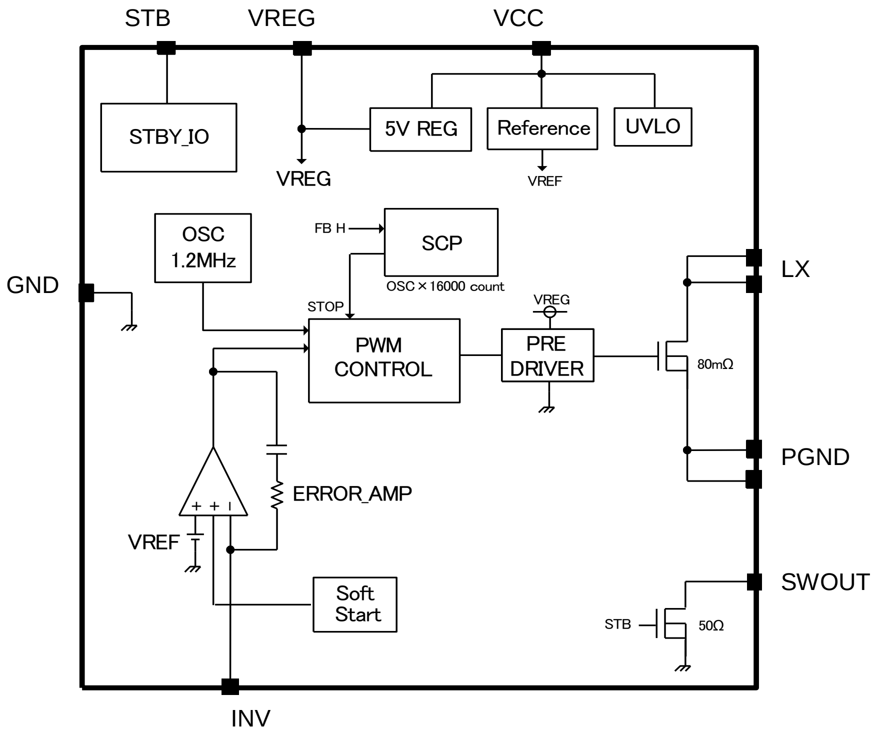


Figure 3. Block Diagram

Description of Blocks

1. VREF
   This block generates the 1.0V internal reference voltage of the ERROR AMP.

2. UVLO
   This circuit prevents low voltage malfunction of the internal circuit during activation of the power supply voltage or during low power supply voltage. It monitors the VREG pin voltage, turns OFF all output FET and DC/DC converter output, and resets the timer latch of the internal SCP circuit and soft-start circuit when VREG voltage becomes lower than 2.9V. Typical UVLO hysteresis is 200 mV.

3. SCP
   SCP is a timer latch system for short circuit protection. When the INV pin is set at 1.0V or lower, the internal SCP circuit starts counting. The internal counter is in-sync with OSC so that the latch circuit activates after a lapse of 13.3msec or after the counter counts about 16000 oscillations, and then the DC/DC converter output is Turned OFF. To reset the latch circuit, turn OFF the STB pin once. Then, turn it ON again or turn ON the power supply voltage again.

4. OSC
   Circuit that generates oscillating saw-tooth waveform signal with a fixed frequency of 1.2 MHz.

5. ERROR AMP
   The Error amplifier detects the output signal and outputs PWM control signals. The internal reference voltage is set at 1.0 V. A primary phase compensation device of 200 pF, 62 kΩ is built-in between the inverting input terminal and the output terminal of this ERROR AMP.

6. PWM COMP
   PWM COMP is the voltage-to-pulse-width converter for controlling the output voltage corresponding to the input voltage. It compares the internal SLOPE waveform with the ERROR AMP output voltage, then controls the pulse width of the output to the driver. Maximum duty is set at 85%.

7. Soft Start
   This circuit prevents inrush current during startup by gradually increasing the output voltage of the DC/DC. Soft-Start time is in-sync with the internal OSC so that the output voltage of the DC/DC converter reaches the set voltage after about 10000 oscillations.

8. PRE DRIVER
   CMOS inverter circuit for driving the built-in N-Channel FET.

9. STBY_IO
   Voltage applied on STB pin (8 pin) controls the ON/OFF state of the IC. The IC is Turned ON when a voltage of 2.5 V or higher is applied and Turned OFF when the terminal is open or when 0V is applied. A pull-down resistor (approximately 400 kΩ) is built-in.

10. Nch FET SW
    This is an internal FET switch that powers the output through the coil of the DC/DC converter. It is an 80 mΩ Nch FET SW that is capable of withstanding up to 14V across. Since the current rating of this FET is 2.5 A, it should be used within 2.5 A including the DC current and ripple current of the coil.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Maximum Applied Power Voltage	V_{CC}, V_{LX}	14	V
Maximum Input Voltage	V_{SWOUT}, V_{INV}	14	V
Maximum Input Current	I_{INMAX}	2.5	A
Power Dissipation	Pd	0.70 (Note 1)	W
Operating Temperature Range	Topr	-25 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 1) When used at Ta = 25°C or more installed on a 74.2 x 74.2 x 1.6^{t}mm board, the rating is reduced by 5.6 mW/°C.
(Note) These specifications are subject to change without advance notice for modifications and other reasons.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	3.5 to 11	V
Output Voltage	V_{OUT}	4.0 to 11	V

Electrical Characteristics

Parameter		Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
[Under Voltage Lock Out (UVLO)]							
Detection Threshold Voltage		V_{UV}	-	2.9	3.2	V	VREG Monitor
Hysteresis Range		ΔV_{UVHY}	100	200	300	mV	
[Oscillator]							
Oscillation Frequency		f_{OSC}	1.1	1.2	1.3	MHz	
[Regulator]							
Output Voltage		V_{REG}	4.65	5.0	5.35	V	
[ERROR AMP]							
INV Threshold Voltage		V_{INV}	0.99	1.00	1.01	V	
Input Bias Current		I_{INV}	-50	0	+50	nA	V_{CC}=11.0V , V_{INV}=5.5V
Soft-Start Time		t_{SS}	5.3	8.8	12.2	msec	
[PWM Comparator]							
LX Maximum Duty		D_{MAX1}	77	85	93	%	
[SWOUT]							
ON-Resistance		$R_{ONSWOUT}$	-	50	100	Ω	
[Output]							
LX NMOS ON-Resistance		R_{ON}	-	80	150	mΩ	
LX Leak Current		I_{LEAK}	-1	0	+1	µA	
[STB]							
STB Pin Control Voltage	Operation	V_{STBH}	2.5	-	V_{CC}	V	
	No-Operation	V_{STBL}	-0.3	-	+0.3	V	
STB Pin Pull-Down Resistance		R_{STB}	250	400	700	kΩ	
[Circuit Current]							
Standby Current VCC		I_{STB}	-	-	1	µA	
Circuit Current at Operation VCC		I_{CC}	-	600	900	µA	V_{INV}=1.2V

Typical Performance Curves

(Unless otherwise specified, Ta = 25°C, V_{CC} = 7.4V)

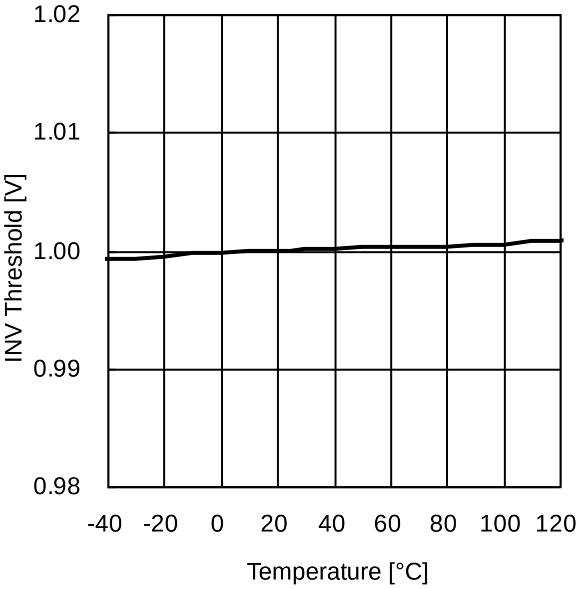


Figure 4. INV Threshold vs Temperature

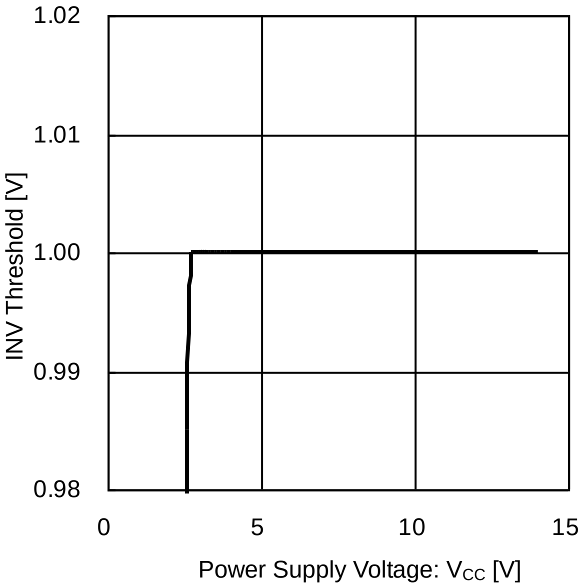


Figure 5. INV Threshold vs V_{CC}

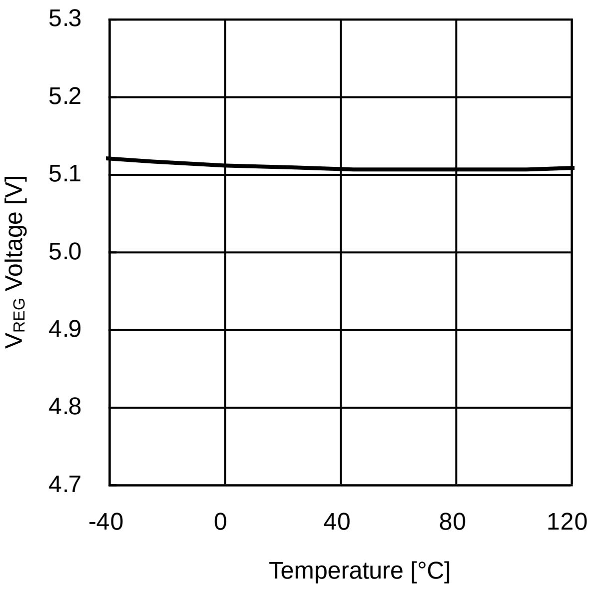


Figure 6. V_{REG} Voltage vs Temperature

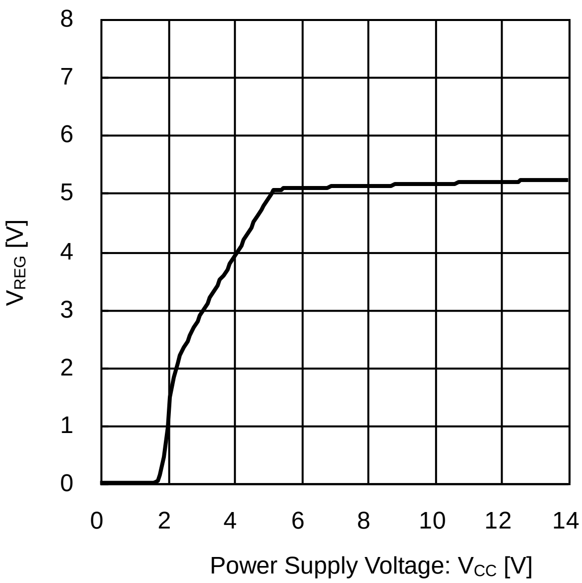
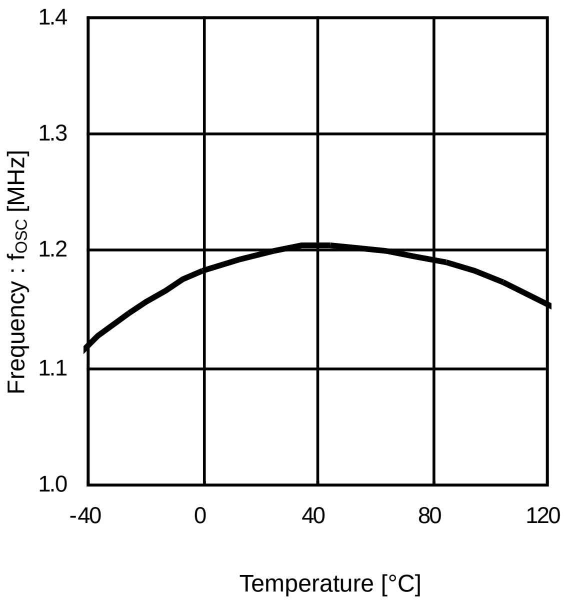


Figure 7. V_{REG} vs Power Supply voltage

Typical Performance Curves - continued



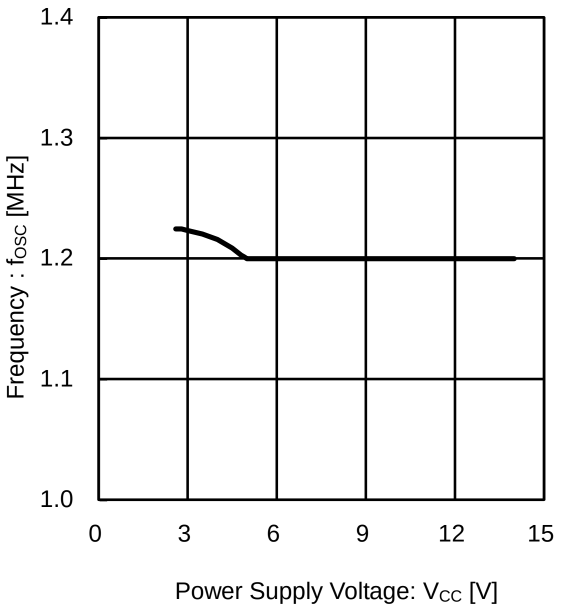


Figure 9. Frequency vs V_{CC}

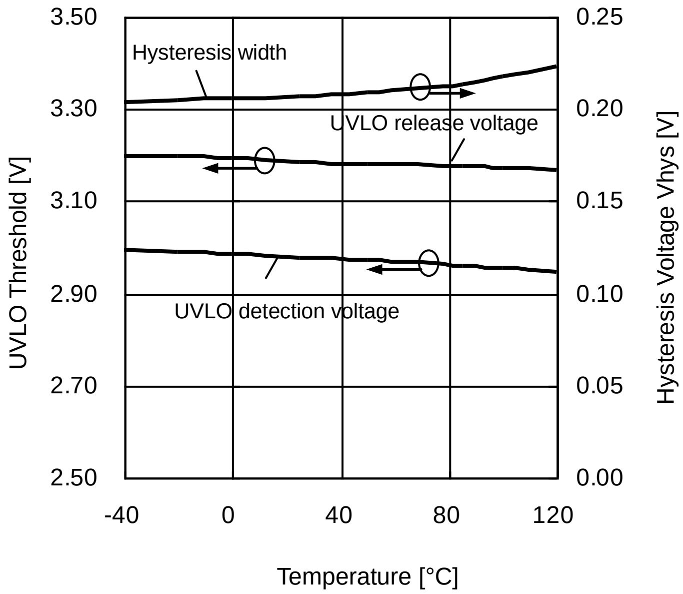


Figure 10. UVLO Threshold vs Environmental Temperature

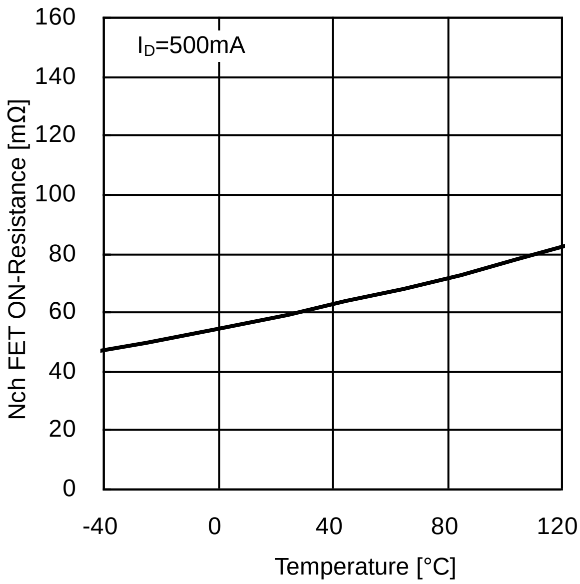


Figure 11. ON-Resistance vs Temperature

Typical Performance Curves - continued

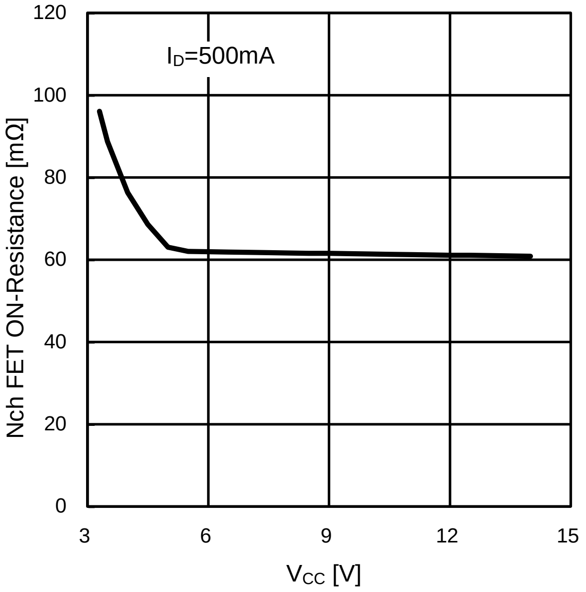


Figure 12. Nch FET ON-Resistance vs V_{CC}

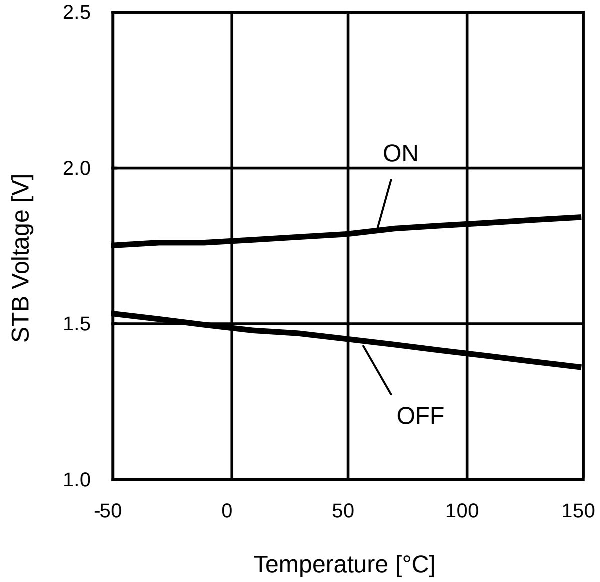


Figure 13. STB Voltage vs Temperature

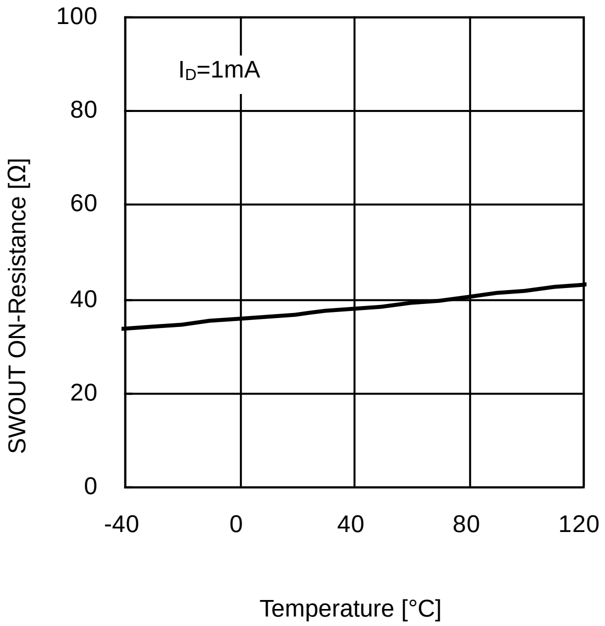


Figure 14. SWOUT ON-Resistance vs Temperature

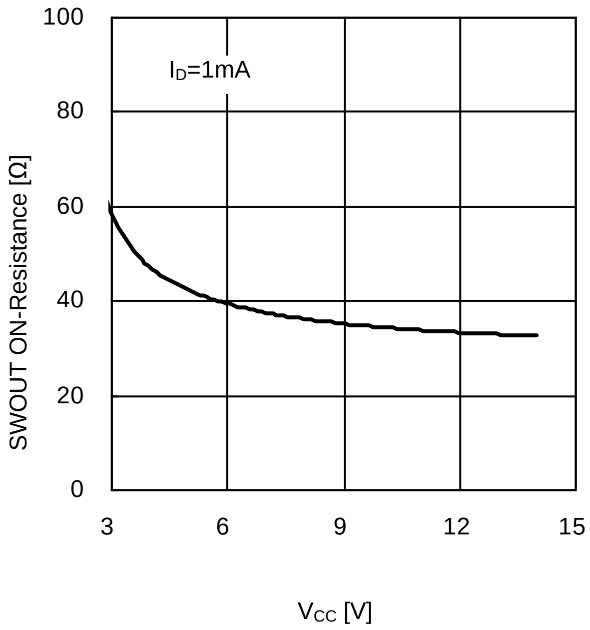


Figure 15. SWOUT ON-Resistance vs V_{CC}

Typical Performance Curves - continued

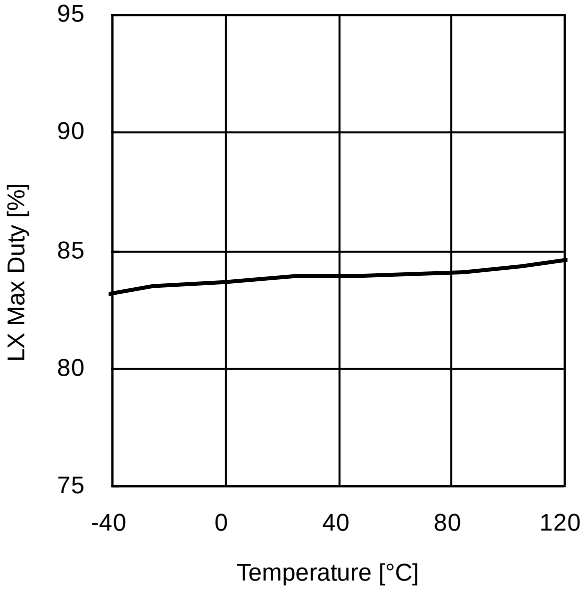


Figure 16. LX Max Duty vs Temperature

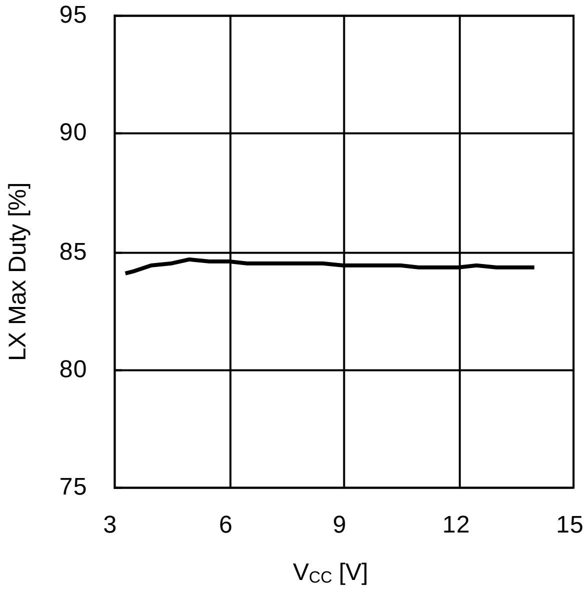


Figure 17. LX Max Duty vs V_{CC}

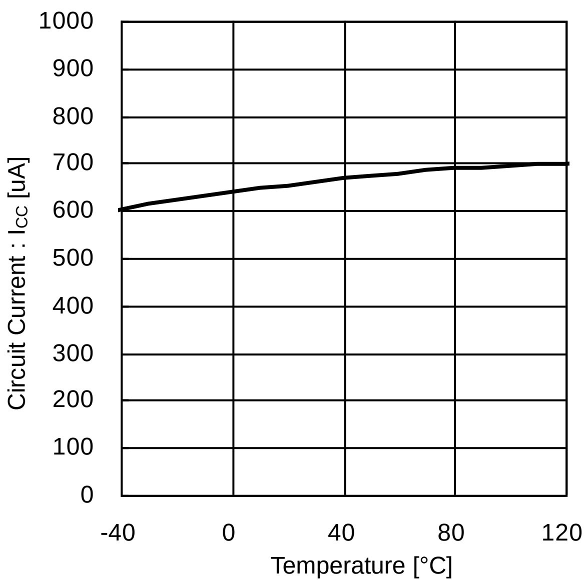


Figure 18. ICC vs Temperature

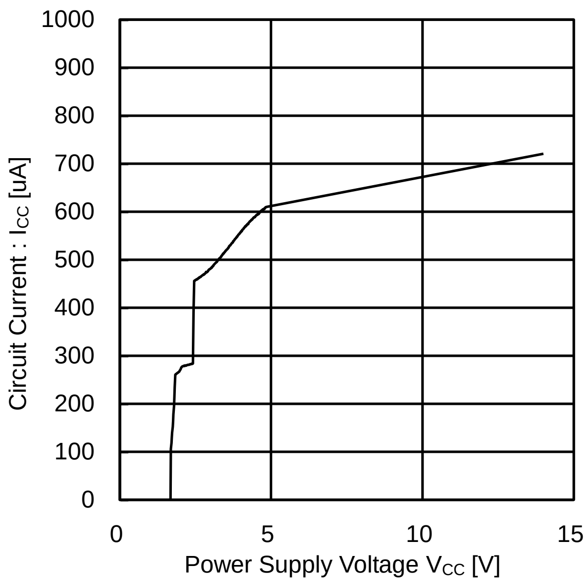


Figure 19. I_{CC} vs V_{CC}

Application Information

1. Example of Application Input: 3.5V to 10V, Output: 10V / 500mA

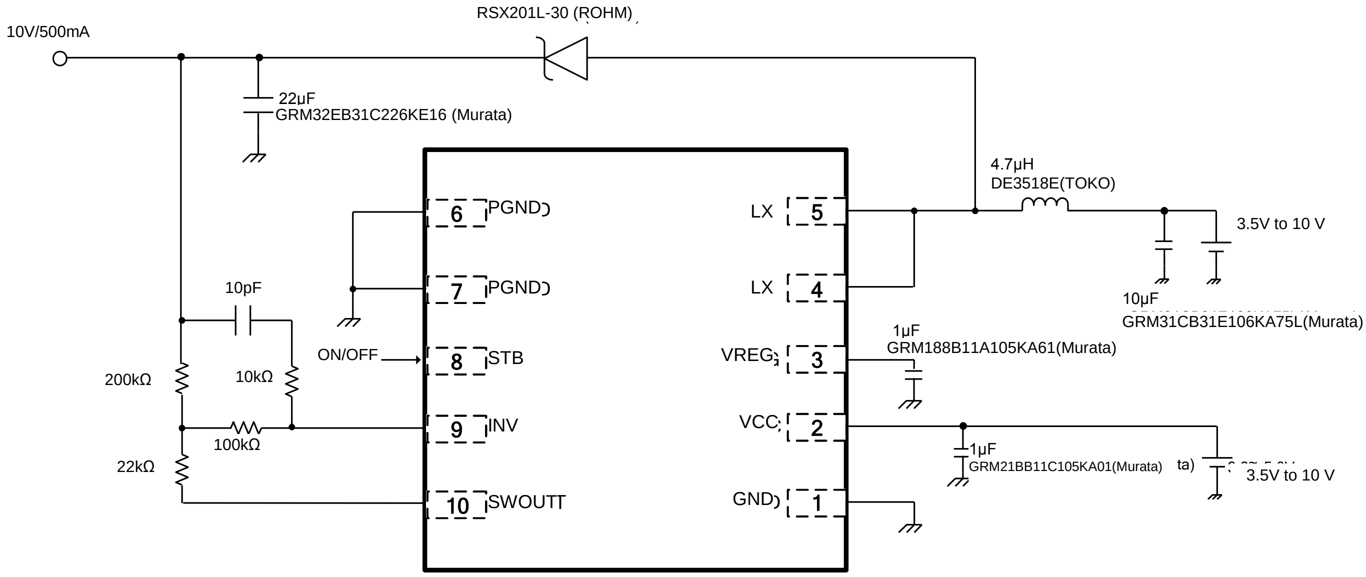


Figure 20. Reference Application Diagram

2. Reference Application Data 1

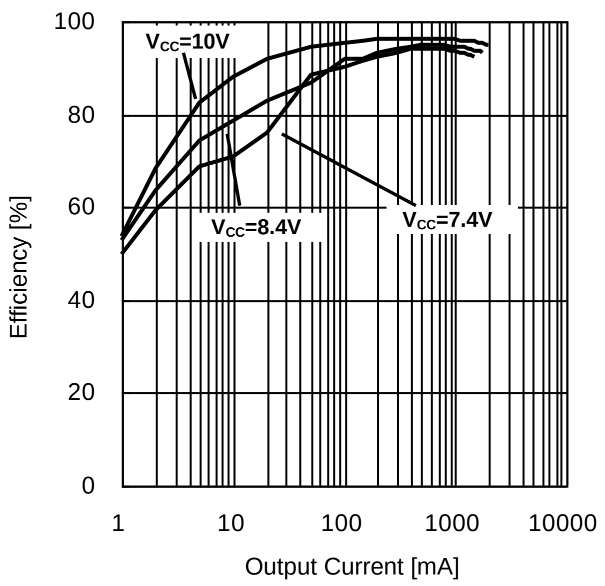


Figure 21. Power Conversion Efficiency 1

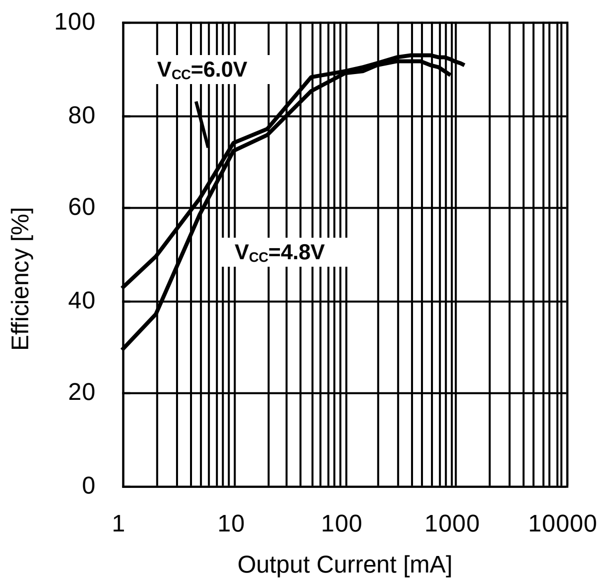


Figure 22. Power Conversion Efficiency 2

Reference Application Data 1 - continued

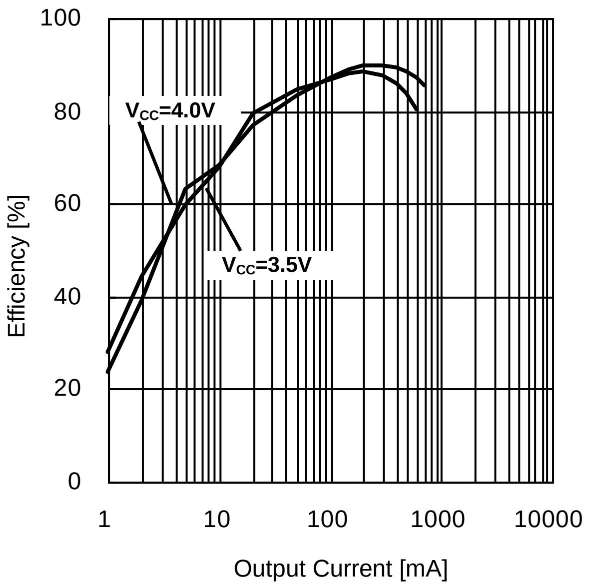


Figure 23. Power Conversion Efficiency3

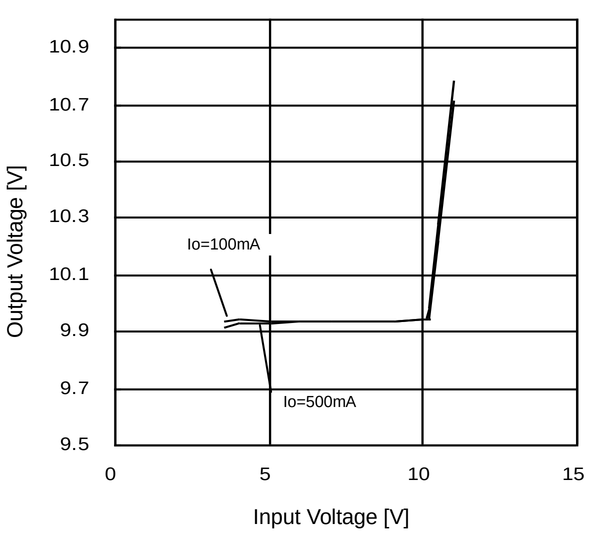
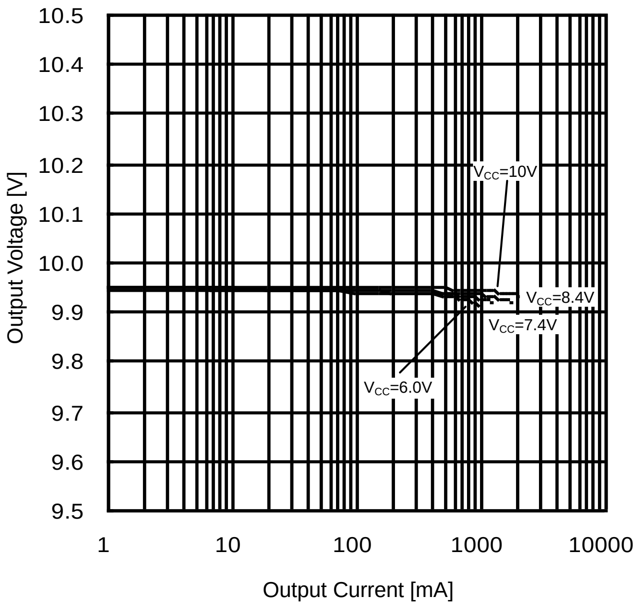
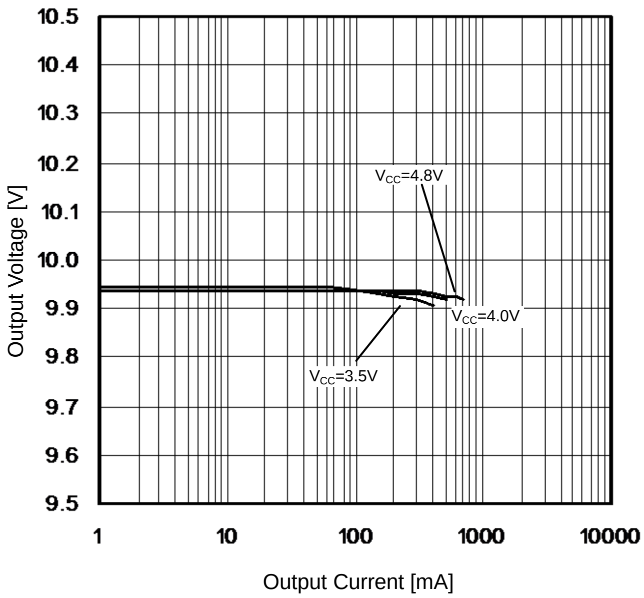


Figure 24. Line Regulation





3. Reference Application Data1 - continued

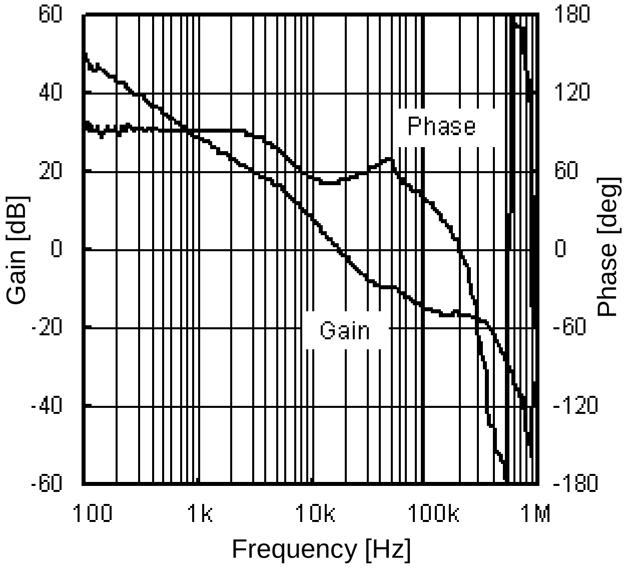


Figure 27. Frequency Response Property 1
(V_{CC} = 3.5V, I_O = 200mA)

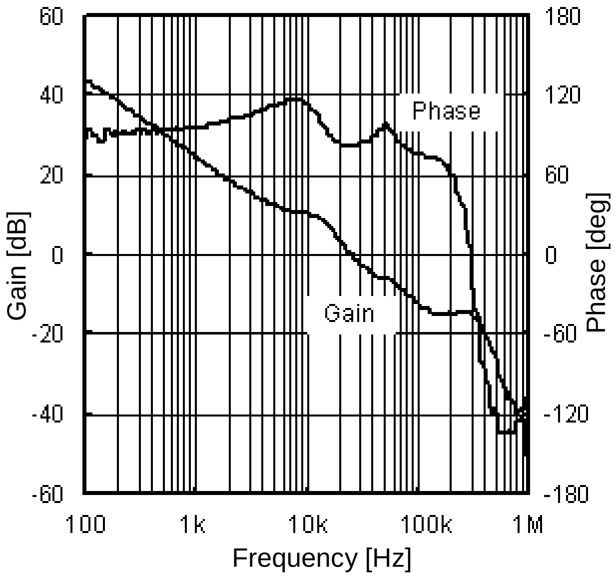


Figure 28. Frequency Response Property 2
(V_{CC} = 6.0V, I_O = 200mA)

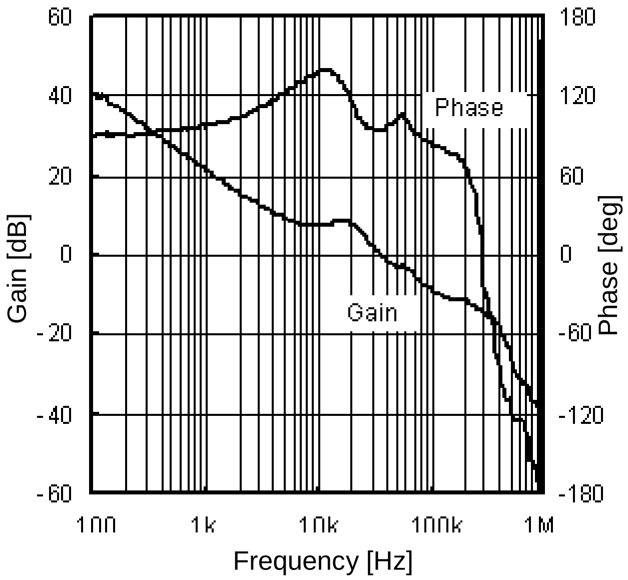


Figure 29. Frequency Response Property 3
(V_{CC} = 8.4 V, I_O = 200mA)

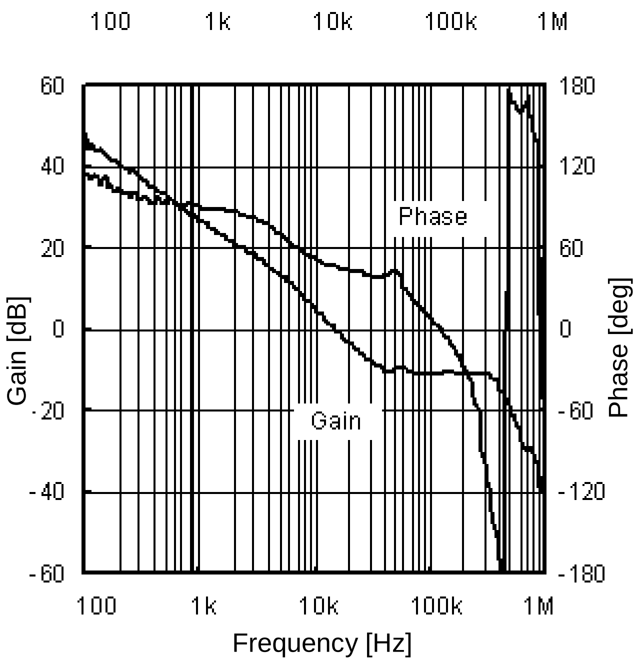


Figure 30. Frequency Response Property 4
(V_{CC} = 3.5 V, I_O = 500mA)

Reference Application Data 1 - continued

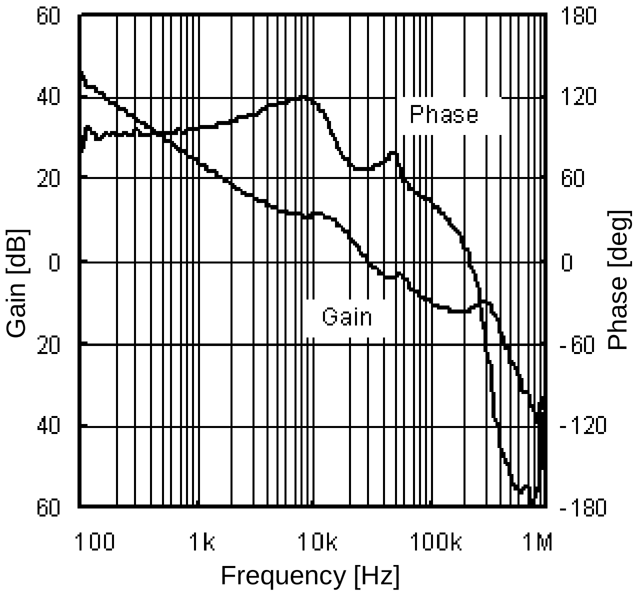


Figure 31. Frequency Response Property 5
(V_{CC} = 6.0 V, I_O = 500mA)

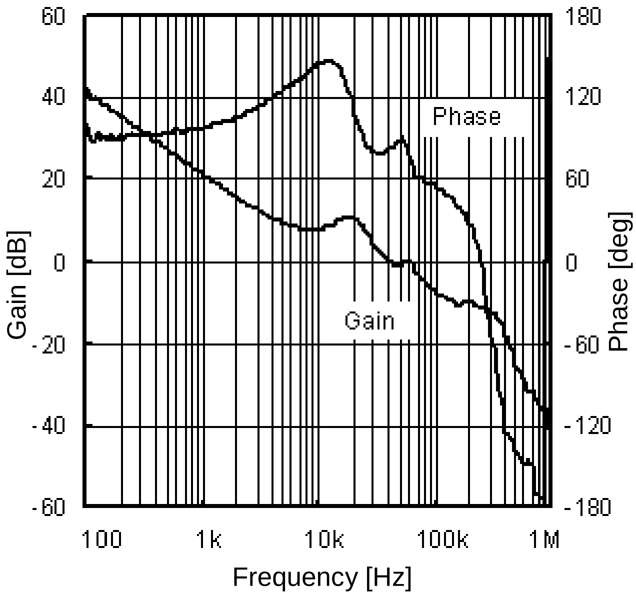
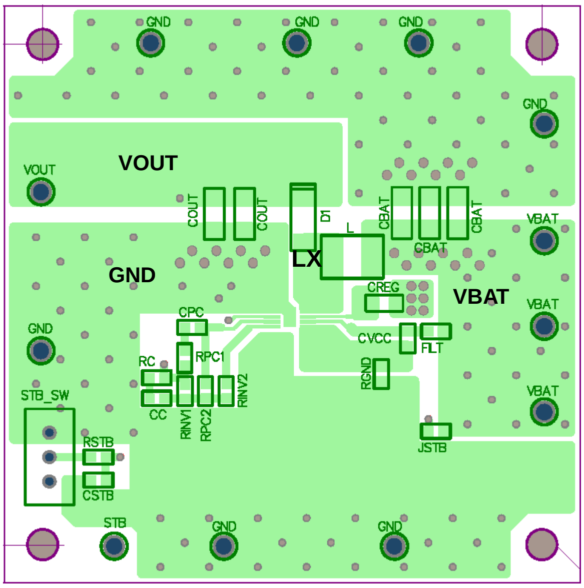


Figure 32. Frequency Response Property 6
(V_{CC} = 8.4 V, I_O = 500mA)

●Reference Board Pattern



The heat sink on the rear should be a GND trace of low impedance and at the same potential with the PGND trace.
It is recommended to install a GND pin not directly connected to the PGND, as shown in the picture above.

●Selection of Part for Applications

(1) Inductor

A shielded inductor with low DCR (direct resistance component) that satisfies the current rating (current value, Ipeak as shown in the equation below) is recommended.
Inductor values affect inductor ripple current, which causes output ripple.
Ripple current can be reduced as the coil L value becomes larger and the switching frequency becomes higher.

$$I_{peak} = I_{OUT} \times (V_{OUT}/V_{IN})/\eta + \Delta I_L/2 \quad [A] \quad (1)$$

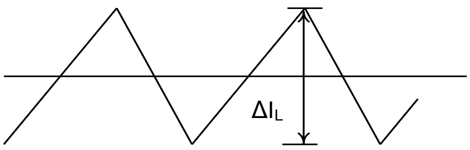


Figure 33. Inductor Current

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{1}{f} \quad [A] \quad (2)$$

where:
η is the Efficiency,
ΔI_L is the Output ripple current
f is the Switching frequency

As a guide, inductor ripple current should be set at about 20% to 50% of the maximum input current.

Note: Inductor current exceeding its current rating will bring the coil into magnetic saturation, which may lead to lower efficiency or output oscillation. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the coil.

(2) Output Capacitor

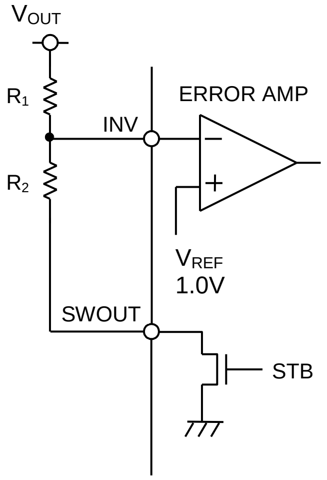
A ceramic capacitor with low ESR is recommended for the output in order to reduce output ripple. There must be an adequate margin between the maximum rating and output voltage of the capacitor, taking the DC bias property into consideration.
Output ripple voltage is obtained by the following equation:

$$V_{PP} = I_{OUT} \times \frac{V_{OUT} - V_{IN}}{f \times C_O \times V_{OUT}} + I_{OUT} \times R_{ESR} \quad [V] \quad (3)$$

Setting must be performed so that output ripple is within the allowable ripple voltage.

(3) Output Voltage Setting

The internal reference voltage of the ERROR AMP is 1.0V. Output voltage is obtained by Equation (4) of Figure 34, but it should be designed taking into consideration the NMOS ON-Resistance of SWOUT (about 50Ω).



$$V_O = \frac{(R_1 + R_2)}{R_2} \times 1.0 \quad [V] \quad (4)$$

Figure 34. Setting of Voltage Feedback Resistance

Selection of Part for Applications - continued

(4) DC/DC Converter Frequency Response Adjustment System

Condition for stable application
The condition for feedback system stability under negative feedback is that the phase delay is 135 °or less when gain is 1 (0 dB). Since DC/DC converter application is sampled according to the switching frequency, the bandwidth G_{BW} of the whole system (frequency at which gain is 0 dB) must be controlled to be equal to or lower than 1/10 of the switching frequency.
In summary, the conditions necessary for the DC/DC converter are:

- Phase delay must be 135°or lower when gain is 1 (0 dB).
- Bandwidth G_{BW} (frequency when gain is 0 dB) must be equal to or lower than 1/10 of the switching frequency.

To satisfy above two items, R_1, R_2, R_3, C_S and R_S in Figure 35 should be set as follows.

(a) R_1, R_2, R_3
BD8311NUV incorporates phase compensation devices of R_4=62kΩ and C_2=200pF. These C_2 and R_1, R_2, and R_3 values decide the primary pole that determines the bandwidth of DC/DC converter.

Primary pole point frequency

$$f_p = \frac{1}{2\pi\left\{A\times\left(\frac{R_1\times R_2}{R_1+R_2}+R_3\right)\times C_2\right\}} \quad \cdots\cdots\cdots\cdots\cdots(5)$$

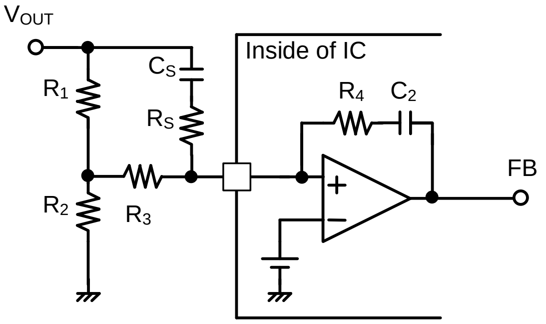


Figure 35. Example of Phase Compensation Setting

DC/DC Converter DC Gain

$$DC\,Gain = A\times\frac{1}{B}\times\frac{V_{OUT}}{V_{OUT}-V_{IN}} \quad \cdots\cdots\cdots\cdots (6)$$

where:
A is the ERROR AMP Gain
About 100dB = 10^5
B is the Oscillator Amplification = 0.5V
V_{IN} is the Input Voltage
V_{OUT} is the Output Voltage

Using Equations (5) and (6), the frequency f_{sw} of point 0 dB under limitation of the bandwidth of the DC gain at the primary pole point is as shown below.

$$f_{SW} = f_P \times DC\,Gain = \frac{1}{2\pi C_2\times\left(\frac{(R_1\times R_2)}{(R_1+R_2)}+R_3\right)}\times\frac{1}{B}\times\frac{V_{OUT}}{V_{OUT}-V_{IN}} \quad \cdots\cdots\cdots\cdots(7)$$

It is recommended that f_{sw} should be approximately 10kHz. When load response is difficult, it may be set at approximately 20kHz. In Equation (3), R_1 and R_2, which determines the voltage value, will be in the order of several hundred kΩ. Therefore, if an appropriate resistance value is not available and if routing may cause noise, the use of R_3 enables easy setting.

Selection of Part for Applications - continued

(b) C_S and R_S setting

In the step-up DC/DC converter, the secondary pole point is caused by the coil and capacitor as expressed by the following equation.

$$f_{LC} = \frac{1-D}{2\pi\sqrt{(LCout)}} \quad \cdots\cdots\cdots\cdots (8)$$

where:

D is the ON Duty = (V_{OUT} - V_{IN}) / Vout

Cout : Output Capacitor

This secondary pole causes a phase rotation of 180°. To secure the stability of the system, put zero points in 2 places to perform compensation.

Zero point by built-in CR $$f_{Z1} = \frac{1}{2\pi R_4 C_2} = 13kHz \quad \cdots\cdots\cdots\cdots (9)$$

Zero point by Cs $$f_{Z2} = \frac{1}{2\pi (R_1 + R_3) C_S} \quad \cdots\cdots\cdots\cdots (10)$$

Setting f_{Z2} frequency to be half to 2 times as large as f_{LC} provides an appropriate phase margin.
It is desirable to set Rs at about 1/20 of (R_1+R_3) to cancel any phase boosting at high frequencies.

These pole points are summarized in the figure below. The actual frequency property is different from the ideal calculation because of part constants. If possible, check the phase margin with a frequency analyzer or network analyzer, etc.. Otherwise, check for the presence or absence of ringing by load response waveform and also check for the presence or absence of oscillation under a load of an adequate margin.

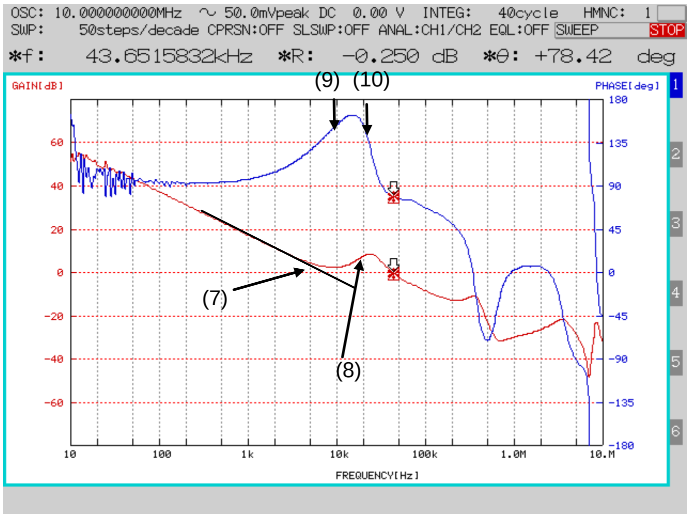
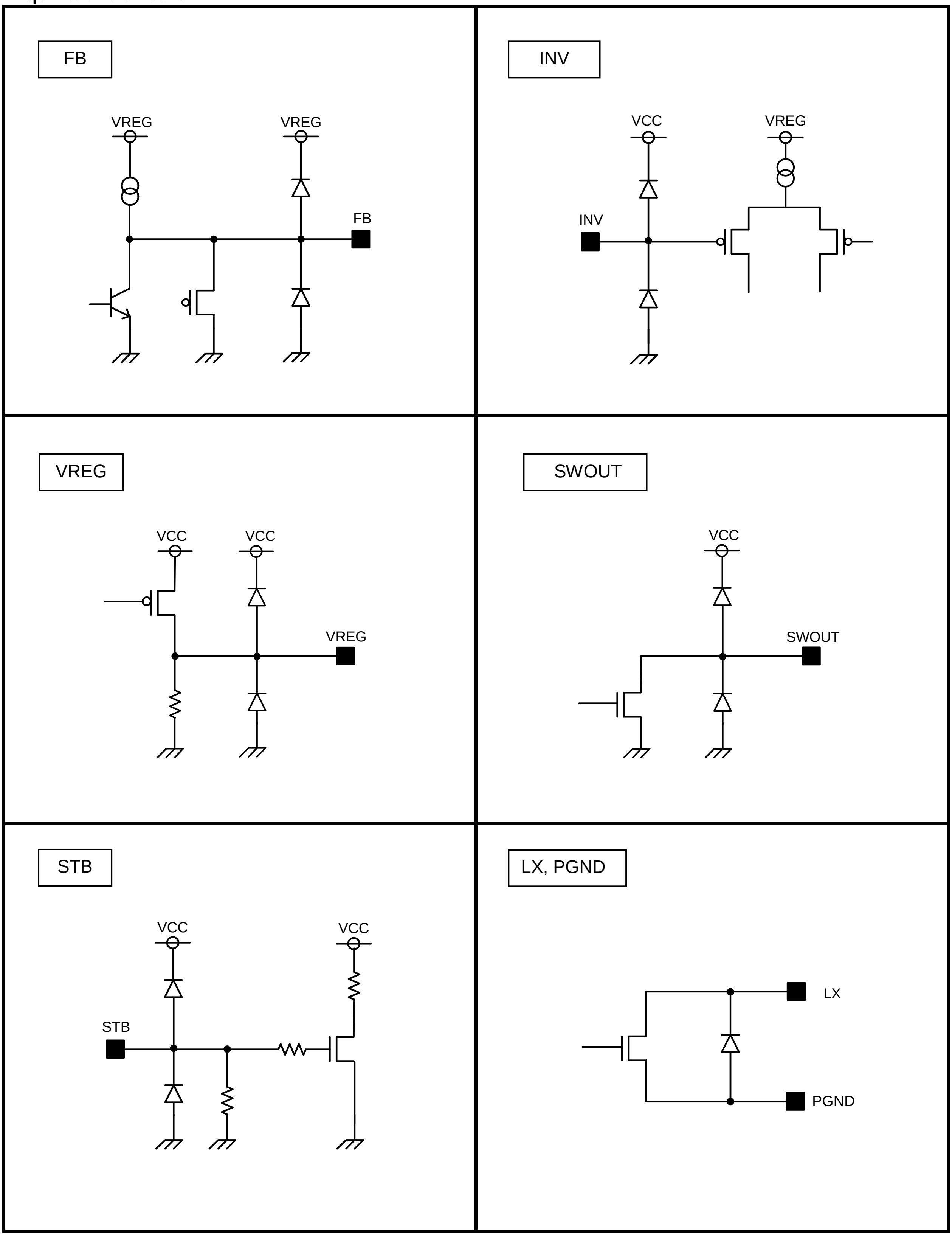


Figure 36. Example of DC/DC Converter Frequency Property
(Measured with FRA5097 by NF Corporation)

I/O Equivalent Circuit



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

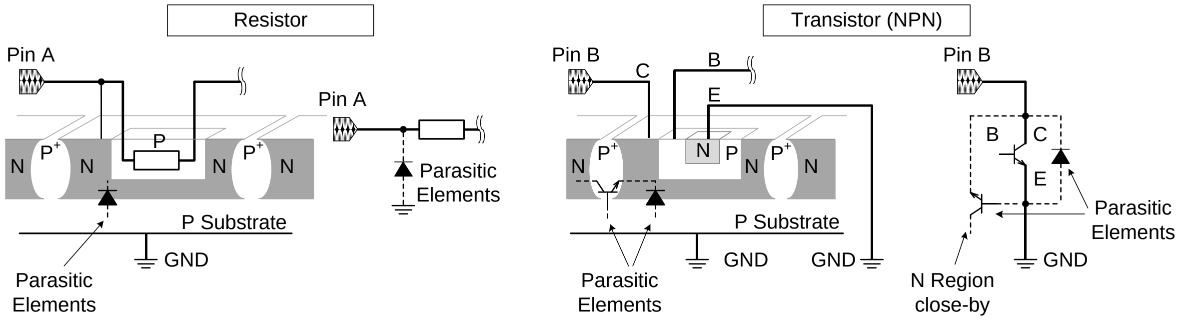


Figure 37. Example of monolithic IC structure

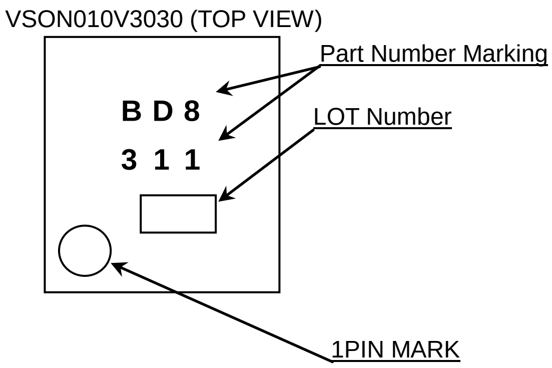
13. **Thermal Shutdown Circuit(TSD)**
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

B	D	8	3	1	1	N	U	V	-	E 2

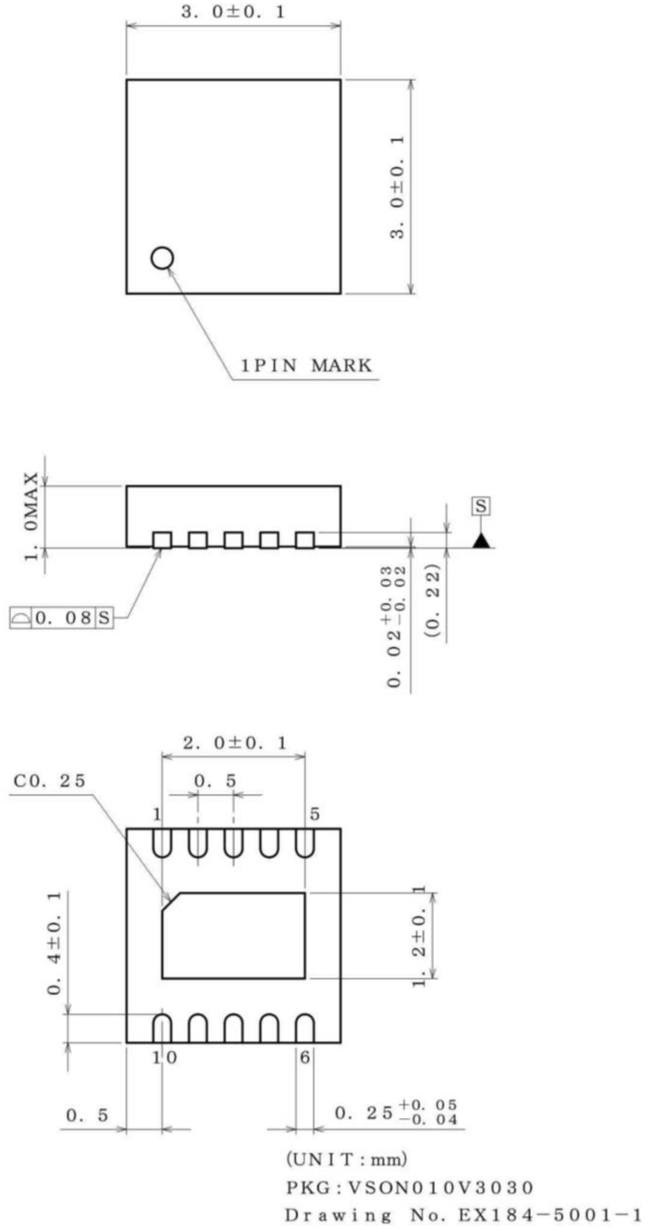
- Part Number: BD8311
- Package
  NUV: VSON010V3030
- Packaging and forming specification
  E2: Embossed tape and reel

Marking Diagram



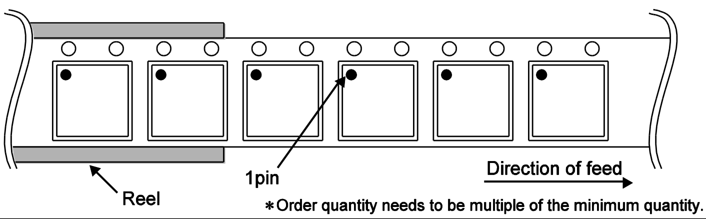
Physical Dimension, Tape and Reel Information

Package Name	VSON010V3030



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
26.Nov.2014	001	New Release
17.Feb.2015	002	Correction of the writing.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

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