Freescale Semiconductor
Product Brief

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QorIQ™ P1020 Integrated Processor Product Brief

This document provides an overview of features and functionality of the QorIQ™ P1020 integrated processor. The P1020 combines dual Power Architecture™ e500v2 processor cores with system logic required for networking, wireless infrastructure, and telecommunications applications.

The P1020 offers an excellent combination of protocol and interface support including dual high-performance CPU cores, an L2 cache, a DDR2/DDR3 memory controller, three enhanced three-speed Ethernet controllers with support for SGMII and for IEEE Std 1588™ precision time protocol for network synchronization over Ethernet, a TDM interface, two USB 2.0 interface, an independent SD/MMC card controller (eSDHC), integrated system performance monitor, and two PCI Express controllers.

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1 Application Examples

The following section provides block diagrams of different P1020 applications. The P1020 is a very flexible device and can be configured to meet many system application needs.

Both cores can operate in a symmetric multiprocessing mode to achieve higher performance, or they can run independent operating systems, each performing separate tasks. This flexibility enables application developers to assign distinct processing resources to distinct tasks that need guaranteed performance. For example, one core can manage a data plane and the other a control plane.

The value proposition of a dual-core device is further enhanced by a high degree of peripheral integration of system controllers such as DDR controllers. A device with faster internal buses can entirely replace the system controller where a discrete processor without integration was used previously.

1.1 Dual-Core Device Application

There are two main ways to map operating systems to the two P1020 cores:

- Symmetric multiprocessing
- Cooperative asymmetric multiprocessing
  - Two copies of the same OS that are non-SMP enabled
  - Two separate operating systems

Figure 1 shows how to use an integrated dual-core device such as the P1020. A line card uses an ASIC or network processing unit (NPU) for the data path. The ASIC/NPU manages user interfaces on the faceplate on the left as well as the interface to the backplane on the right. The dual-core device is responsible for the control plane. The two cores can operate in an SMP configuration, or two separate operating systems can be used for separate control plane tasks.

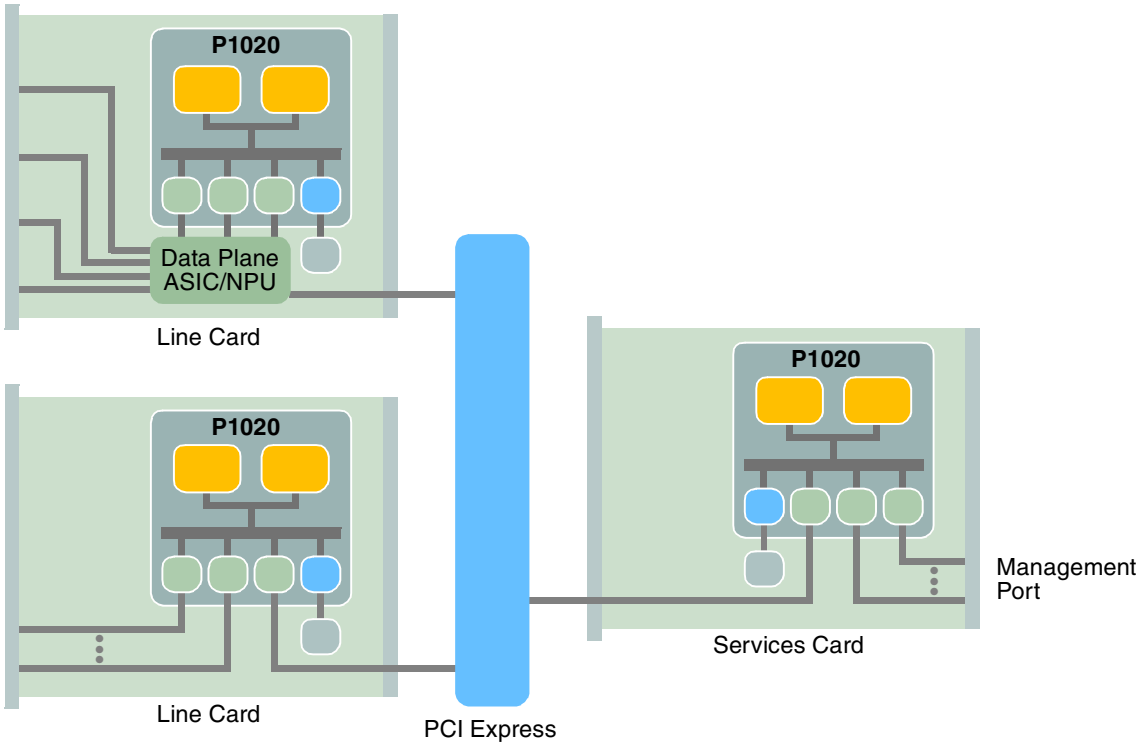

Figure 1. Integrated Dual-Core Device Application

The lower line card shows the eTSEC interfaces attach to faceplate connectors, and the PCI Express block connects to the backplane switch fabric. The CPUs handle both the control and data plane in a variety of configurations. Two popular alternatives split functionality directionally (one core per direction) or split functionality vertically (one core handling the data plane, one core handling the control plane).

At the right of the switch fabric is an example service card, which is easily added to a system to add new features without replacing all the line cards with upgraded ASICs. One service card supports a new feature set in a centralized scheme, receiving traffic from all line cards, so the high performance of a dual-core device is required. The PCI Express port connects to the fabric, and the eTSECs implement a management interface.

1.2 High-Performance Communication System

Figure 2 shows the P1020 as part of a high-end network card used in a system area network that is enabled by PCI Express.

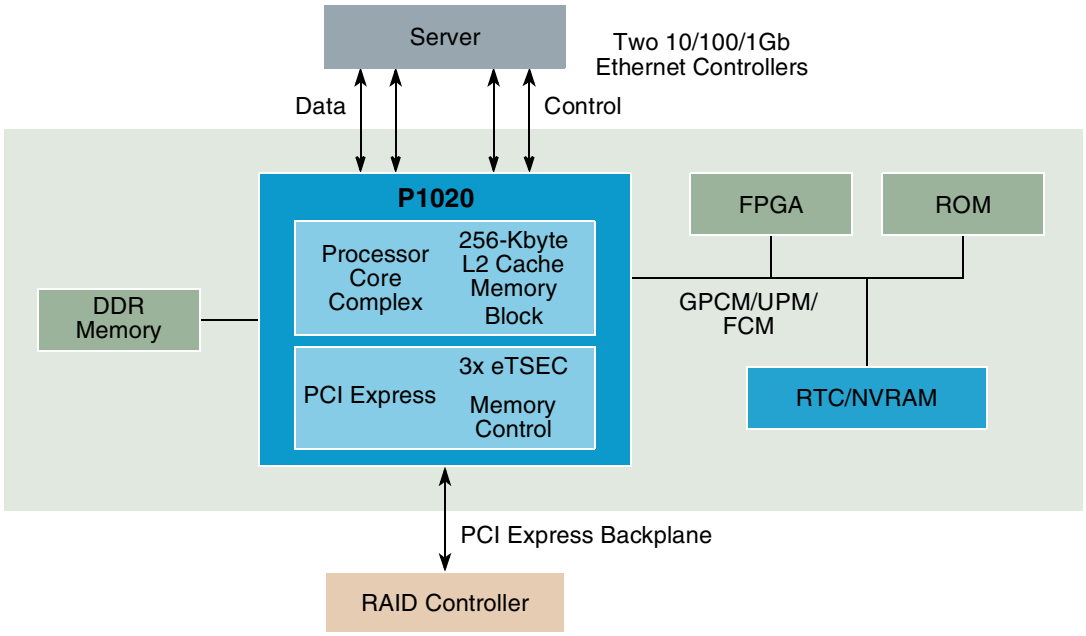

Figure 2. High-Performance Communication System

1.3 RAID Controller Application

Figure 3 shows the P1020 in a redundant array of independent disks (RAID) controller application.

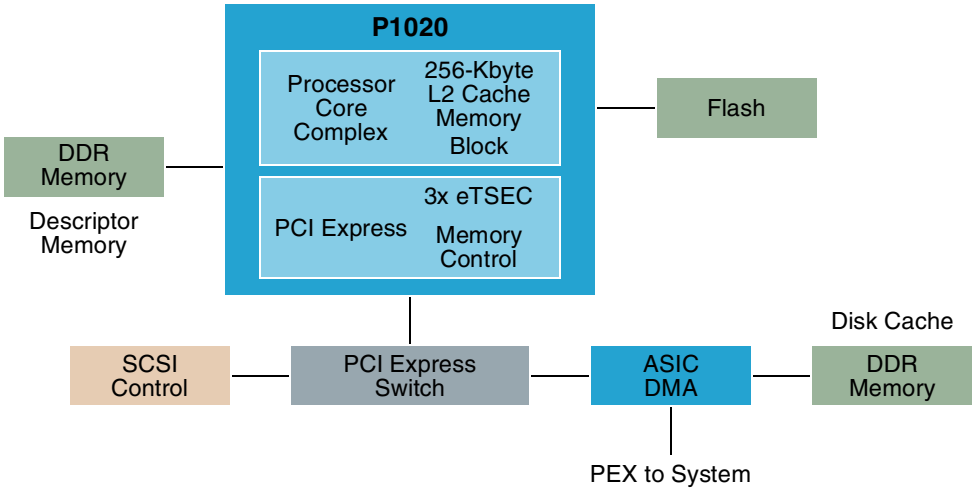

Figure 3. RAID Controller Application Using P1020

1.4 SMB Gateway Application

Figure 4 shows a multiservice router or business gateway targeting small-to-medium business customer premise equipment. The solution enables complete secure data, voice and wireless communications services in a single easy-to-manage platform.

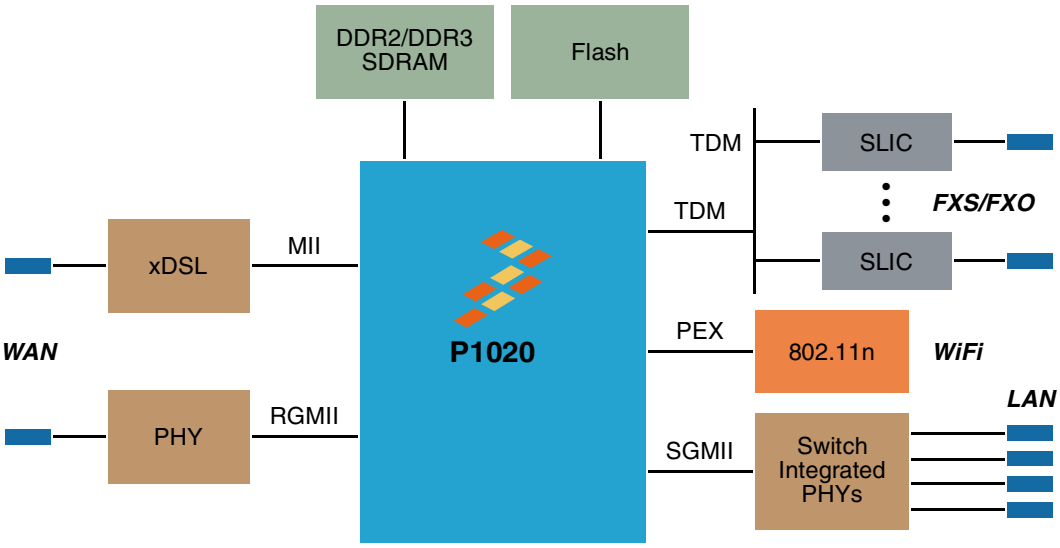

Figure 4. P1020 SMB Multiservice Gateway Example

1.5 WLAN Access Point Application

Figure 5 shows a high performance WLAN access point application where the CPU provided the complete data and control path processing needs for multiple MAC/radio interfaces. The P1020 is ideally suited for this application with its high performance system interfaces and best-in-class performance/watt.

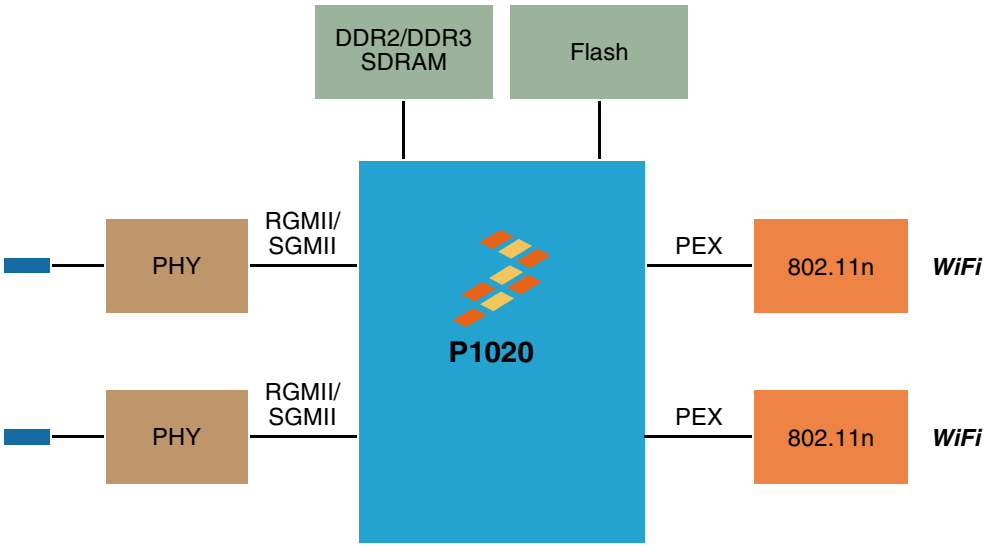

Figure 5. P1020 WLAN Access Point Example

2 Features

This section describes the features of the P1020.

2.1 Block Diagram

Figure 6 shows the major functional units within the P1020/P1011.

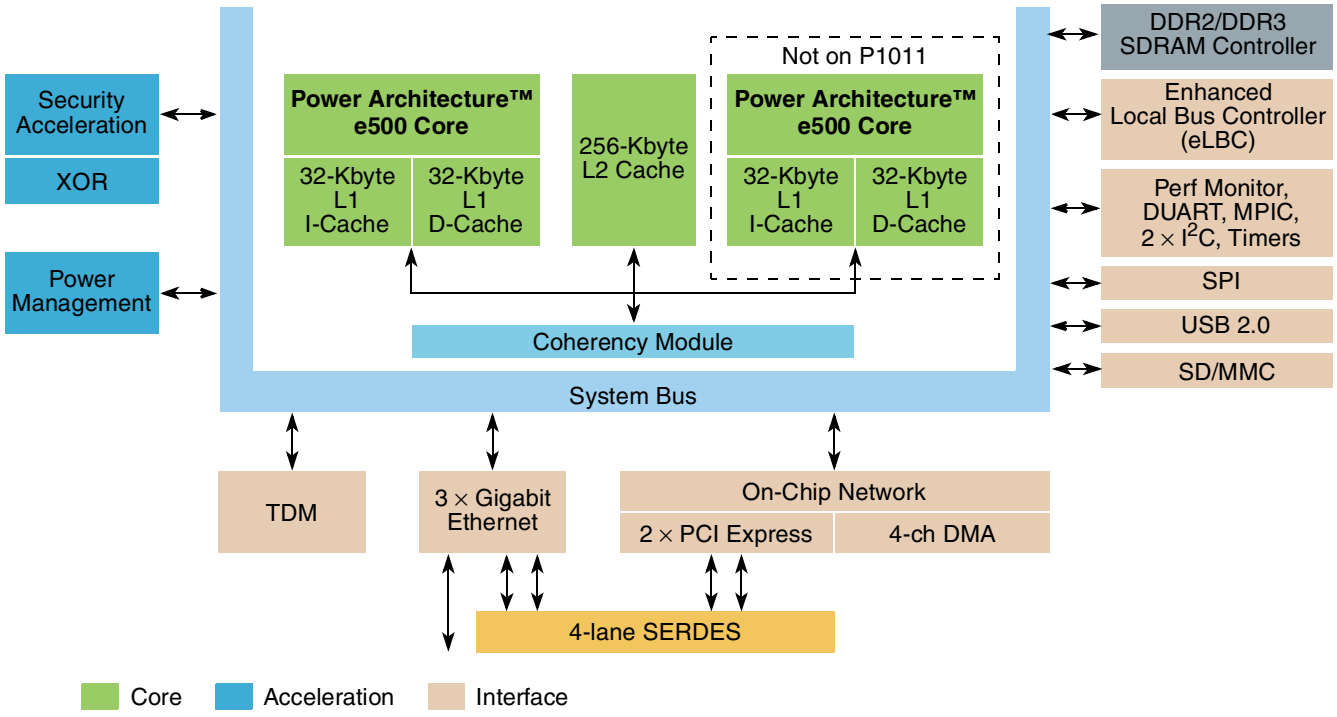

Figure 6. P1020/P1011 Block Diagram

2.2 Critical Performance Parameters

Critical performance parameters include the following:

- e500v2 core frequency of up to 800 MHz
- Power consumption less than 5.0 W at 800 MHz core speed
- 45-nm SOI process technology
- Data rate of up to 667 Mbps/pin for DDR2 and DDR3
- Supply voltage for core/platform: 0.95 V
- Operating junction temperature (T_j) range: 0–125°C and -40–125°C (industrial specification)
- 31 × 31 mm 689-pin TEPBGA II (temperature-enhanced plastic BGA)

2.3 Chip-Level Features

Key features of the P1020 include the following:

- Dual (P1020) or single (P1011) high-performance Power Architecture e500v2 cores

  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache for each core
  - 533 MHz to 800 MHz core clock frequency
- 256-Kbyte L2 cache with ECC, also configurable as SRAM and stashing memory
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration and classification capabilities
  - IEEE 1588 support
  - Lossless flow control
  - RGMII, RMII, SGMII
- High-speed interfaces (not all available simultaneously):
  - Four SerDes lanes running at 2.5 GHz (multiplexed across controllers)
  - Two x1 PCI Express interfaces
  - Two SGMII interfaces
- Two high-speed USB controllers (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
  - One dedicated USB interface, one multiplexed with the local bus
- Enhanced secure digital host controller (SD/MMC)
- Serial peripheral interface
- Integrated security engine (SEC 3.3.2)
  - Crypto algorithm support includes 3DES, AES, MD5/SHA, RSA/ECC, and FIPS deterministic RNG
  - Single pass encryption/message authentication for common security protocols (IPsec, SSL, SRTP, WiMax)
  - XOR acceleration
- 32-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Four-channel DMA controller
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- TDM interface supporting up to 128 channels
- 16 general-purpose I/O signals

These features are described in greater detail in subsequent sections.

NOTE

The P1020 is also available without a security engine. All specifications other than those relating to security apply to the non-security version exactly as described in this document.

2.4 Module Features

This section contains a high-level view of the P1020 architecture.

2.4.1 e500v2 Cores and Memory Unit

The P1020 contains two high-performance 32-bit e500v2 cores that implement the Power Architecture. In addition to 36-bit physical addressing, this version of the e500 core includes the following:

- SPE double-precision floating-point instruction set using 64-bit operands
- SPE embedded vector and scalar single-precision floating-point instruction set using 32- or 64-bit operands
- 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection

The device also contains 256 Kbytes of L2 cache/SRAM, as follows:

- Four-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global)
  - Regions can reside at any aligned location in the memory map
  - Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses

2.4.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500v2 cores and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The P1020 supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by ten local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The P1020 can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the P1020 to be part of larger address maps such as those of PCI Express.

2.4.3 Integrated Security Engine (SEC 3.3.2)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std 802.11i™, IEEE Std 802.16™ (WiMAX), and IEEE Std 802.1AE™ . (MACSec). Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the P1020 is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and IEEE 802.11i.

SEC features include the following:

- Compatible with code written for the Freescale MPC8548E, MPC8555E, MPC8541E, and MPC8572E devices
- XOR engine for parity checking in RAID storage applications
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  - PKEU—public key execution unit
  - DEU—data encryption standard execution unit
  - AESU—advanced encryption standard unit
  - MDEU—message digest execution unit
  - CRCU—cyclical redundancy check unit
  - RNG—random number generator

2.4.4 Enhanced Three-Speed Ethernet Controllers (eTSECs)

The P1020 has three on-chip enhanced eTSECs. The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/IEEE Std 802.3™ networks with SGMII, RGMII, and RMII physical interfaces. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit DMA functions.

The P1020 eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are designed to comply with IEEE 802.3, IEEE Std 802.3u™, IEEE Std 802.3x™, IEEE Std 802.3z™, IEEE Std 802.3ac™, and IEEE Std 802.3ab™.

The buffer descriptors are based on the MPC8540 three-speed Ethernet controller programming model. Each eTSEC can emulate a PowerQUICC III TSEC, allowing existing driver software to be re-used with minimal change.

Some of the key features of these controllers include the following:

- Flexible configuration for multiple PHY interface configurations. Table 1 lists available configurations.

Table 1. eTSEC Configuration Options[1]

eTSEC1	eTSEC2	eTSEC3
RGMII -or- none	SGMII -or- none	RGMII -or- SGMII -or- none

Notes:
1 The parallel interface I/O voltages operate simultaneously at either 2.5 or 3.3 V (nominal)

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex)
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE 802.1 virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

2.4.5 Universal Serial Bus (USB) 2.0

The P1020 USB 2.0 controller provides point-to-point connectivity complying with the *Universal Serial Bus Revision 2.0 Specification*. The USB controller can be configured to operate as a stand-alone host, stand-alone device, or both host and device functions operating simultaneously. The host and device functions are both configured to support the following types of USB transfers:

- Bulk

- Control
- Interrupt
- Isochronous

Some of the key features include the following:

- Supports USB dual-role operation and can be configured as host or device
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports six programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Supports external PHY with UTMI+ low-pin interface (ULPI)

2.4.6 DDR SDRAM Controller

The P1020 supports DDR2 and DDR3 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 4 Gbytes of main memory.

The P1020 supports a variety of SDRAM configurations. Sixteen multiplexed address signals provide for device densities from 32 Mbits to 4 Gbits. Four chip select signals support up to four banks of memory. The P1020 supports bank sizes from 32 Mbytes to 4 Gbytes. Five column address strobes ($\overline{\text{MDM}}$[0:3], $\overline{\text{MDM8}}$) are used to provide byte selection for memory bank writes.

The P1020 can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 32 simultaneously open pages can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the P1020 detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The P1020 can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

The P1020 offers both hardware and software options to support battery-backed main memory. In addition, the DDR controller offers an initialization bypass feature which system designers may use to prevent re-initialization of main memory during system power-on following abnormal shutdown.

2.4.7 High Speed I/O Interfaces

The P1020 supports the SGMII and PCI Express high-speed I/O interface standards.

2.4.7.1 PCI Express Interfaces

The P1020 supports two PCI Express interfaces designed to comply with the *PCI Express Base Specification Revision 1.0a*. They are configurable at boot time to act as either root complex or endpoint.

The physical layer of the PCI Express interface operates at a transmission rate of 2.5 Gbaud (data rate of 2.0 Gbps) per lane. The theoretical unidirectional peak bandwidth is 2 Gbps per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 4 Gbps per lane.

Other features of the PCI Express interface include:

- Supports two x1 interfaces
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows

2.4.7.2 SGMII

The serial gigabit media independent interface (SGMII) is a high-speed interface linking the Ethernet controller with an Ethernet PHY. SGMII uses differential signaling for electrical robustness. Only four signals are required: receive data and its inverse, and send data and its inverse; no clock signals are required.

2.4.7.3 High-Speed Interface Multiplexing

Table 2 shows the supported high-speed interface configurations. The desired configuration must be selected at power-on reset.

Table 2. Supported High-Speed Interface Combinations

Lanes				Gbaud	
A	**B**	**E**	**F**	**A&B**	**E&F**
PEX1: x1	PEX2: x1	SGMII2	SGMII3	2.5	1.25

2.4.8 Programmable Interrupt Controller (PIC)

The P1020 PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported. The PIC can be bypassed to allow use of an external interrupt controller.

2.4.9 Time Division Multiplexing (TDM) Interface

The TDM interface supports the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive
- 8- or 16-bit word widths
- The TDM Transmitter Sync Signal (TFS), Transmitter Clock Signal (TCK) and Receiver Clock Signal (RCK) can be configured as either input or output
- Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock
- Frame sync can be programmed as active low or active high
- MSB or LSB first support

2.4.10 Enhanced Secure Digital Host Controller (eSDHC)

The eSDHC provides an interface between the host system and several types of memory cards: MultiMediaCard (MMC), secure digital (SD) card. The eSDHC acts as a bridge, passing host bus transactions to SD/MMC cards by sending commands and performing data accesses to or from the cards.

The eSDHC includes the following features:

- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD modes, 1-/4-bit MMC modes
  - Up to 200 Mbps data transfer for SD/MMC cards, using 4 parallel data lines
- Supports single- and multi-block read and write
- Supports write protection switch for write operations
- Supports synchronous and asynchronous abort
- Supports pause during the data transfer at a block gap
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer commands while the data transfer is in progress
- Embodies a fully configurable 128 × 32-bit FIFO for read/write data
- Supports internal DMA capabilities

2.4.11 DMA, I^2C, DUART, and Enhanced Local Bus Controller (eLBC)

The P1020 provides an integrated four-channel DMA controller, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller can be used as follows:

- To chain (both extended and direct) through local memory-mapped chain descriptors
- To handle misaligned transfers as well as stride transfers and complex transaction chaining

- To specify local attributes such as snoop and L2 write stashing

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. Both the transmitter and receiver support 16-byte FIFOs.

The P1020 enhanced local bus controller (eLBC) port allows connection with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface with synchronous devices or custom ASIC interfaces. The NAND flash control machine (FCM) further extends interface options. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or FCM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 32-bit address and data bus operating at 100 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 16- and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8 or 16 bits)
- FCM supports NAND flash, GPCM supports NOR flash

2.4.12 Device Boot Locations

The P1020 may be configured to boot using one of the following interfaces:

- DDR2/DDR3 memory controller
- Any PCI Express interface
- Enhanced local bus interface (using the GPCM or FCM)
- SPI flash
- SD/MMC flash

2.4.13 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

3 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and the Freescale Alliance Program, including third party protocol and signaling stack suppliers, real-time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

4 Document Revision History

Table 3 provides a revision history for this product brief.

Table 3. Document Revision History

Rev. No.	Date	Substantive Change(s)
0	11/2008	Initial release.

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