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FEUL610Q101-02

ML610Q101/ML610Q102
User's Manual

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q101 / ML610Q102.

The following manuals are also available. Read them as necessary.

■ nX-U8/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U8/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ IDEU8 User's Manual
Description on the integrated development environment IDEU8.

■ uEASE User's Manual
Description on the on-chip debug tool uEASE.

■ uEASE connection Manual for ML610QXXX
Description about the connection between uEASE and ML610QXXX.

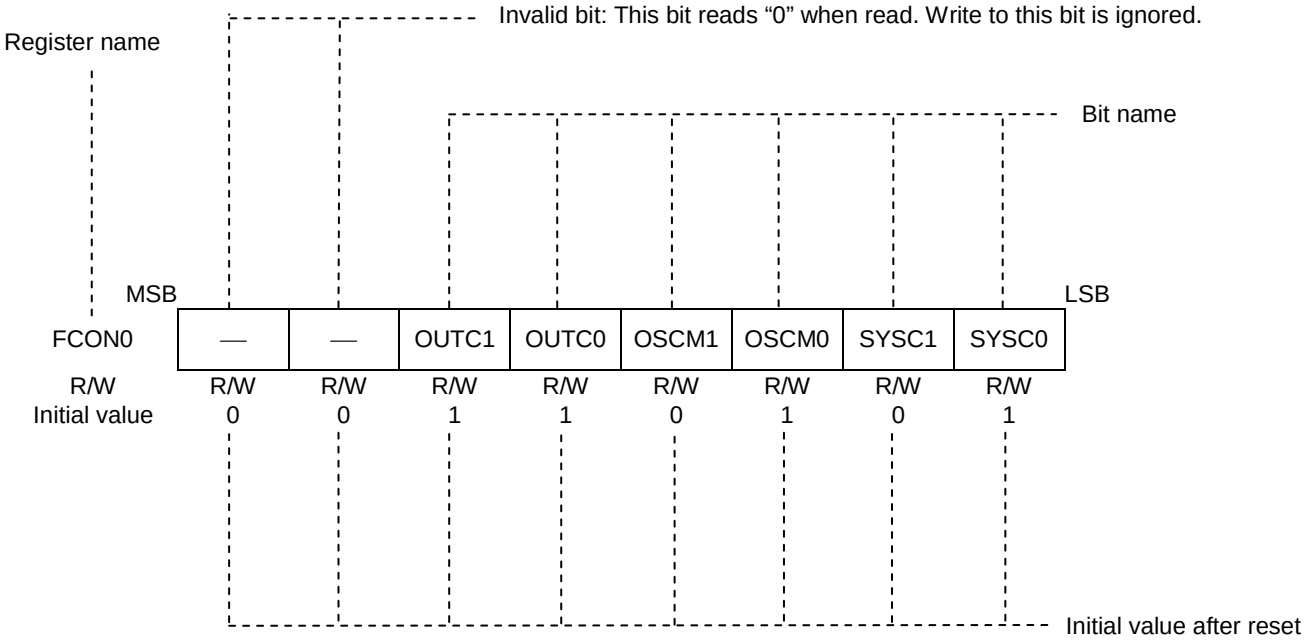
■ FWuEASE Flash Writer Host Program User's Manual
Description on the Flash Writer host program.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1

Overview

1 Overview

1.1 Features

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as timers, PWM, UART, voltage level supervisor (VLS) function, and 10-bit successive approximation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by pipe line architecture parallel processing.
The on-chip debug function that is installed enables program debugging and programming.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set:
    Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5μs (@32.768kHz system clock)
    0.122μs (@8.192MHz system clock)

- Internal memory
  - ML610Q101 : Internal 4Kbyte Flash ROM (2K×16 bits) (including unusable 32 byte test data area)
  - ML610Q102 : Internal 6Kbyte Flash ROM (3K×16 bits) (including unusable 32 byte test data area)
  - Internal 256byte data RAM (256×8 bits)

- Interrupt controller
  - 1 non-maskable interrupt source (Internal source: 1)
  - 21 maskable interrupt sources (Internal sources: 16, External sources: 5)

- Time base counter (TBC)
  - Low-speed time base counter ×1 channel
  - High-speed time base counter ×1 channel

- Watchdog timer (WDT)
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable by software (125ms, 500ms, 2s, and 8s)

- Timer
  - 8 bits × 6 channels (16-bit configuration available)
  - Support Continuos timer mode/one shot timer mode
  - Timer start/stop function by software or external trigger input

- PWM
  - Resolution 16 bits × 1 channel
  - Support Continuos timer mode/one shot timer mode
  - PWM start/stop function by software or external trigger input

- UART
  - Half-duplex
  - TXD/RXD × 1 channels
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Successive approximation type A/D converter (SA-ADC)
  - 10-bit A/D converter
  - Input × 6 channels

- Analog Comparator
  - Operating voltage: V_{DD} = 2.7V to 5.5V
  - Common mode input voltage range : V_{DD} = 0.1V to V_{DD} - 1.5V
  - Hysteresis (Comparator0 only): 20mV(Typ.)
  - Allows selection of interrupt disabled mode,falling-edge interrupt mode,rising-edge interrupt mode, or both-edge interrupt mode.

- General-purpose ports (GPIO)
  - Input/output port × 11 channels (including secondary functions)

- Reset
  - Reset by the RESET_N pin
  - Reset by power-on detection
  - Reset by the watchdog timer (WDT) overflow
  - Reset by voltage level supervisor(VLS)

- Voltage level supervisor (VLS)
  - Judgment accuracy: ±3.0% (Typ.)
  - It can be used for voltage level detection reset.

- Clock
  - Low-speed clock:
    Built-in RC oscillation (32.768 kHz)
  - High-speed clock:
    Built-in PLL oscillation (16.384 MHz), external clock
    * The clock of the CPU is 8.192MHz(Max)
  - Selection of high-speed clock mode by software:
    Built-in PLL oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - 16-pin plastic SSOP
    ML610Q101-xxxMB (Blank product: ML610Q101-NNNMB)
    ML610Q102-xxxMB (Blank product: ML610Q102-NNNMB)
    xxx: ROM code number

  - 16-pin WQFN
    ML610Q101-xxxGD (Blank product: ML610Q101-NNNGD)
    ML610Q102-xxxGD (Blank product: ML610Q102-NNNGD)
    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: –40°C to 85°C
  - Operating voltage: V_{DD} = 2.7V to 5.5V

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML610Q101

Figure 1 show the block diagram of the ML610Q101.
"*" indicates secondary function, tertiary function or quaternary function of each port.

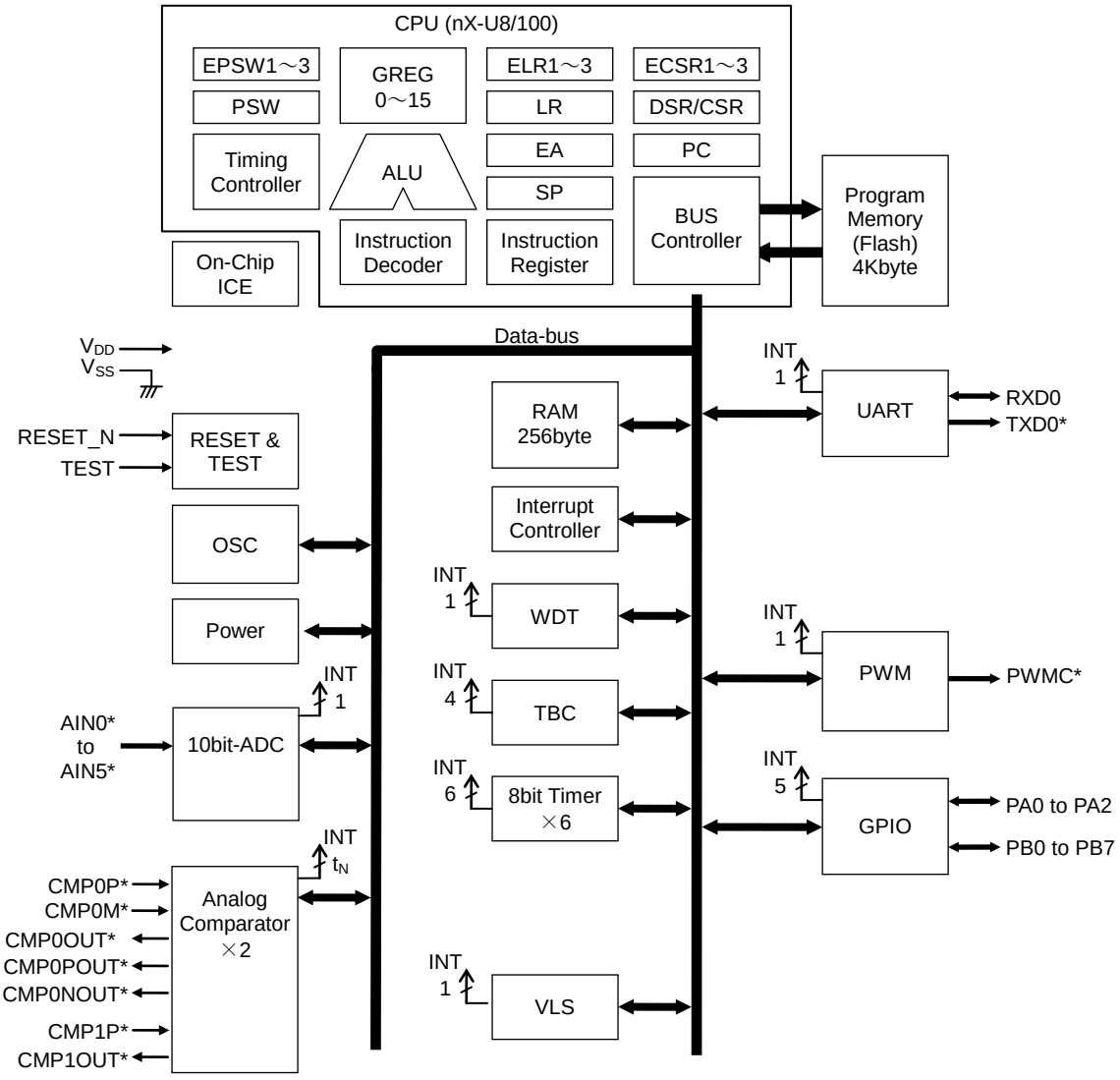


Figure 1-1 ML610Q101 Block Diagram

1.2.2 Block Diagram of ML610Q102

Figure 2 show the block diagram of the ML610Q102.
"*" indicates secondary function, tertiary function or quaternary function of each port.

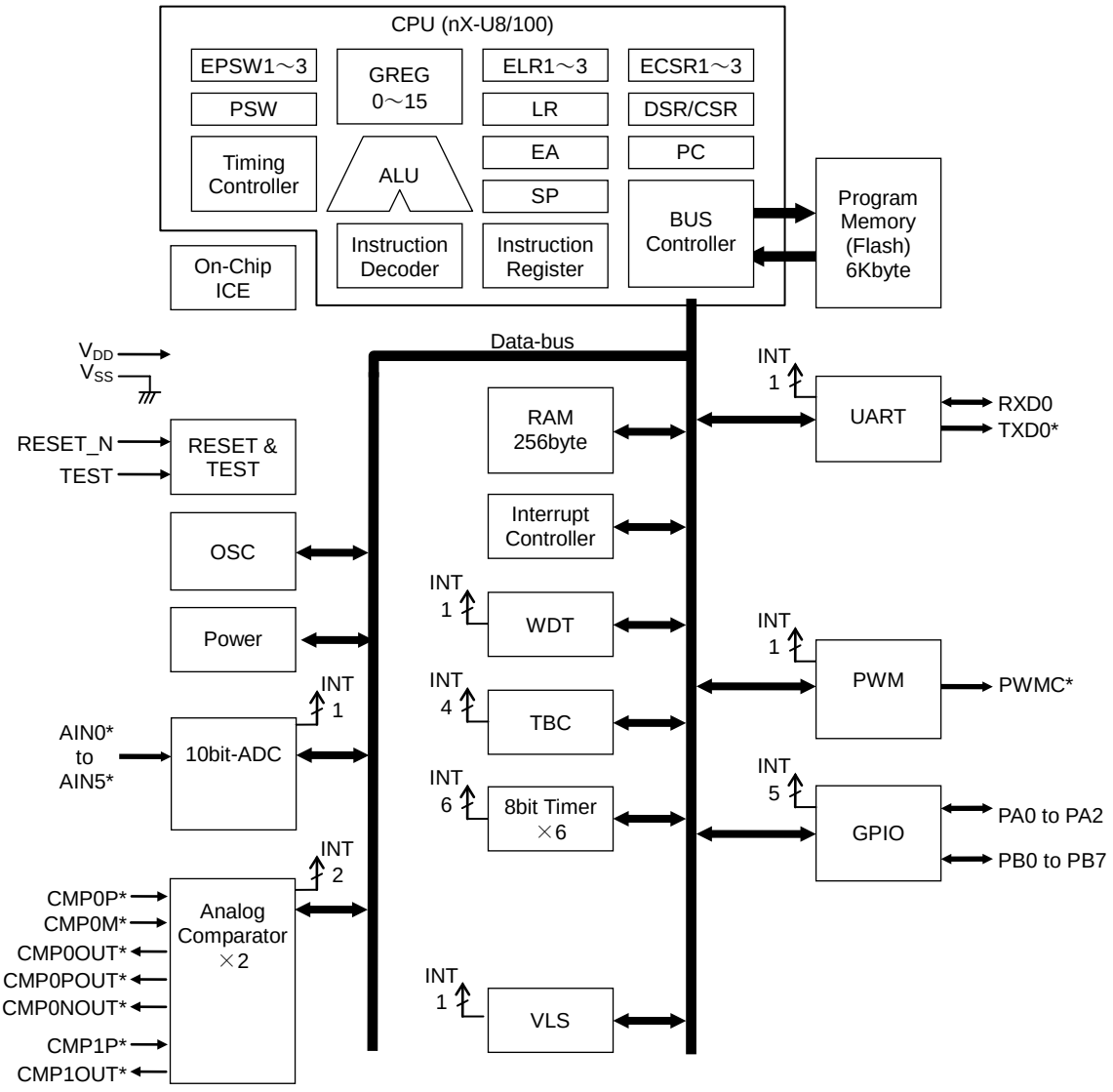


Figure 2 ML610Q102 Block Diagram

1.3 Pins

1.3.1 Pin Layouts

1.3.1.1 Pin Layout of ML610Q101/ML610Q102 SSOP16 Package

Figure 3 show the SSOP16 pin layout of the ML610Q101/ML610Q102.

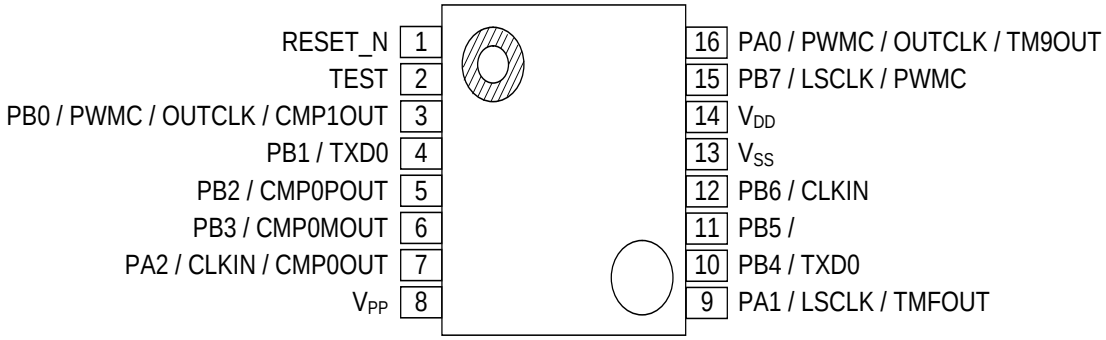


Figure 3 Pin Layout of ML610Q101/ML610Q102 SSOP16 Package

1.3.1.2 Pin Layout of ML610Q101/ML610Q102 WQFN16 Package

Figure 4 show the WQFN16 pin layout of the ML610Q101/ML610Q102.

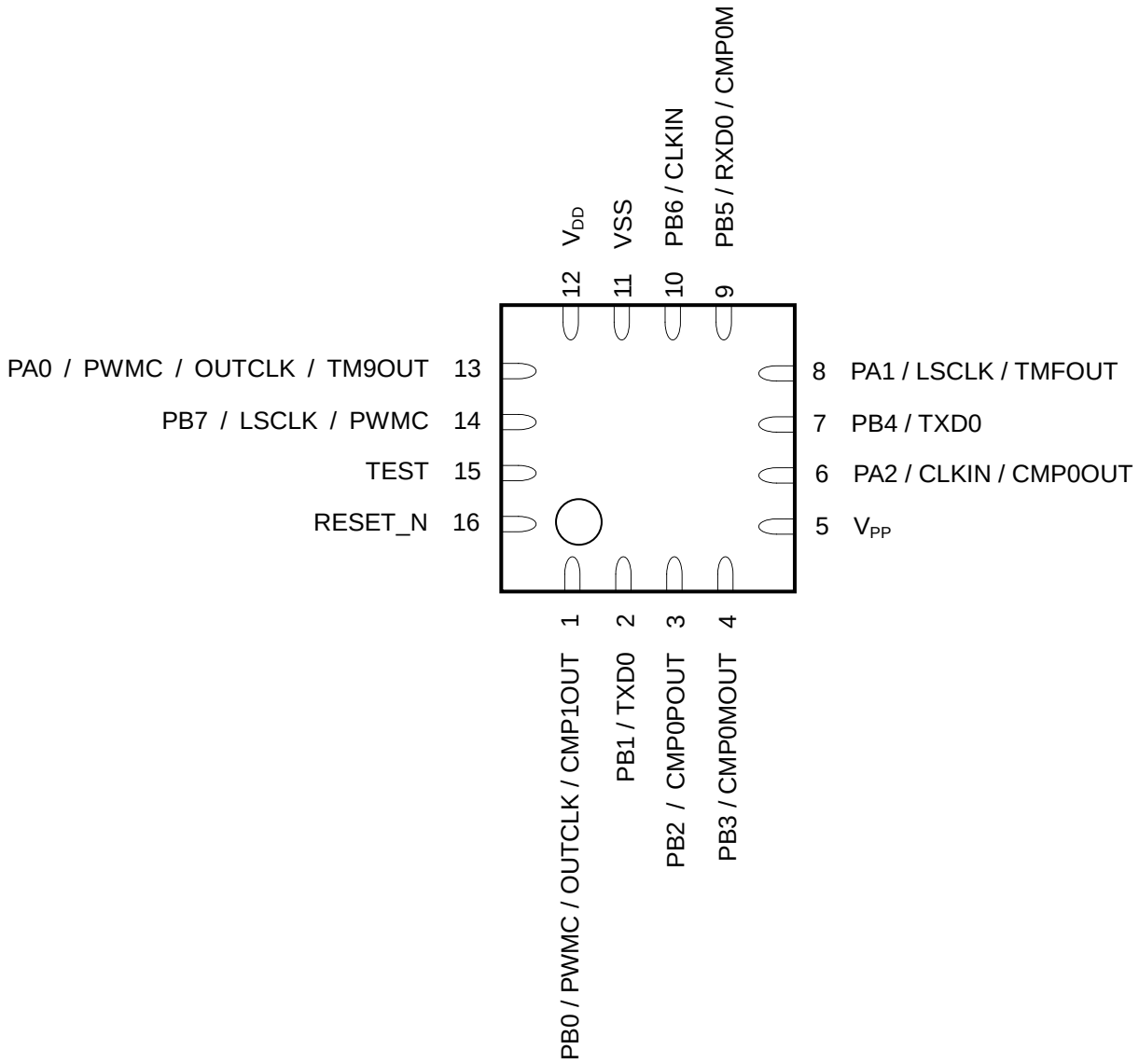


Figure 4 Pin Layout of ML610Q101/ML610Q102 WQFN16 Package

1.3.2 List of Pins

Table 1-1 shows list of pins.

Table 1-1 List of pins

PIN No. (SSOP)	PIN No. (WQFN)	Primary function			Secondary function			Tertiary function			Quaternary function		
		Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
1	16	RESET_N	I	Reset input pin	—	—	—	—	—	—	—	—	—
2	15	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—	—	—	—
3	1	PB0/ EXI4/ AIN2/ RXD0	I/O	Input/output port, External interrupt 4, ADC input 2, UART receive	PWMC	O	PWMC output	OUTCLK	O	High-speed clock output	CMP1OUT	O	CMP1 output
4	2	PB1/ EXI5/ AIN3	I/O	Input/output port, External interrupt 5,ADC input 3	—	—	—	TXD0	O	UART data output	—	—	—
5	3	PB2	I/O	Input/output port,	—	—	—	—	—	—	CMP0POUT	O	CMP0__P output
6	4	PB3	I/O	Input/output port	—	—	—	—	—	—	CMP0NOUT	O	CMP0__N output
7	6	PA2/EXI2	I/O	Input/output port, External interrupt	—	—	—	CLKIN	I	clock input	CMP0OUT	O	CMP0 output
8	5	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—	—	—	—
9	8	PA1/ EXI1/ AIN1/ CMP1P	I/O	Input/output port, External interrupt 1, ADC input 1, Comparator1 non-inverting input	—	—	—	LSCLK	O	Low speed clock output	TMF OUT	O	timer F output
10	7	PB4/ CMP0P	I/O	Input/output port, Comparator0 non-inverting input	—	—	—	TXD0	O	UART data output	—	—	—
11	9	PB5/ RXD0/ CMP0M	I/O	Input/output port, UART data receive, Comparator1 inverting input	—	—	—	—	—	—	—	—	—
12	10	PB6/ AIN4	I/O	Input/output port, ADC input 4	CLKIN	I	clock input	—	—	—	—	—	—
13	11	Vss	—	Negative power supply pin	—	—	—	—	—	—	—	—	—
14	12	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—	—	—	—
15	14	PB7/ AIN5	I/O	Input/output port, ADC input 5	LSCLK	O	Low-speed clock output	—	—	—	PWMC	O	PWMC output
16	13	PA0/ EXI0/ AIN0	I/O	Input/output port, External interrupt 0, ADC input 0	PWMC	O	PWMC output	OUTCLK	O	High-speed clock output	TM9OUT	O	timer 9 output

1.3.3 Description of Pins

Table 1-2 shows description of pins.

Table 1-2 (1/2) Description of pins

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
CLKIN	I	High-speed clock output pin. This pin is used as the tertiary function of the PA2 or the secondary function of PB6 pin.	Secondary/ Tertiary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the tertiary function of the PA1 or the secondary function of the PB7 pin.	Secondary/ Tertiary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the tertiary function of the PA0 or PB0 pin.	Tertiary	—
General-purpose input/output port				
PA0 to PA2 PB0 to PB7	I/O	General-purpose input/output port. Since these pins have secondary functions and tertiary functions and quaternary functions, the pins cannot be used as a port when the secondary functions and tertiary functions and quaternary functions are used.	—	Positive
UART				
TXD0	O	UART0 data output pin. This pin is used as the tertiary function of the PB1 or PB4 pin.	Tertiary	Positive
RXD0	I	UART0 data input pin. This pin is used as the primary function of the PB0 or PB5 or the quaternary function of the PB7 pin.	Primary	Positive
PWM				
PWMC	O	PWMC output pin. This pin is used as the secondary function of the PB0 or PA0 or the quaternary function of the PB7 pin.	Secondary Quaternary	Positive
External interrupt				
EXI0 to 2	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PA0 – PA2 pins.	Primary	Positive/ negative
EXI4,5	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PB0, PB1 pins.	Primary	Positive/ negative
Timer				
TnTG	I	External clock input pin used for both Timer E and Timer F.These pins are used as the primary function of the PA0-PA2, PB0-PB7 pins.	Primary	—
TM9OUT	O	Timer 9 output pin. This pin is used as the quaternary function of the PA0 pin.	Quaternary	Positive
TMFOUT	O	Timer F output pin. This pin is used as the quaternary function of the PA1 pin.	Quaternary	Positive

Table 1-2 (2/2) Description of pins

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
Successive approximation type A/D converter				
AIN0	I	Channel 0 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA0 pin.	Primary	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA1 pin.	Primary	—
AIN2	I	Channel 2 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB0 pin.	Primary	—
AIN3	I	Channel 3 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB1 pin.	Primary	—
AIN4	I	Channel 4 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB6 pin.	Primary	—
AIN5	I	Channel 5 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB7 pin.	Primary	—
Conparator				
CMP0P	I	Non-inverting input for comparator0. This pin is used as the primary function of the PB4 pin.	Primary	—
CMP0M	I	Inverting input for comparator0. This pin is used as the primary function of the PB5 pin.	Primary	—
CMP0OUT	O	Output for comparator0. This pin is used as the quaternary function of the PA2 pin.	Quaternary	—
CMP0OUT	O	Output for comparator0. This pin is used as the quaternary function of the PB2 pin.	Quaternary	—
CMP0OUT	O	Output for comparator0. This pin is used as the quaternary function of the PB3 pin.	Quaternary	—
CMP1P	I	Non-inverting input for comparator1. This pin is used as the primary function of the PA1 pin.	Primary	—
CMP1OUT	O	Output for comparator1. This pin is used as the quaternary function of the PB0 pin.	Quaternary	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	Positive
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{PP}	—	Power supply pin for Flash ROM	—	—

1.3.4 Termination of Unused Pins

Table 1-3 shows methods of terminating the unused pins.

Table 1-3 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	Open
TEST	Open
PA0 to PA2	Open
PB0 to PB7	Open
V_{PP}	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

Chapter 2

CPU and Memory Space

2 CPU and Memory Space

2.1 Overview

This LSI includes 8-bit CPU nX-U8/100 and the memory model is "SMALL model".
For details of the CPU nX-U8/100, see "nX-U8/100 Core Instruction Manual".

2.2 Program Memory Space

The program memory space is used to store program codes, table data (ROM window), or vector tables.
The program codes have a length of 16 bits and are specified by a 16-bit program counter (PC).
The ROM window area data has a length of 8 bits and can be used as table data.
The vector table, which has 16-bit long data, can be used as reset vectors, hardware interrupt vectors, and software interrupt vectors.
The program memory space consists of 1 segments and ML610Q101 has 4-Kbyte (2-Kword) capacity, ML610Q102 has 6-Kbyte (3-Kword) capacity.
Figure 2-1 shows the configuration of the program memory space of the ML610Q101.
Figure 2-2 shows the configuration of the program memory space of the ML610Q102.

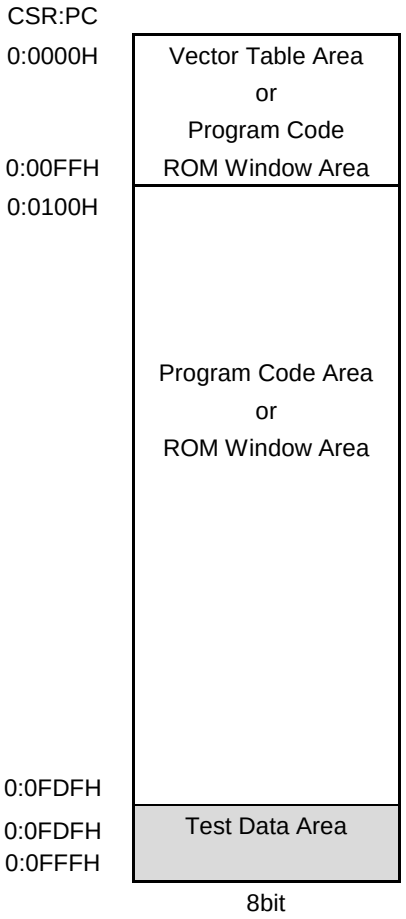


Figure 2-1 Configuration of Program Memory Space of the ML610Q101

Notes:
- Because test program data is stored in the 32Byte (16Word) test data area (0: 0FE0H to 0:0FFFH) of the Segment 0, this area cannot be used as a program code area.
- The address "0: 0FE0H to 0: 0FFFH" in the test area is write-able and erase-able. Fill the area with "0FFH". If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code can not be guaranteed.
- Set "0FFH" data (BRK instruction) in the unused area of the program memory space.

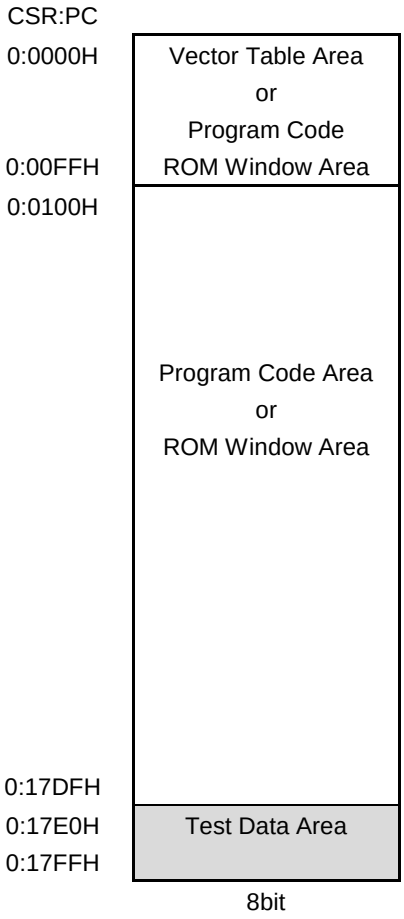


Figure 2-2 Configuration of Program Memory Space of the ML610Q102

Notes:
- Because test program data is stored in the 32Byte (16Word) test data area (0:17E0H to 0:17FFH) of the Segment 0, this area cannot be used as a program code area.
- The address "0: 17E0H to 0: 17FFH" in the test area is write-able and erase-able. Fill the area with "0FFH". If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code can not be guaranteed.
- Set "0FFH" data (BRK instruction) in the unused area of the program memory space.

2.3 Data Memory Space

The data memory space of this LSI consists of the ROM window area, 256Byte RAM area and SFR area of the Segment 0 and the ROM reference areas of the Segment 8.
The data memory stores 8-bit data and is specified by 20 bits consisting of higher 4 bits as DSR and lower 16 bits as addressing specified by each instruction.
Figure 2-3 shows the configuration of the data memory space of the ML610Q101.
Figure 2-4 shows the configuration of the data memory space of the ML610Q102.

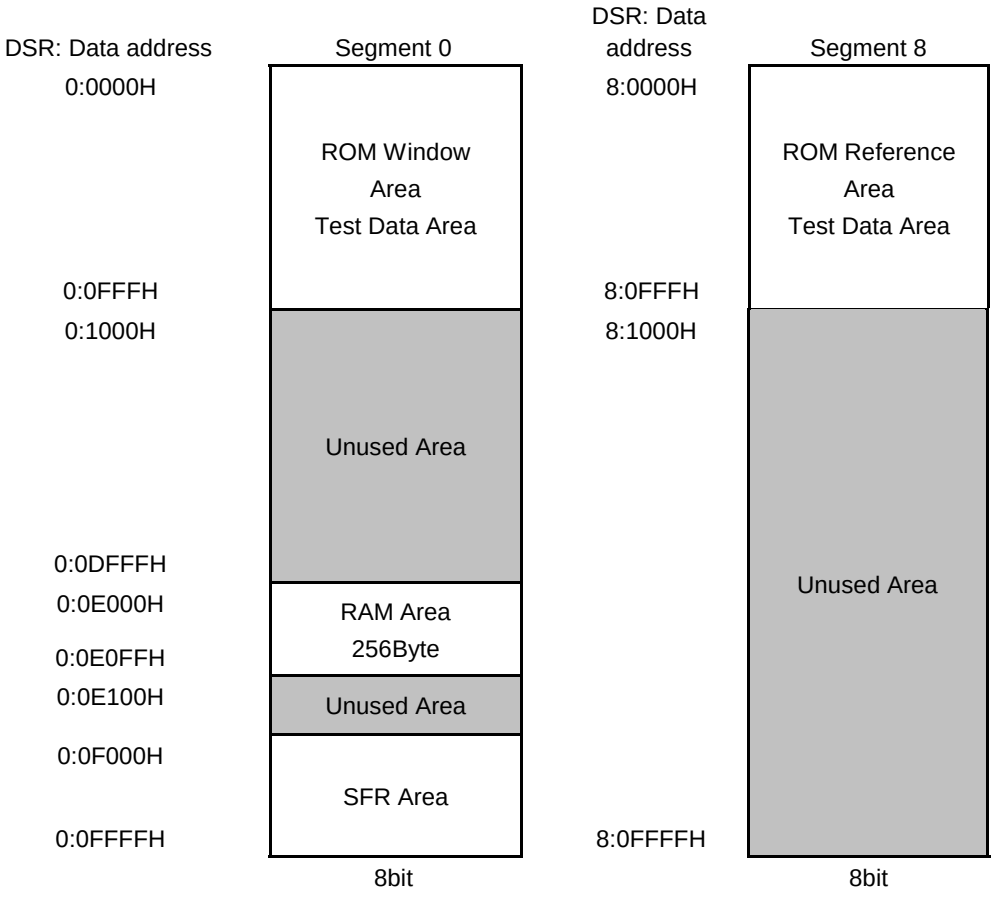


Figure 2-3 Configuration of Data Memory Space

Notes:
– The contents of the 256byte RAM area are undefined at system reset. Initialize this area by software.
– The contents of the Segment 0 of the program memory space are read from the ROM reference area of the Segment 8.

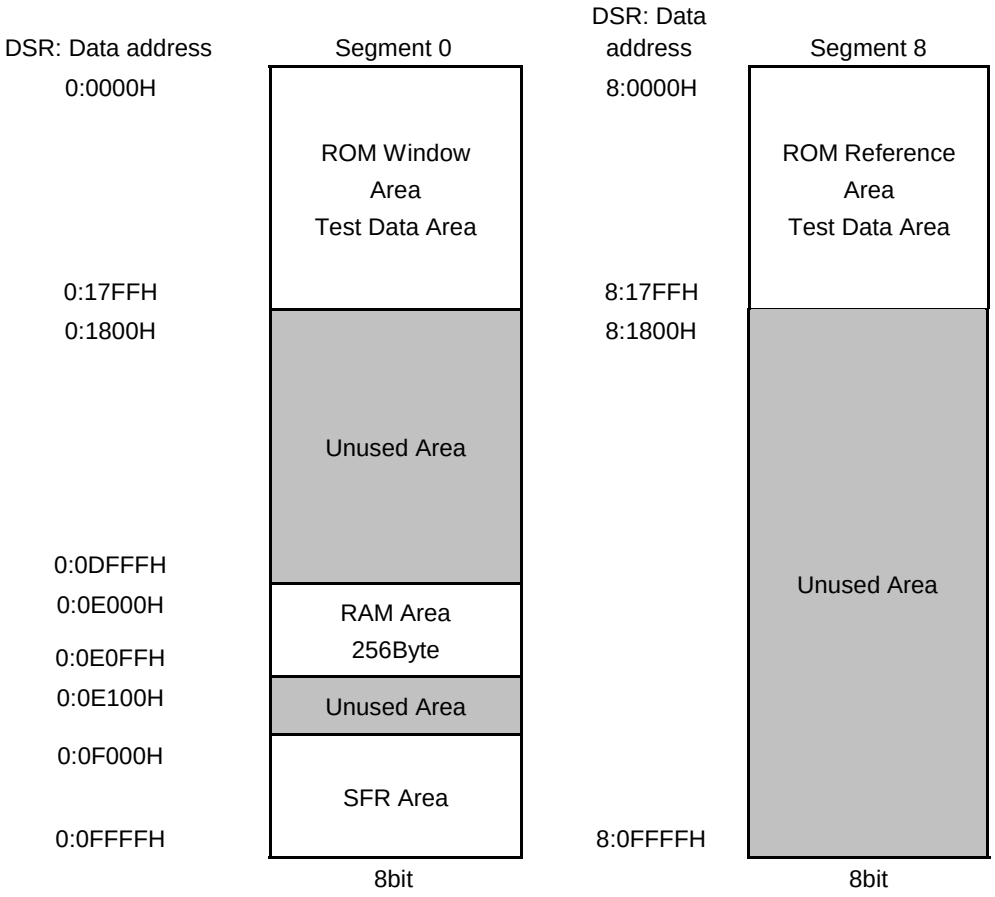


Figure 2-4 Configuration of Data Memory Space

Notes:
– The contents of the 256byte RAM area are undefined at system reset. Initialize this area by software.
– The contents of the Segment 0 of the program memory space are read from the ROM reference area of the Segment 8.

2.4 Instruction Length

The length of an instruction is 16 bits.

2.5 Data Type

The data types supported include byte (8 bits) and word (16 bits).

2.6 Description of Registers

2.6.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H

2.6.2 Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	—	—	—	—	DSR3	DSR2	DSR1	DSR0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) to retain a data segment address. For details of DSR, see "nX-U8/100 Core Instruction Manual".

[Description of Bits]

- **DSR3-DSR0** (bits 3-0)

DSR3	DSR2	DSR1	DSR0	Description
0	0	0	0	Data segment 0 (initial value)
0	0	0	1	Prohibited
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Data segment 8
1	0	0	1	Prohibited
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Chapter 3

Reset Function

3 Reset Function

3.1 Overview

This LSI has the five reset functions shown below. If any of the five reset conditions is satisfied, this LSI enters system reset mode.

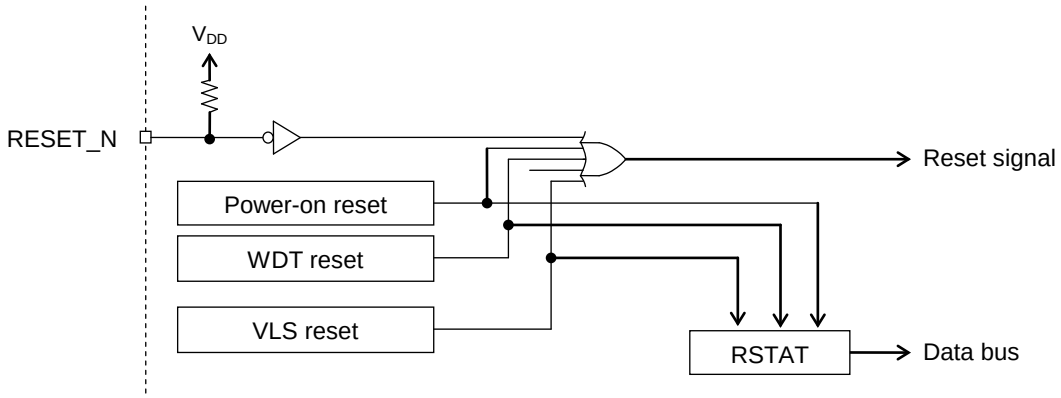
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Reset by the voltage level supervisor (VLS)
- Software reset by execution of the BRK instruction

3.1.1 Features

- The RESER_N pin has an internal pull-up resistor
- 250 ms, 1 sec, 4 sec, or 16 sec can be selected as the watchdog timer (WDT) second overflow period
- Built-in reset status register (RSTAT) indicating the reset generation causes
- Only the CPU is reset by the BRK instruction (neither the RAM area nor the SFR area are reset).

3.1.2 Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT: Reset status register

Figure 3-1 Configuration of Reset Generation Circuit

3.1.3 List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F001H	Reset status register	RSTAT	—	R/W	8	Undefined

3.2.2 Reset Status Register (RSTAT)

Address: 0F001H
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
RSTAT	—	—	VLSR	—	—	WDTR	—	POR
R/W	R	R	R/W	R	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	1

RSTAT is a special function register (SFR) that indicates the causes by which the reset is generated.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to "1". When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the contents of RSTAT to "00H".

[Description of Bits]

- **POR** (bit 0)
  The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to "1" when powered on.

POR	Description
0	Power-on reset not generated
1	Power-on reset generated

- **WDTR** (bit 2)
  The WDTR is a flag that indicates that the watchdog timer reset is generated. This bit is set to "1" when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

- **VLSR** (bit 5)

The VLSR is a flag that indicates that the voltage level supervisor (VLS) reset is generated. This bit is set to "1" when the reset by the VLS is generated.

VLSR	Description
0	Voltage level supervisor (VLS) reset not occurred
1	Voltage level supervisor (VLS) reset occurred

Note:
No flag is provided that indicates the occurrence of reset by the RESET_N pin.

3.3 Description of Operation

3.3.1 Operation of System Reset Mode

System reset has the highest priority among all the processing and any other processing being executed up to then is cancelled.
The system reset mode is set by any of the following causes.

- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Reset by the voltage level supervisor (VLS)
- Software reset by the BRK instruction (only the CPU is reset)

In system reset mode, the following processing is performed.

(1) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, the initialization is not performed by software reset due to execution of the BRK instruction. See Appendix A "Registers" for the initial values of the SFRs.
(2) CPU is initialized.
- All the registers in CPU are initialized.
- The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
- The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEEVL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see "nX-U8/100 Core Instruction Manual".

Note:
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

Chapter 4

MCU Control Function

4 MCU Control Function

4.1 Overview

The operating states of this LSI are classified into the following 4 modes including system reset mode:

System reset mode
Program run mode
HALT mode
STOP mode

For system reset mode, see Chapter 3, "Reset Function".

This LSI has a block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies) to make even more reducing the current consumption.

This LSI has software and hardware remap function for the boot area, too.

4.1.1 Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- STOP mode, where both low-speed oscillation and high-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies).

4.1.2 Configuration

Figure 4-1 shows an CPU operating state transition diagram.

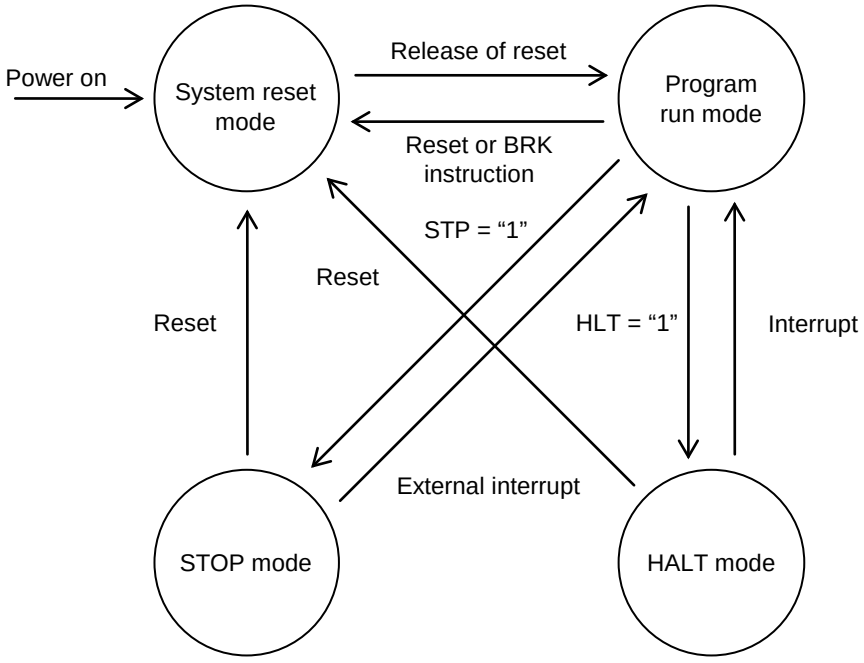


Figure 4-1 Operating State Transition Diagram

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F008H	Stop code acceptor	STPACP	—	W	8	—
0F009H	Standby control register	SBYCON	—	W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H
0F02EH	Block control register 6	BLKCON6	—	R/W	8	00H
0F02FH	Block control register 7	BLKCON7	—	R/W	8	00H

4.2.2 Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8 bits
Initial value: — (Undefined)

	7	6	5	4	3	2	1	0
STPACP	—	—	—	—	—	—	—	—
W	W	W	W	W	W	W	W	W
Initial value	—	—	—	—	—	—	—	—

STPACP is a write-only special function register (SFR) that is used for setting a STOP mode.
When STPACP is read, "00H" is read.
When data is written to STPACP in the order of "5nH" (n: an arbitrary value) and "0AnH" (n: an arbitrary value), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to "1" in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes "5nH" to STPACP and the instruction that writes "0AnH", the stop code acceptor is enabled after "0AnH" is written. However, if data other than "0AnH" is written to STPACP after "5nH" is written, the "5nH" write processing becomes invalid so that data must be written again starting from "5nH".
During a system reset, the stop code acceptor is disabled.

Note:
The STOP code acceptor can not be enabled on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).

4.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	—	—	—	—	—	—	STP	HLT
W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control operating mode of MCU.

[Description of Bits]

- **STP** (bit 1)
  The STP bit is used for setting the STOP mode. When the STP bit is set to "1" with the stop code adapter enabled by using STPACP, the mode is changed to the STOP mode. When the interrupt request enabled by the interrupt enable register (IE0-IE7) is issued, the STP bit is set to "0" and the LSI returns to the program run mode.

- **HLT** (bit 0)
  The HALT bit is used for setting a HALT mode. When the HALT bit is set to "1", the mode is changed to the HALT mode. When the WDT interrupt request, or enabled (the interrupt enable flag is "1") interrupt request is issued, the HALT bit is set to "1" and the mode is returned to program run mode.

STP	HLT	Description
0	0	Program run mode (initial value)
0	1	HALT mode
1	0	STOP mode
1	1	Prohibited

Note:
The mode can not be changed to HALT mode or STOP mode on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).
When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U8/100 core is "0", the STOP mode and the HALT mode are simply released and interrupt processing is not performed. Refer to the "nX-U8/100 Core Instruction Manual" for details of PSW.

4.2.4 Block Control Register 2 (BLKCON2)

Address: 0F02AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON2	—	—	—	—	—	DUA0	—	—
R/W	R	R	R	R	R	R/W	R	R
Initial value	0	0	0	0	0	0	0	0

BLKCON2 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DUA0** (bit 2)
  DUA0 controls the operation of UART0.

DUA0	Description
0	Enables the operation of UART0(initial value).
1	Disables the operation of UART0.

Note:

- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 11, "UART" for details of the UART operation.

4.2.5 Block Control Register 4 (BLKCON4)

Address: 0F02CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON4	—	—	—	—	—	—	—	DSAD
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON4 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DSAD** (bit 0)
  The DSAD bit is used to control SA type A/D converter operation. When the DSAD bit is set to "1", the circuits related to SA type A/D converter are reset and turned off.

DSAD	Description
0	Enable operating SA type A/D converter (initial value)
1	Disable operating SA type A/D converter

Note:
- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 15, "Successive Approximation Type A/D Converter" for details of the successive approximation type A/D converter operation.

4.2.6 Block Control Register 6 (BLKCON6)

Address: 0F02EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON6	DTMF	DTME	—	—	DTMB	DTMA	DTM9	DTM8
R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON6 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DTMF** (bit 7)
  DTMF controls the operation of the TimerF.

DTMF	Description
0	Enable the operation of the TimerF (initial value).
1	Disable the operation of the TimerF.

- **DTME** (bit 6)
  DTME controls the operation of the TimerE.

DTME	Description
0	Enable the operation of the TimerE (initial value).
1	Disable the operation of the TimerE.

- **DTMB** (bit 3)
  DTMB controls the operation of the TimerB.

DTMB	Description
0	Enable the operation of the TimerB (initial value).
1	Disable the operation of the TimerB.

- **DTMA** (bit 2)
  DTMA controls the operation of the TimerA.

DTMA	Description
0	Enable the operation of the TimerA (initial value).
1	Disable the operation of the TimerA.

- **DTM9** (bit 1)
  DTM9 controls the operation of the Timer9.

DTM9	Description
0	Enable the operation of the Timer9 (initial value).
1	Disable the operation of the Timer9.

- **DTM8** (bit 0)
  DTMB controls the operation of the Timer 8.

DTM8	Description
0	Enable the operation of the Timer8 (initial value).
1	Disable the operation of the Timer8.

Note:
- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 8, "Timer" for details of the Timer operation.

4.2.7 Block Control Register 7 (BLKCON7)

Address: 0F02FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON7	—	—	—	—	—	—	—	DPWC
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON7 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

- **DPWC** (bit 0)
  DPWC controls the operation of the PWMC.

DPWC	Description
0	Enable the operation of the PWMC (initial value).
1	Disable the operation of the PWMC.

Note:

- If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
- Refer to Chapter 10, "PWM" for details of the Timer operation.

4.3 Description of Operation

4.3.1 Program Run Mode

The program run mode is the state where the CPU executes instructions sequentially.
At power-on reset, RESET_N pin reset, low level detection reset, VLS reset, or WDT overflow reset, the CPU executes instructions from the addresses that are set in addresses 0002H and 0003H of program memory (ROM) after the system reset mode is released.
At reset by the BRK instruction, the CPU executes instructions from the addresses that are set in the addresses 0004H and 0005H of the program memory after the system reset mode is released. However, when the value of the interrupt level bit (ELEVEL) of the program status word (PSW) is 02H or higher at execution of the BRK instruction (after the occurrence of the WDT interrupt), the CPU executes instructions from the addresses that are set in the addresses 0002H and 0003H.
For details of the BRK instruction and PSW, see the "nX-U8/100 Core Instruction Manual" and for the reset function, see Chapter 3, "Reset Function".

4.3.2 HALT Mode

The HALT mode is the state where the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the HALT mode is set.
When a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE0–IE7) is issued, the HLT bit is set to "0" on the falling edge of the next system clock (SYSCLK) and the HALT mode is returned to the program run mode released.
Figure 4-2 shows the operation waveforms in HALT mode.

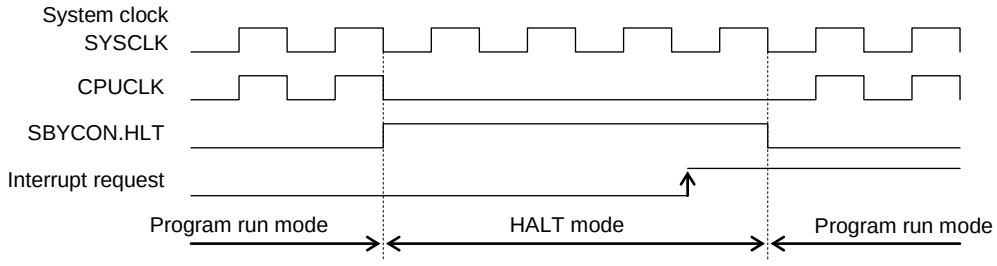


Figure 4-2 Operation Waveforms in HALT Mode

Note:
Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1".

4.3.3 STOP Mode

The STOP mode is the state where low-speed oscillation and high-speed oscillation stop and the CPU and peripheral circuits stop the operation.
When the stop code acceptor is enabled by writing "5nH" (n: an arbitrary value) and "0AnH" (n: an arbitrary value) to the stop code acceptor (STPACP) sequentially and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the stop code acceptor is disabled.
When a VLS interrupt request or an interrupt-enabled (the interrupt enable flag is "1") interrupt request is issued, the STP bit is set to "0", the STOP mode is released, and the mode is returned to the program run mode.

4.3.3.1 STOP Mode When CPU Operates with Low-Speed Clock

When the stop code acceptor is in the enabled state and the STP bit of SBYCON is set to "1", the STOP mode is entered, stopping low-speed oscillation and high-speed oscillation.
When interrupt-enabled (the interrupt enable flag is "1") interrupt request occurs, the STP bit is set to "0" and low-speed oscillation restarts. If the high-speed clock was oscillating before the STOP mode is entered, the high-speed oscillation restarts. When the high-speed clock was not oscillating before the STOP mode is entered, high-speed oscillation does not start.
When an interrupt request occurs, the STOP mode is released after counting low-speed clock(LSCLK) 32 times., the mode is returned to the program mode, and the low-speed clock(LSCLK) restarts supply to the peripheral circuits. If the high-speed clock already started oscillation at this time, the high-speed clocks (OSCLK and HSCLK) also restart supply to the peripheral circuits.
Figure 4-3 shows the operation waveforms in STOP mode when CPU operates with the low-speed clock.

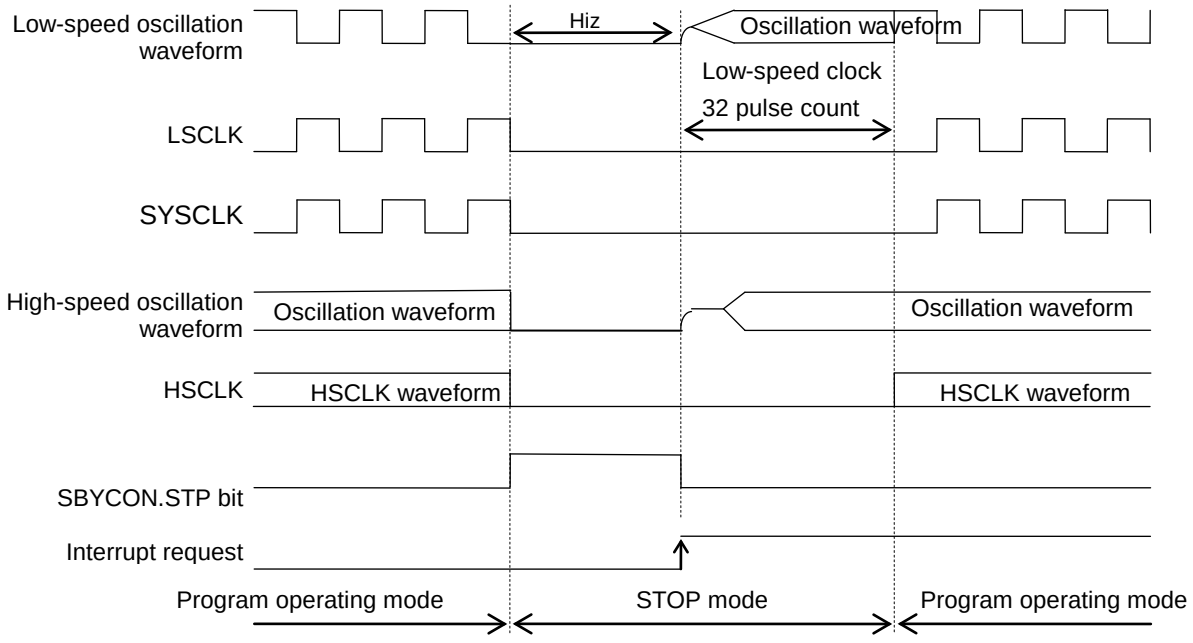


Figure 4-3 Operation Waveforms in STOP Mode When CPU Operates with Low-Speed Clock

4.3.3.2 STOP Mode When CPU Operates with High-Speed Clock

When the CPU is operating with a high-speed clock and the STP bit of SBYCON is set to "1" with the stop code acceptor enabled, the STOP mode is entered and high-speed oscillation and low-speed oscillation stop.
When interrupt-enabled (the interrupt enable flag is "1") interrupt request occurs, the STP bit is set to "0" and the low-speed and high-speed oscillation restart.
When an interrupt request is issued, the STOP mode is released after the elapse of the high-speed oscillation start time (T_{pll}) and the high-speed clock (OSCLK) oscillation stabilization time (8192-pulse count), the mode is returned to the program run mode, and the high-speed clocks (OSCLK and HSCLK) restart supply to the peripheral circuits.
The low-speed clock (LSCLK) restarts supply to the peripheral circuits after low-speed clock (LSCLK) oscillation stabilization time (32 count).
For the oscillation start time (T_{pll}), see the "Electrical Characteristics" Section in Appendix C.
Figure 4-4 shows the operation waveforms in STOP mode when CPU operates with the high-speed clock.

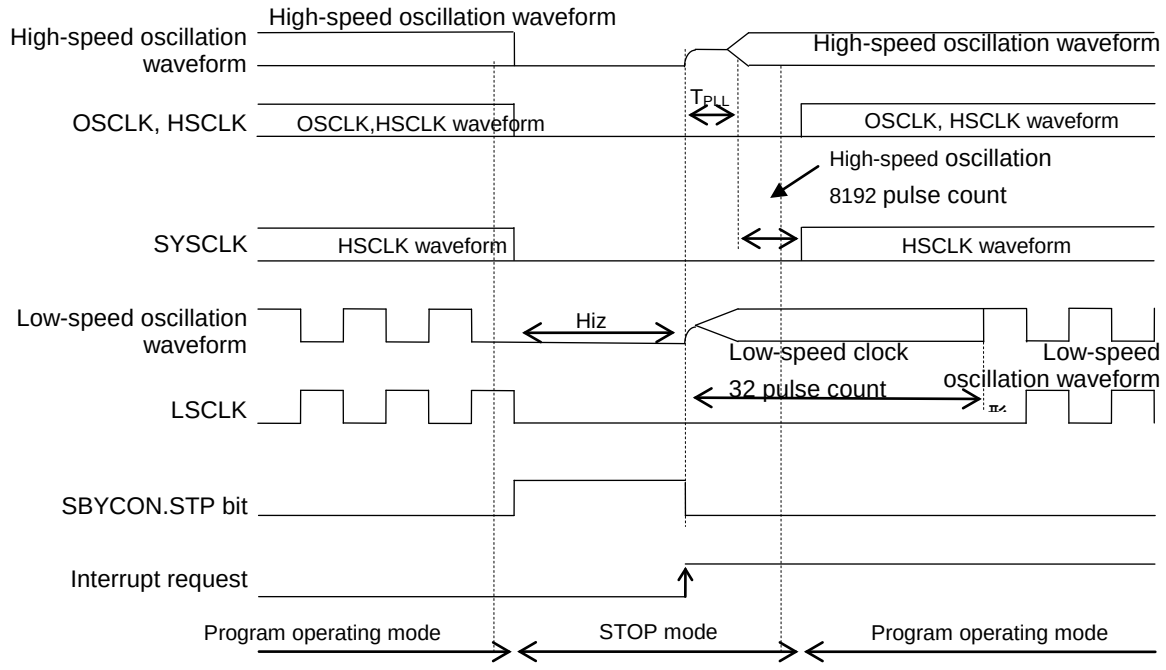


Figure 4-4 Operation Waveforms in STOP Mode When CPU Operates with High-Speed Clock

Note:
The STOP mode is entered two cycles after the instruction that sets the STP bit to "1" and up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing. Therefore, place two NOP instructions next to the instruction that set the STP bit to "1".

4.3.3.3 Note on Return Operation from STOP/HALT Mode

The operation of returning from the STOP mode and HALT mode varies according to the interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE0 to IE7), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U8/100 Core Instruction Manual" and Chapter 5, "Interrupt", respectively.

Table 4-1 and Table 4-2 show the return operations from STOP/HALT mode.

Table 4-1 Return Operation from STOP/HALT Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	–	0	Not returned from STOP/HALT mode.
3	*	–	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
0, 1, 2	*	–	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Table 4-2 Return Operation from STOP/HALT Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	*	0	Not returned from STOP/HALT mode.
*	*	0	1	
*	0	1	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
2,3	1	1	1	
0, 1	1	1	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Notes:
- If the ELEVEL bit is 0H, it indicates that the CPU is performing neither nonmaskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
- If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

4.3.4 Block Control Function

This LSI has a block control function, which resets and completely turns operating circuits of unused peripherals off to make even more reducing current consumption.

When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop. Writing to every SFR (special function register) in the corresponding peripherals is not valid while the bits of block control registers are set to "1" and returns the initial value for read. Ensure the bits are reset to "0" before using the peripherals to enable the operation.

BLKCON2 register controls (disables/enables) operation of UART.
BLKCON4 register controls (disables/enables) operation of SA type A/D converter.
BLKCON6 register controls (enables or disables) the operation of Timer.
BLKCON7 register controls (enables or disables) the operation of PWM.

Note:
- If the appropriate bit of the block register is set to "1", all relevant registers are initialized.
- Refer to the relevant chapter for details of operation or notes of each block.

Chapter 5

Interrupts (INTs)

5 Interrupts (INTs)

5.1 Overview

This LSI has 32 interrupt sources (External interrupts: 8 sources, Internal interrupts: 24 sources) and a software interrupt (SWI).
For details of each interrupt, see the following chapters:

Chapter 7, "Time Base Counter"
Chapter 8, "Timers"
Chapter 9, "Watchdog Timer"
Chapter 10, "PWM"
Chapter 11, "UART"
Chapter 12, "PortA"
Chapter 13, "PortB"
Chapter 15, "Successive Approximation Type A/D Converter"
Chapter 16, "Voltage Level Supervisor"
Chapter 17, "Analog Comparator"

5.1.1 Features

- 1 non-maskable interrupt sources (Internal source)
- 21 maskable interrupt sources (Internal sources: 16, External sources: 5)
- Software interrupt (SWI): 64 sources max.
- External interrupts allow edge selection and sampling selection.

5.2 Description of Registers

5.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F010H	Interrupt enable register 0	IE0	—	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H

5.2.2 Interrupt Enable Register 0 (IE0)

Address: 0F010H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE0	—	EVLS	—	—	—	—	—	—
R/W	R	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IE0 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE0 is not reset.

[Description of Bits]

- **EVLS** (bit 6)
  EVLS is the enable flag for the voltage level supervisor interrupt (VLSINT).

EVLS	Description
0	Disabled (initial value)
1	Enabled

5.2.3 Interrupt Enable Register 1 (IE1)

Address: 0F011H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE1	—	—	EPB1	EPB0	—	EPA2	EPA1	EPA0
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE1 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

[Description of Bits]

- **EPA0** (bit 0)
  EPA0 is the enable flag for the input/output port PA0 pin interrupt (PA0INT).

EPA0	Description
0	Disabled (initial value)
1	Enabled

- **EPA1** (bit 1)
  EPA1 is the enable flag for the input/output port PA1 pin interrupt (PA1INT).

EPA1	Description
0	Disabled (initial value)
1	Enabled

- **EPA2** (bit 2)
  EPA2 is the enable flag for the input/output port PA2 pin interrupt (PA2INT).

EPA2	Description
0	Disabled (initial value)
1	Enabled

- **EPB0** (bit 4)
  EPB0 is the enable flag for the input/output port PB0 pin interrupt (PB0INT).

EPB0	Description
0	Disabled (initial value)
1	Enabled

- **EPB1** (bit 5)
  EPB1 is the enable flag for the input/output port PB1 pin interrupt (PB1INT).

EPB1	Description
0	Disabled (initial value)
1	Enabled

5.2.4 Interrupt Enable Register 2 (IE2)

Address: 0F012H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE2	—	—	—	—	—	ESAD	—	—
R/W	R	R	R	R	R	R/W	R	R
Initial value	0	0	0	0	0	0	0	0

IE2 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE2 is not reset.

[Description of Bits]

- **ESAD** (bit 2)
  ESAD is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

ESAD	Description
0	Disabled (initial value)
1	Enabled

5.2.5 Interrupt Enable Register 3 (IE3)

Address: 0F013H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE3	—	—	—	—	ETM9	ETM8	—	—
R/W	R	R	R	R	R/W	R/W	R	R
Initial value	0	0	0	0	0	0	0	0

IE3 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE3 is not reset.

[Description of Bits]

- **ETM8** (bit 2)
  ETM8 is the enable flag for the timer 8 interrupt (TM8INT).

ETM8	Description
0	Disabled (initial value)
1	Enabled

- **ETM9** (bit 3)
  ETM9 is the enable flag for the timer 9 interrupt (TM9INT).

ETM9	Description
0	Disabled (initial value)
1	Enabled

5.2.6 Interrupt Enable Register 4 (IE4)

Address: 0F014H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE4	ECMP1	ECMP0	—	—	—	—	—	EUA0
R/W	R/W	R/W	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IE4 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE4 is not reset.

[Description of Bits]

- **EUA0** (bit 0)
  EUA0 is the enable flag for the UART0 interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

- **ECMP0** (bit 6)
  ECMP0 is the enable flag for the comparator0 interrupt (CMP0INT).

ECMP0	Description
0	Disabled (initial value)
1	Enabled

- **ECMP1** (bit 7)
  ECMP1 is the enable flag for the comparator1 interrupt (CMP1INT).

ECMP1	Description
0	Disabled (initial value)
1	Enabled

5.2.7 Interrupt Enable Register 5 (IE5)

Address: 0F015H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE5	ETMB	ETMA	ETMF	ETME	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IE5 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE5 is not reset.

[Description of Bits]

- **ETME** (bit 4)
  ETME the enable flag for the timer E interrupt (TMEINT).

ETME	Description
0	Disabled (initial value)
1	Enabled

- **ETMF** (bit 5)
  ETMF the enable flag for the timer F interrupt (TMFINT)

ETMF	Description
0	Disabled (initial value)
1	Enabled

- **ETMA** (bit 6)
  ETMA the enable flag for the timer A interrupt (TMAINT).

ETMA	Description
0	Disabled (initial value)
1	Enabled

- **ETMB** (bit 7)
  ETMB the enable flag for the timer B interrupt (TMBINT)

ETMB	Description
0	Disabled (initial value)
1	Enabled

5.2.8 Interrupt Enable Register 6 (IE6)

Address: 0F016H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE6	E32H	—	E128H	—	—	—	—	EPWC
R/W	R/W	R	R/W	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IE6 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE6 is not reset.

[Description of Bits]

- **EPWC** (bit 0)
  EPWC is the enable flag for the PWMC interrupt (PWCINT)

EPWC	Description
0	Disabled (initial value)
1	Enabled

- **E128H** (bit 5)
  E128H is the enable flag for the time base counter 128 Hz interrupt (T128HINT).

E128H	Description
0	Disabled (initial value)
1	Enabled

- **E32H** (bit 7)
  E32H is the enable flag for the time base counter 32 Hz interrupt (T32HINT).

E32H	Description
0	Disabled (initial value)
1	Enabled

5.2.9 Interrupt Enable Register 7 (IE7)

Address: 0F017H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE7	—	—	—	—	E2H	—	—	E16H
R/W	R	R	R	R	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IE7 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE7 is not reset.

[Description of Bits]

- **E16H** (bit 0)
  E16H is the enable flag for the time base counter 16 Hz interrupt (T16HINT).

E16H	Description
0	Disabled (initial value)
1	Enabled

- **E2H** (bit 3)
  E2H is the enable flag for the time base counter 2 Hz interrupt (T2HINT).

E2H	Description
0	Disabled (initial value)
1	Enabled

5.2.10 Interrupt Request Register 0 (IRQ0)

Address: 0F018H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ0	—	QVLS	—	—	—	—	—	QWDT
R/W	R	R/W	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ0 is a special function register (SFR) to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that do not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the Mask Interrupt Enable flag (MIE).
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated. By setting the IRQ0 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ0 is set to "0" by hardware when the interrupt request is accepted by the CPU.The factor

[Description of Bits]

- **QWDT** (bit 0)
  QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

- **QVLS** (bit 6)
  QVLS is the request flag for the volage level supervisor interrupt (VLSINT)

QVLS	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ0), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.11 Interrupt Request Register 1 (IRQ1)

Address: 0F019H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ1	—	—	QPB1	QPB0	—	QPA2	QPA1	QPA0
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ1 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ1 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ1 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QPA0** (bit 0)
  QPA0 is the request flag for the input port PA0 pin interrupt (PA0INT).

QPA0	Description
0	No request (initial value)
1	Request

- **QPA1** (bit 1)
  QPA1 is the request flag for the input port PA1 pin interrupt (PA1INT).

QPA1	Description
0	No request (initial value)
1	Request

- **QPA2** (bit 2)
  QPA2 is the request flag for the input port PA2 pin interrupt (PA2INT).

QPA2	Description
0	No request (initial value)
1	Request

- **QPB0** (bit 4)
  QPB0 is the request flag for the input port PB0 pin interrupt (PB0INT).

QPB0	Description
0	No request (initial value)
1	Request

- **QPB1** (bit 5)
  QPB1 is the request flag for the input port PB1 pin interrupt (PB1INT).

QPB1	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.12 Interrupt Request Register 2 (IRQ2)

Address: 0F01AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ2	—	—	—	—	—	QSAD	—	—
R/W	R	R	R	R	R	R/W	R	R
Initial value	0	0	0	0	0	0	0	0

IRQ2 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ2 request flag is set to "1" regardless of the IE2 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE2) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ2 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QSAD** (bit 2)
  QSAD is the request flag for the successive approximation type A/D converter interrupt (SADINT)

QSAD	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ2) or to the interrupt enable register (IE2), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.13 Interrupt Request Register 3 (IRQ3)

Address: 0F01BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ3	—	—	—	—	QTM9	QTM8	—	—
R/W	R	R	R	R	R/W	R/W	R	R
Initial value	0	0	0	0	0	0	0	0

IRQ3 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ3 request flag is set to "1" regardless of the IE3 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE3) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ3 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ3 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTM8** (bit 2)
  QTM8 is the request flag for the timer 8 interrupt (TM8INT).

QTM8	Description
0	No request (initial value)
1	Request

- **QTM9** (bit 3)
  QTM9 is the request flag for the timer 9 interrupt (TM9INT).

QTM9	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ3) or to the interrupt enable register (IE3), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.14 Interrupt Request Register 4 (IRQ4)

Address: 0F01CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ4	QCMP1	QCMP0	—	—	—	—	—	QUA0
R/W	R/W	R/W	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ4 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ4 request flag is set to "1" regardless of the IE4 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE4) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ4 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ4 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QUA0** (bit 0)
  QUA0 is the request flag for the UART0 interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

- **QCMP0** (bit 6)
  QCMP0 is the request flag for comparator0 interrupt (CMP0INT).

QCMP0	Description
0	No request (initial value)
1	Request

- **QCMP1** (bit 7)
  QCMP1 is the request flag for comparator1 interrupt (CMP1INT).

QCMP1	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ4) or to the interrupt enable register (IE4), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.15 Interrupt Request Register 5 (IRQ5)

Address: 0F01DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ5	QTMB	QTMA	QTMF	QTME	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

IRQ5 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ5 request flag is set to "1" regardless of the IE5 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE5) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ5 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ5 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QTME** (bit 4)
  QTME is the request flag for the timer E interrupt (TMEINT).

QTME	Description
0	No request (initial value)
1	Request

- **QTMF** (bit 5)
  QTMF is the request flag for the timer F interrupt (TMFINT).

QTMF	Description
0	No request (initial value)
1	Request

- **QTMA** (bit 6)
  QTMA is the request flag for the timer A interrupt (TMAINT).

QTMA	Description
0	No request (initial value)
1	Request

- **QTMB** (bit 7)
  QTMB is the request flag for the timer B interrupt (TMBINT).

QTMB	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ5) or to the interrupt enable register (IE5), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.16 Interrupt Request Register 6 (IRQ6)

Address: 0F01EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ6	Q32H	—	Q128H	—	—	—	—	QPWC
R/W	R/W	R	R/W	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ6 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ6 request flag is set to "1" regardless of the IE6 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE6) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ6 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ6 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QPWC** (bit 0)
  QPWC is the request flag for the PWMC interrupt (PWCINT).

QPWC	Description
0	No request (initial value)
1	Request

- **Q128H** (bit 5)
  Q128H is the request flag for the time base counter 128 Hz interrupt (T128HINT).

Q128H	Description
0	No request (initial value)
1	Request

- **Q32H** (bit 7)
  Q32H is the request flag for the time base counter 32 Hz interrupt (T32HINT).

Q32H	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ6) or to the interrupt enable register (IE6), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.17 Interrupt Request Register 7 (IRQ7)

Address: 0F01FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ7	—	—	—	—	Q2H	—	—	Q16H
R/W	R	R	R	R	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ7 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ7 request flag is set to "1" regardless of the IE7 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE7) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ7 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ7 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **Q16H** (bit 0)
  Q16H is the request flag for the time base counter 16 Hz interrupt (T16HINT).

Q16H	Description
0	No request (initial value)
1	Request

- **Q2H** (bit 3)
  Q2H is the request flag for the time base counter 2 Hz interrupt (T2HINT).

Q2H	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the instruction to write to the interrupt request register (IRQ7) or to the interrupt enable register (IE7), the the interrupt shift cycle starts after the next 1 instruction is executed.

5.3 Description of Operation

With the exception of the watchdog timer interrupt (WDTINT), interrupt enable/disable for 21 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to 7). WDTINT is non-maskable interrupts.
When the interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine.
Table 5-1 lists the interrupt sources.

Table 5-1 Interrupt Sources

Priority	Interrupt source	Symbol	Vector table address
1	Watchdog timer interrupt	WDTINT	0008H
3	Voltage level supervisor interrupt	VLSINT	000CH
5	PA0 interrupt	PA0INT	0010H
6	PA1 interrupt	PA1INT	0012H
7	PA2 interrupt	PA2INT	0014H
9	PB0 interrupt	PB0INT	0018H
10	PB1 interrupt	PB1INT	001AH
15	Successive approximation type A/D converter interrupt	SADINT	0024H
23	Timer 8 interrupt	TM8INT	0034H
24	Timer 9 interrupt	TM9INT	0036H
29	UART 0 interrupt	UA0INT	0040H
35	Comparator interrupt0	CMP0INT	004CH
36	Comparator interrupt1	CMP1INT	004EH
41	Timer E interrupt	TMEINT	0058H
42	Timer F interrupt	TMFINT	005AH
43	Timer A interrupt	TMAINT	005CH
44	Timer B interrupt	TMBINT	005EH
45	PWMC interrupt	PWCINT	0060H
50	TBC128Hz interrupt	T128HINT	006AH
52	TBC32Hz interrupt	T32HINT	006EH
53	TBC16Hz interrupt	T16HINT	0070H
56	TBC2Hz interrupt	T2HINT	0076H

Note:
- When multiple interrupts are generated concurrently, the interrupts are serviced according to this priority and processing of low-priority interrupts is pending.
- Please define vector tables for all unused interrupts for fail safe.

5.3.1 Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer the program counter (PC) to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW toEPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to"1".
(6) Load the interrupt start address into PC.

5.3.2 Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer PC to ELR2.
(2) Transfer CSR to ECSR2.
(3) Transfer PSW to EPSW2.
(4) Set the ELEVEL field to "2".
(5) Load the interrupt start address into PC.

5.3.3 Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1) Transfer PC to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW to EPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to "1".
(6) Load the interrupt start address into PC.

Reference:
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U8/100 Core Instruction Manual".

5.3.4 Notes on Interrupt Routine

Notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

State A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine

A-1-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  No specific notes.
- Processing at the end of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

A-1-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.

Example of description: State A-1-1

```
Intrpt_A-1-1;          ; A-1-1 state
   DI                  ; Disable interrupt
    :
    :
    :
   RTI                 ; Return PC from ELR
                       ; Return PSW form EPSW
                       ; End
```

Example of description: State A-1-2

```
Intrpt_A-1-2;          ; Start
   PUSH ELR, EPSW      ; Save ELR and EPSW at the
                         beginning
   EI                  ; Enable interrupt
    :
    :
    :
    :
    :
   POP PC, PSW         ; Return PC from the stack
                       ; Return PSW from the stack
                       ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine

A-2-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

A-2-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: A-2-2

```
Intrpt_A-2-2;          ; Start
   PUSH ELR, EPSW,     ; Save ELR, EPSW, LR at
   LR                    the beginning

   EI                  ; Enable interrupt
    :
    :
    :

   BL Sub_1            ; Call subroutine Sub_1
    :
   POP PC, PSW, LR     ; Return PC from the stack
                       ; Return PSW from the stack
                       ; Return LR from the stack
                       ; End
```

```
Sub_1;          ;
DI              ; Disable interrupt
                    :
                    :
                    :
RT              ; Return PC from LR
                ; End of subroutine
```

State B: Non-maskable interrupt is being processed

B-1: When a subroutine is not called

- Processing immediately after the start of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to PC and those of the EPSW register to PSW.

B-2: When a subroutine is called

B-2-1: When a subroutine is not called for an interruption routine to a run time by a program

- Processing immediately after the start of interrupt routine execution
  "PUSH ELR, EPSW" are specified and the return address of an interruption and the status of EPSW are evacuated to a stack.
- Processing at the end of interrupt routine execution
  Specifying "POP PC, PSW" instead of a RTI supervisor call, the save data of EPSW returns the save data of the return address of an interruption to PC at PSW. B-2-2: When a subroutine is called for an interruption routine to a run time by a program
- Processing immediately after the start of interrupt routine execution
  "PUSH LR, ELR, EPSW" are specified and the return address of an interruption, the return address of a subroutine, and the status of EPSW are evacuated to a stack.
- Processing at the end of interrupt routine execution
  Specifying "POP PC, PSW, LR" instead of a RTI supervisor call, as for the save data of the return address of an interruption, the save data of EPSW returns the save data of LR to LR to PC to PSW.

Example of description: State B-1

```
Intrpt_B-1;          ; B-1 state
   RTI               ; Return PC from ELR
                     ; Return PSW form EPSW
                     ; End
```

Example of description: State B-2-1

```
Intrpt_B-2-2;        ; Start
   PUSH ELR, EPSW    ; Save ELR and EPSW at the
                       beginning
   :
   :
   :
   POP PC, PSW       ; Return PC from the stack
                     ; Return PSW from the stack
                     ; End
```

Example of description: B-2-2

```
Intrpt_B-2-2;        ; Start
   PUSH ELR, EPSW,   ; Save ELR, EPSW, LR at
   LR                  the beginning
    :
    :
    :
   BL Sub_1          ; Call subroutine Sub_1
    :
   POP PC, PSW, LR   ; Return PC from the stack
                     ; Return PSW from the
                     stack
```

```
Sub_1;
                        :
                        :
                        :
RT                  ; Return PC from LR
                    ; End of subroutine
```

5.3.5 Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1: Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine
When the interrupt conditions are satisfied in this section, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2: Between the DSR prefix instruction and the next instruction
When the interrupt conditions are satisfied in this section, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

Reference:
For the DSR prefix instruction, see "nX-U8/100 Core Instruction Manual".

Chapter 6

Clock Generation Circuit

6 Clock Generation Circuit

6.1 Overview

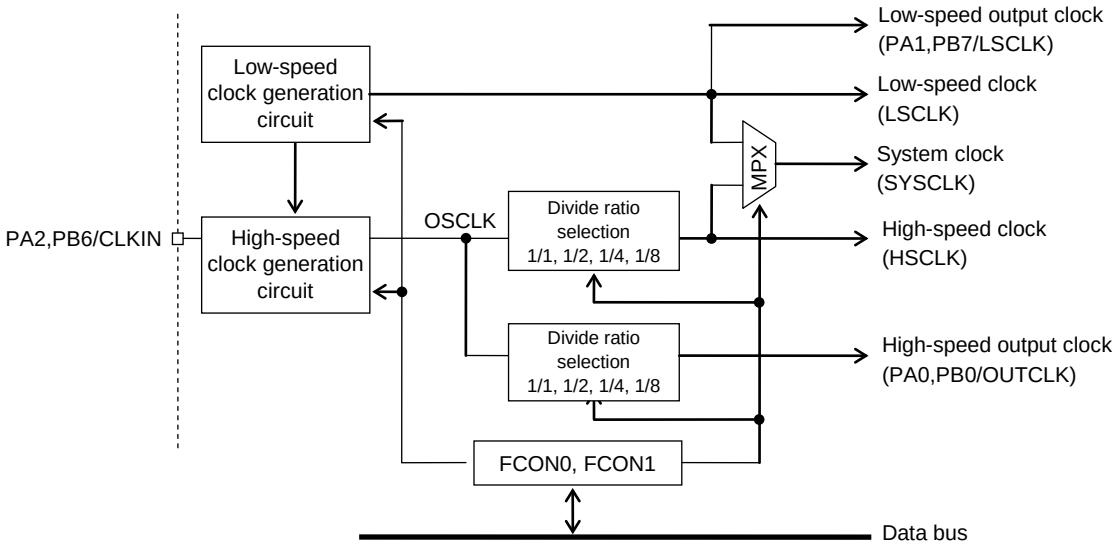
The clock generation circuit generates and provides a low-speed clock (LSCLK), a high-speed clock (HSCLK), a system clock (SYSCLK), and a high-speed output clock (OUTCLK). LSCLK, and HSCLK are time base clocks for the peripheral circuits, SYSCLK is a basic operation clock of CPU, and LSCLK/OUTCLK is a clock that is output from a port.
For the OUTCLK output port, see Chapter 12, "Port A" and Chapter 13, "Port B".
Additionally, for the STOP mode described in this chapter, see Chapter 4, "MCU Control Function".

6.1.1 Features

- Low-speed clock generation circuit:
  – Built-in RC oscillation (32.768kHz) mode
- High-speed clock: Software selection
  – Built-in PLL oscillation mode
  – External clock input mode

6.1.2 Configuration

Figure 6-1 shows the configuration of the clock generation circuit.



FCON0 : Frequency control register 0
FCON1 : Frequency control register 1

Figure 6-1 Configuration of Clock Generation Circuit

Note:
This LSI starts operation with the 32.768kHz RC oscillation clock after power-on or a system reset. At initialization by software, set the FCON0, FCON1 register to switch the clock to a required one.

6.1.3 List of Pins

Pin name	I/O	Description
PA0/OUTCLK	O	High-speed clock output pin Used for the tertiary function of the PA0 pin
PB0/OUTCLK	O	High-speed clock output pin Used for the tertiary function of the PB0 pin
PA2/CLKIN	I	External clock input pin Used for the tertiary function of the PA2 pin
PB6/CLKIN	I	External clock input pin Used for the secondary function of the PB6 pin
PA1/LSCLK	O	Low-speed clock output pin Used for the tertiary function of the PA1 pin
PB7/LSCLK	O	Low-speed clock output pin Used for the secondary function of the PB7 pin

6.2 Description of Registers

6.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	3BH
0F003H	Frequency control register 1	FCON1		R/W	8	00H

6.2.2 Frequency Control Register 0 (FCON0)

Address: 0F002H
Access: R/W
Access size: 8/16 bits
Initial value: 3BH

	7	6	5	4	3	2	1	0
FCON0	—	—	OUTC1	OUTC0	OSCM1	OSCM0	SYSC1	SYSC0
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	1	1	1	0	1	1

FCON0 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock. OSCM1 always returns the value "1".

[Description of Bits]

- **SYSC1, SYSC0** (bits 1, 0)
  The SYSC1 and SYSC0 bits are used to select the frequency of the high-speed clock (HSCLK) used for system clock and peripheral circuits (including high-speed time base counter). OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected. The maximum operating frequency guaranteed for the system clock (SYSCLK) of this LSI is 8.192MHz.
  At system reset, 1/8OSCLK is selected.

SYSC1	SYSC0	Description
0	0	OSCLK (1/2OSCLK in built-in PLL oscillation mode)
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

- **OSCM0** (bits 2)
  The OSCM0 bits are used to select the mode of the high-speed clock generation circuit. PLL oscillation mode, or external clock input mode can be selected.
  The setting of OSCM0 can be changed only when high-speed oscillation is being stopped (ENOSC bit of FCON1 is "0"). At system reset, PLL oscillation mode is selected.
  When switching the high-speed oscillation mode, please first switch back to low speed clock before switching to other high-speed clock (set the ENOSC bit and SYSCLK bit of FCON1 to "0").

OSCM0	Description
0	Built-in PLL oscillation mode(initial value)
1	External clock input mode(PA2,PB6/CLKIN)

- **OUTC1, OUTC0** (bits 5, 4)
  The OUTC1 and OUTC0 bits are used to select the frequency of the high-speed output clock which is output when the tertiary function of PA0 pin, PB0 pin are used.
  OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

OUTC1	OUTC0	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

Note:
- To switch the mode of the high-speed clock generation circuit using the OSCM0 bits, stop the high-speed oscillation and set the system clock to the low-speed clock (set the ENOSC bit and SYSCLK of FCON1 to "0").
- In external clock mode, an external clock is input from the PA2/CLKIN, PB6/CLKIN pin. And in external clock mode, input a clock that does not exceed 8.192 MHz.
- In external clock mode, when using PA2/CLKIN and PB6/CLKIN as external clock input pin, PA2/CLKIN has the higher priority.

6.2.3 Frequency Control Register 1 (FCON1)

Address: 0F003H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FCON1	LPLL	—	—	—	—	—	ENOSC	SYSCLK
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FCON1 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

- **SYSCLK** (bit 0)
  The SYSCLK bit is used to select system clock. It allows selection of the low-speed clock (LSCLK) or HSCLK (1/nOSCLK: n = 1, 2, 4, 8) selected by using the high-speed clock frequency select bit (SYSC1, 0) of FCON0.
  When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK (initial value)
1	HSCLK

- **ENOSC** (bit 1)
  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator.

ENOSC	Description
0	Disables high-speed oscillation (initial value)
1	Enables high-speed oscillation

- **LPLL** (bit 7)
  The LPLL bit is used as a flag to indicate the oscillation state of PLL oscillation.
  When the LPLL bit is set to "1", this indicates that the PLL oscillation frequency is locked within 16.384 MHz±1.0%.
  When the LPLL bit is set to "0", this indicates that the PLL oscillation is inactive or the PLL oscillation frequency is not within 16.384 MHz±1.0%.
  LPLL is a read-only bit.

LPLL	Description
0	Disables the use of PLL oscillation (initial value)
1	Enables the use of PLL oscillation

Note:
– LPLL flag is a reference flag. The oscillation stabilization time for 3ms (max) is required after PLL oscillation starting.
– Although the oscillated frequency of PLL is 16.384MHz, a CPU clock is a maximum of 8.192MHz.

6.3 Description of Operation

6.3.1 Low-Speed Clock

6.3.1.1 Low-Speed Clock Generation Circuit (built-in RC oscillating circuit)

Figure 6-2 shows the circuit configuration of the low-speed clock generation circuit.
The 32.768kHz RC oscillation clock generation circuit is activated by the occurrence of power ON reset or port reset or WDT reset. In starting by reset, after waiting oscillation stable time (256 counts), the clock is supplied to the peripheral circuit. In the return from a STOP mode, after waiting oscillation stable time(32 coounts), a clock is supplied to a peripheral circuit.

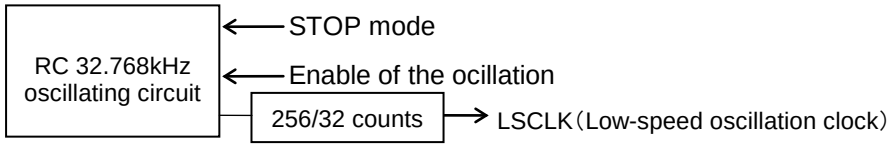


Figure 6-2 Circuit Configuration of RC 32.768 kHz Oscillation Mode

6.3.1.2 Operation of Low-Speed Clock Generation Circuit

The low-speed clock generation circuit is activated by the occurrence of power-on reset.
The low-speed clock (LSCLK) is supplied to the peripheral circuits after a lapse of the low-speed clock oscillation stabilization period (256 counts) after power-on.
When the low-speed clock generation circuit shifts to STOP mode by software, it stops oscillation. It resumes oscillation when the STOP mode is released by an external interrupt. Then, LSCLK is supplied to the peripheral circuits after a lapse of the low-speed clock oscillation stabilization period (32 counts). For STOP mode, see Chapter 4, "MCU Control Function".
Figure 6-3 shows the waveforms of the low-speed clock generation circuit.

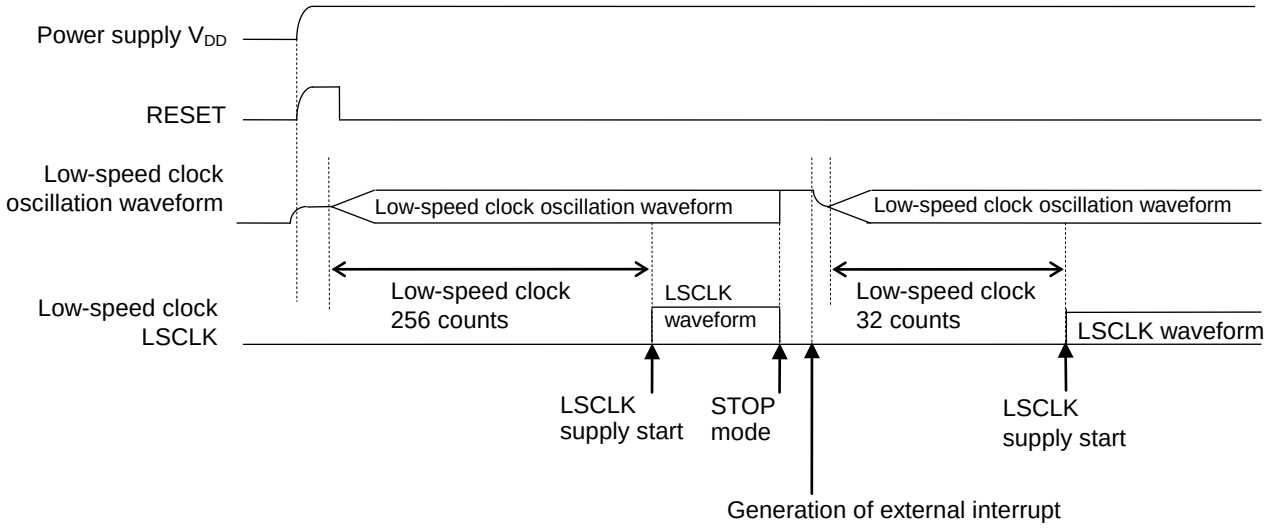


Figure 6-3 Operation of Low-Speed Clock Generation Circuit

Note:
After the power supply is turned on, CPU starts operation with a low-speed clock (RC 32.768kHz oscillation).

6.3.2 High-Speed Clock

For the high-speed clock generation circuit, built-in PLL oscillation mode or external clock input mode can be selected.

6.3.2.1 Built-in PLL Oscillation Mode

The PLL oscillation circuit generates a clock of 16.384 MHz ±1.0% (= 32.768 kHz × 512).
When the frequency of a PLL oscillation clock is less than 8.192MHz ± 1.0%, the LPLL flag of FCON1 is set to "1."
In built-in PLL oscillation mode (OSCM0 = "0", OSCM1 = "1"), supply of OSCLK (high-speed oscillation clock) is started when PLL oscillation clock pulse count reaches 8192 after oscillation is enabled (ENOSC is set to "1").
In PLL oscillation mode, both the PA2,PB6/CLKIN pin can be used as general-purpose input ports.
Figure 6-4 shows the circuit configuration in PLL oscillation mode.

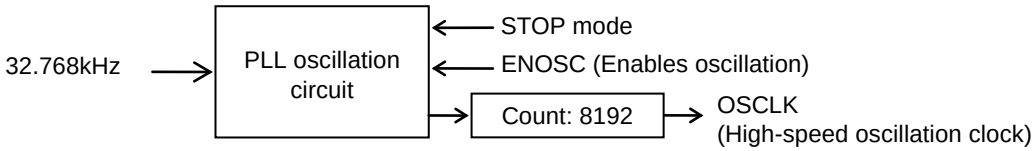


Figure 6-4 Circuit Configuration in PLL Oscillation Mode

6.3.2.2 High-Speed External Clock Input Mode

In high-speed external clock input mode, an external clock is input from the P10/OSC0 pin.
When set as external clock input mode(OSCM0="1", OSCM1="1"), supply of OSCLK is started after permitting an oscillation(ENOSC is set to "1.") and counting an external input clock 128 times.
Figure 6-5 shows the circuit configuration in high-speed external clock input mode.

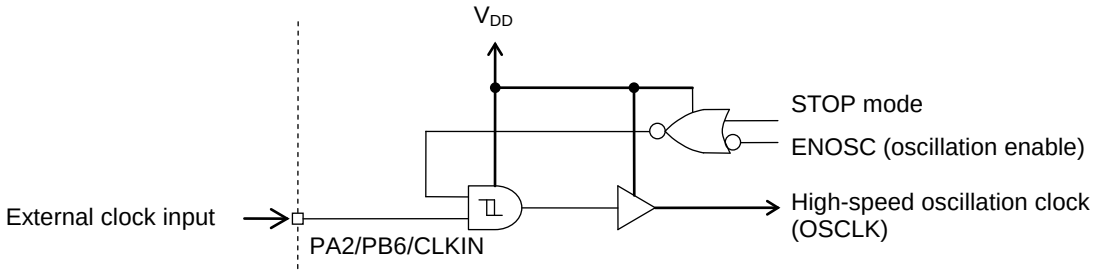


Figure 6-5 Circuit Configuration in High-Speed External Clock Input Mode

Notes:
- High-speed external clock input mode can be used within the limits of VDD=2.7V to 5.5V.
- If the PA2,PB6/CLKIN pin is left open in high-speed external clock input mode, excessive current can flow. Therefore, be sure to input a "H" level (DV_{DD}) or a "L" level (DV_{SS}) to the P10/OSC0 pin.
- The clock that is input must not exceed 8.192 MHz, the guaranteed maximum operating frequency of the system clock (SYSCLK) of this LSI.
- In external clock input mode, priority is given to PA2 when both PA2 and PB6 are set as a clock input pin

6.3.2.3 Operation of High-Speed Clock Generation Circuit

For the high-speed clock generation circuit, the chice of the oscillation mode and starting/stopping oscillation can be controlled by the frequency control register 0,1 (FCON0,1).
After selecting high-speed oscillation mode and its frequency in FCON0, the oscillation will be started if the ENOSC bit of FCON1 is set to "1." After an oscillation start, after waiting the oscillation stabilization period (T_{WAIT}) of a high-speed oscillation clock(OSCLK) in each mode, HSCLK begins to be supplied to a peripheral circuit.
The high-speed clock generation circuit stops oscillation when it enters STOP mode by software. When a STOP mode is canceled by external interruption and an oscillation restarts, after waiting the oscillation stabilization period (T_{WAIT}) of a high-speed oscillation(OSCLK) clock in each mode, HSCLK begins to be supplied to a peripheral circuit. The oscillation stabilization period (T_{WAIT}) is the duration of 128 clock pulses in high-speed external clock input mode and the duration of 8192 clock pulses in PLL oscillation mode.

Figure 6-6 shows the waveforms of the high-speed clock generation circuit in bult-in PLL oscillation mode.

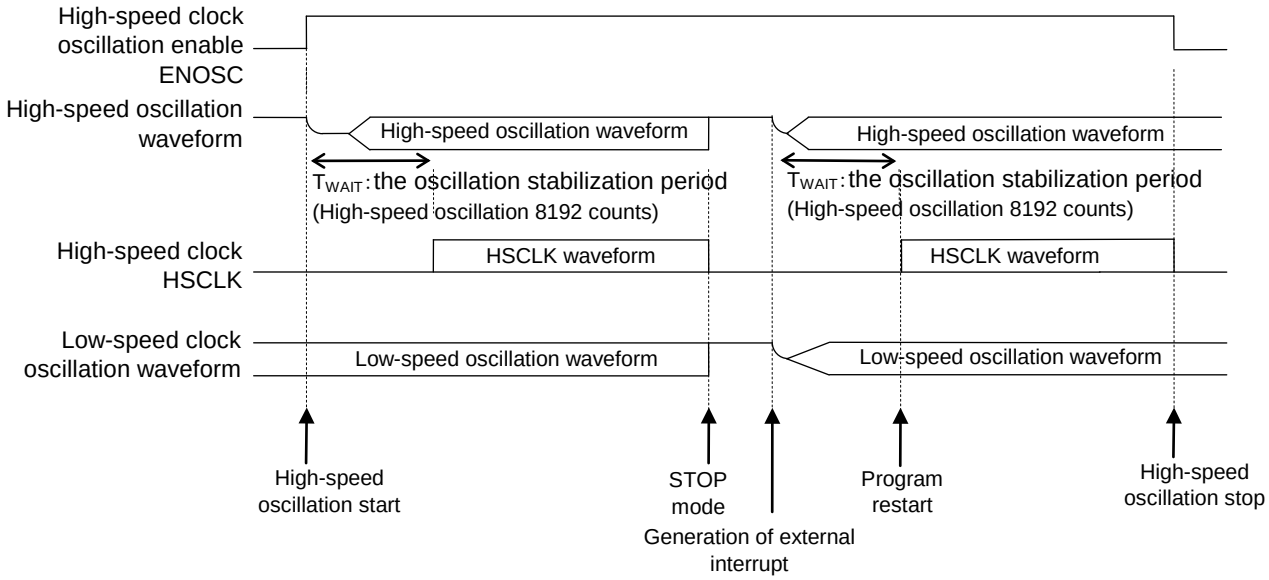


Figure 6-6 Operation of the High-Speed Clock Generation Circuit at Power-On

6.3.3 Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 6-7 shows a flow of system clock switching processing (HSCLK→LSCLK) and Figure 6-8 shows a flow of system clock switching processing (LSCLK→HSCLK).

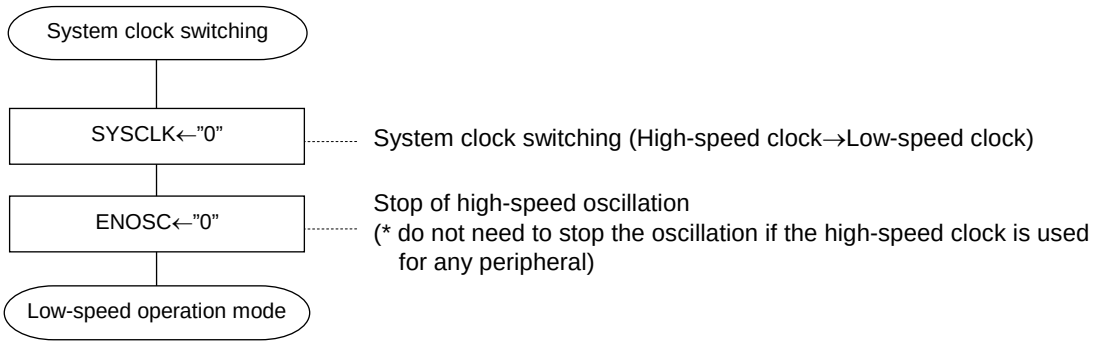


Figure 6-7 Flow of System Clock Switching Processing (HSCLK→LSCLK)

Note:
After power is turned on or if the system clock is switched from HSCLK to LSCLK immediately following return from the STOP mode, the CPU becomes inactive until LSCLK starts clock supply to the peripheral circuits. Therefore, It is recommended to switch to LSCLK after confirming that the LSCLK is oscillating by checking that the time-base counter interrupt request bit (Q128H) is "1".

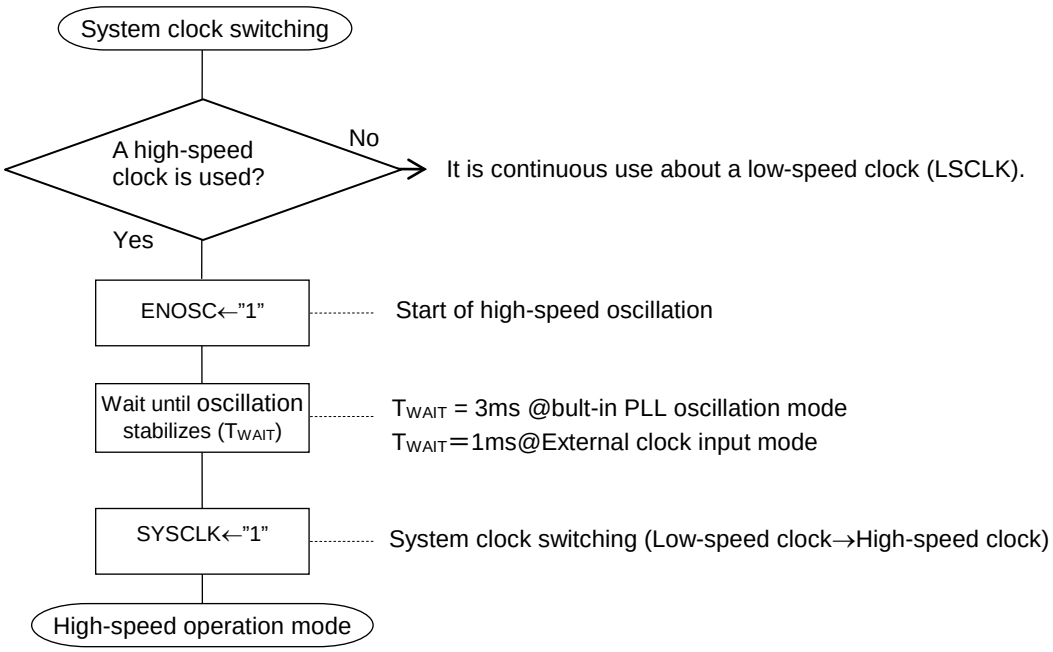


Figure 6-8 Flow of System Clock Switching Processing (LSCLK→HSCLK)

Note:
If the system clock is switched from a low-speed clock to a high-speed clock before the high-speed clock (HSCLK) starts oscillation, the CPU becomes inactive until HSCLK starts clock supply to the peripheral circuits.

6.4 Specifying port registers

For enable a clock output function, each related port register needs to be set up. Refer to the Chapter 12, "Port A" and the Chapter 13 "Port B" for details of each register.

6.4.1 Functioning PB7 (LSCLK) as the low speed clock output

Set PB7MD0 bit (bit7 of PBMOD0 register) to "1" for specifying the low speed clock output as the secondary function of PB7.

Reg. name	PBMOD0 register (Address: 0F25DH)							
Bit	**7**	6	**5**	4	3	2	1	0
Bit name	**PB7MD1**	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Data	**0**	*	*	*	*	*	*	*

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	**7**	6	**5**	4	3	2	1	0
Bit name	**PB7MD0**	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Data	**1**	*	*	*	*	*	*	*

Set PB7C1 bit (bit7 of PBCON1 register) to "1" and set PB7C0 bit(bit7 of PBCON0 register) to "1", and set PB7DIR bit(bit7 of PBDIR register) to "0"for specifying the PB7 as CMOS output.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C1**	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C0**	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBDIR register (Address: 0F259H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7DIR**	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Data	**0**	*	*	*	*	*	*	*

Data of PB7D bit (bit7 of PBD register) does not affect to the high speed clock output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7D**	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	PB0D
Data	******	*	*	*	*	*	*	*

- : Bit does not exist.
* : Bit not related to the high speed clock function
** : Don't care the data.

6.4.2 Functioning PB0 (OUTCLK) as the High speed clock output

Set PB0MD0 bit (bit0 of PBMOD1 register) to "1" for specifying the low speed clock output as the tertiary function of PB0.

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	**5**	4	3	2	1	**0**
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	**PB0MD1**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	**5**	4	3	2	1	**0**
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	**PB0MD0**
Data	*	*	*	*	*	*	*	**0**

Set PB0C1 bit (bit0 of PBCON1 register) to "1" and set PB0C0 bit(bit0 of PBCON0 register) to "1", and set PB0DIR bit(bit0 of PBDIR register) to "0"for specifying the PB0 as CMOS output.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C1	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	PB1C1	**PB0C1**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	**PB0C0**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBDIR register (Address: 0F259H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7DIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	**PB0DIR**
Data	*	*	*	*	*	*	*	**0**

Data of PB0D bit (bit0 of PBD register) does not affect to the high speed clock output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	**PB0D**
Data	*	*	*	*	*	*	*	******

- : Bit does not exist.
* : Bit not related to the high speed clock function
** : Don't care the data.

Chapter 7

Time Base Counter

7 Time Base Counter

7.1 Overview

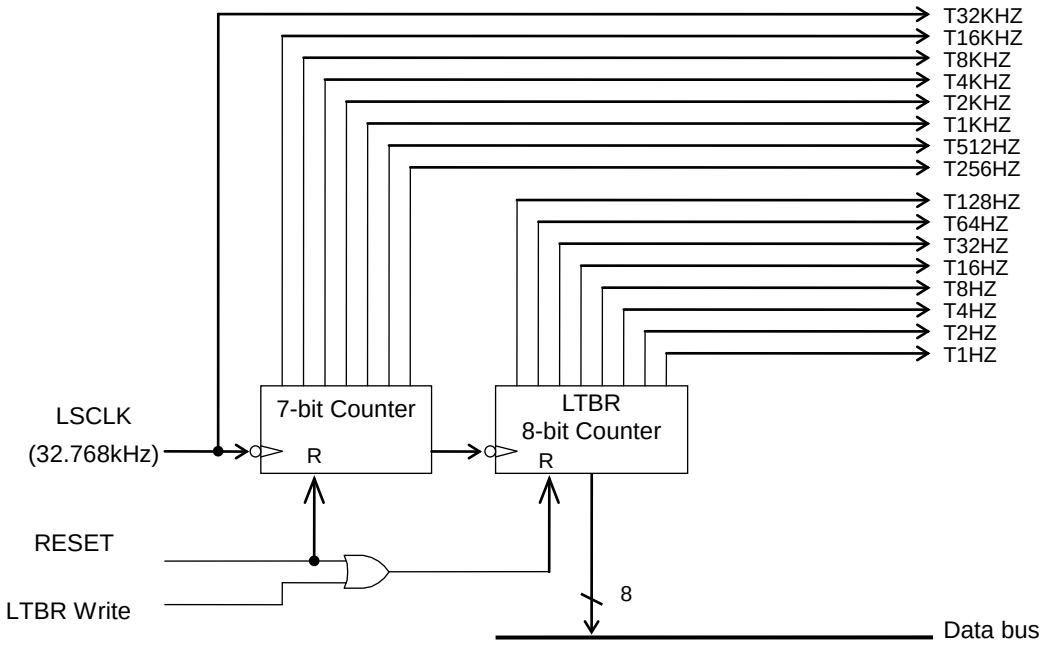
This LSI includes a low-speed time base counter (LTBC) and a high-speed time base counter (HTBC) that generate base clocks for peripheral circuits. By using the time base counter, it is possible to generate events periodically.
For input clocks, see Chapter 6, "Clock Generation Circuit". For interrupt permission, interrupt request flags, etc., described in this chapter, see Chapter 5, "Interrupts".

7.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK) frequency.
- HTBC generates HTB1 to HTB32 signals by dividing the high-speed clock (HSCLK) frequency.
- Capable of generating 128Hz , 32Hz , 16Hz , and 2Hz interrupts.

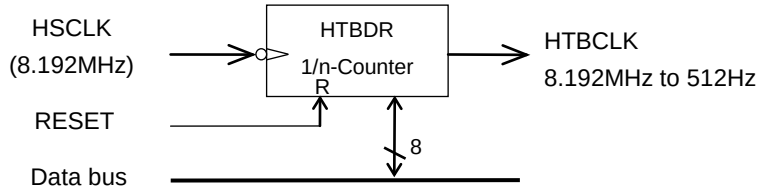
7.1.2 Configuration

Figure 7-1 and Figure 7-2 show the configuration of a low-speed time base counter and a high-speed time base counter, respectively.



LTBR: Low-speed time base counter register

Figure 7-1 Configuration of Low-Speed Time Base Counter (LTBC)



HTBDR: High-speed time base counter frequency divide register

Figure 7-2 Configuration of High-Speed Time Base Counter

Note:
The frequency of HSCLK is changed by setting of SYSC1 bit and SYSC0 bit in the frequency control register 0 (FCON0).

7.2 Description of Registers

7.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00AH	Low-speed time base counter register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter frequency divide register	HTBDR	—	R/W	8	00H

7.2.2 Low-Speed Time Base Counter (LTBR)

Address: 0F00AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ-T1HZ outputs of the low-speed time base counter. The T128HZ-T1HZ outputs are set to "0" when write operation is performed for LTBR.

Note:
A TBC interrupt (128Hz interrupt, 32Hz interrupt, 16Hz interrupt, or 2Hz interrupt) may occur depending on the LTBR write timing (see Figure 7-4, "Interrupt Timing and Reset Timing by Writing to LTBR"). Therefore, take care in software programming, refer to Figure 7-4, "Interrupt Timing and Reset Timing by Writing to LTBR".

7.2.3 High-Speed Time Base Counter Divide Register (HTBDR)

Address: 0F00BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
HTBDR	—	—	—	—	HTD3	HTD2	HTD1	HTD0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

HTBDR is a special function register (SFR) to set the divide ratio of the 4-bit, 1/n counter.

[Description of Bits]

- **HTD3 to HTD0** (bits 3-0)
  The HTD3-HTD0 bits are used to set the frequency divide ratio of the 4-bit, 1/n counter. The frequency divide ratios selectable include 1/1 to 1/16.

HTD3	HTD2	HTD1	HTD0	Description	
				Divide ratio	Frequency of HTBCLK (*1)
0	0	0	0	× 1/16 (initial value)	512 kHz
0	0	0	1	× 1/15	546 kHz
0	0	1	0	× 1/14	586 kHz
0	0	1	1	× 1/13	630 kHz
0	1	0	0	× 1/12	682 kHz
0	1	0	1	× 1/11	744 kHz
0	1	1	0	× 1/10	820 kHz
0	1	1	1	× 1/9	910 kHz
1	0	0	0	× 1/8	1024 kHz
1	0	0	1	× 1/7	1170 kHz
1	0	1	0	× 1/6	1366 kHz
1	0	1	1	× 1/5	1638 kHz
1	1	0	0	× 1/4	2048 kHz
1	1	0	1	× 1/3	2730 kHz
1	1	1	0	× 1/2	4096 kHz
1	1	1	1	× 1/1	8192 kHz

*1: Indicates the frequency when the high-speed oscillation clock, HSCLK, is 8192 kHz.

7.3 Description of Operation

7.3.1 Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
The T128HZ, T32HZ, T16HZ, and T2HZ outputs of LTBC are used as time base interrupts and an interrupt is requested on the falling edge of each output. Each of LTBC outputs is also used as an operation clock for peripheral circuits.
The output data of T128HZ to T1HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 7-3 shows an example of program to read LTBR.

```
        LEA     offset LTBR         ; EA←LTBR address
MARK:
        L       R0,     [EA]        ; 1st read
        L       R1,     [EA]        ; 2nd read
;
        CMP     R0,     R1          ; Comparison for LTBR
        BNE     MARK                ; To MARK when the values do not coincide
;
          :
```

Figure 7-3 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". Write data is invalid. Since an interrupt occurs if a falling edge occurs in the T128Hz to T1Hz outputs during writing to LTBR, take care in software programming.
Figure 7-4 shows interrupt generation timing and reset timing of the time base counter output by writing to LTBR.

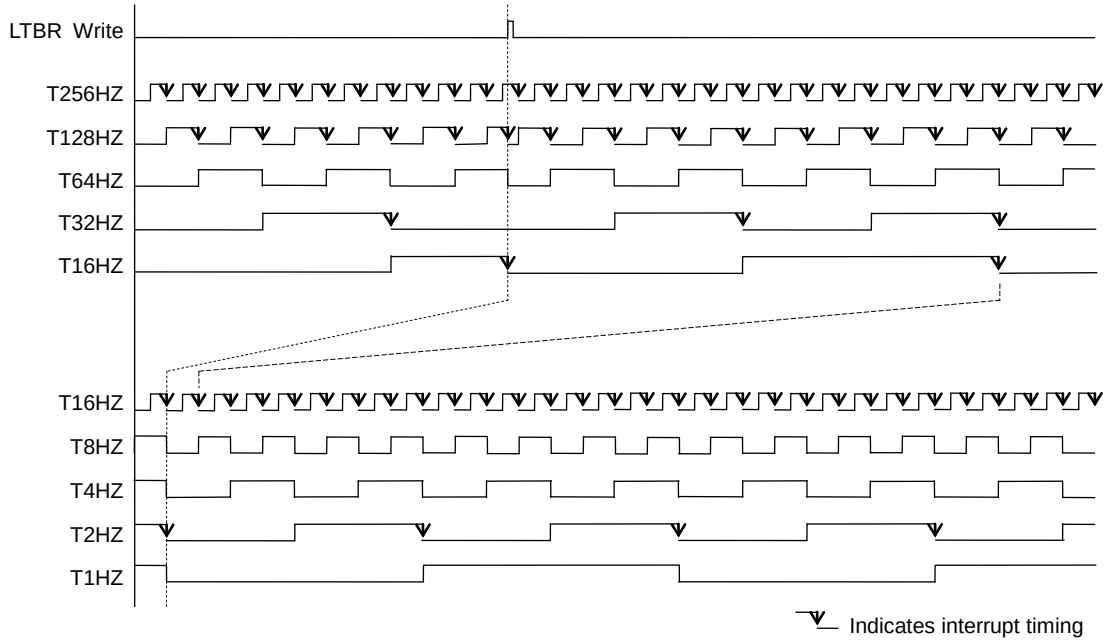


Figure 7-4 Interrupt Timing and Reset Timing by Writing to LTBR

7.3.2 High-Speed Time Base Counter

The high-speed time base counter is configured as a 4-bit 1/n counter (n = 1 to 16).
In the 4-bit 1/n counter, the divided clock (1/16×HSCLK to 1/1×HSCLK) selected by the high-speed time base counter divide register (HTBDR) is generated as HTBCLK. HTBCLK is used as a timer and also as an operation clock of PWM.
Figure 7-5 shows the output waveform of HTBCLK.

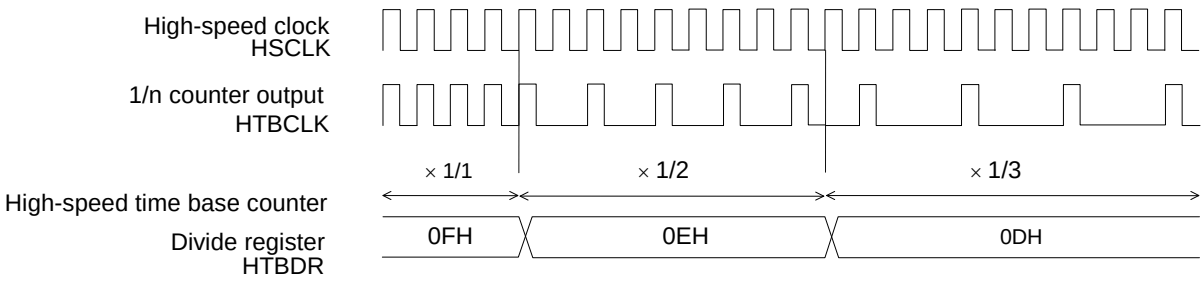


Figure 7-5 Output Waveform of HTBCLK

Chapter 8

Timers

8 Timers

8.1 Overview

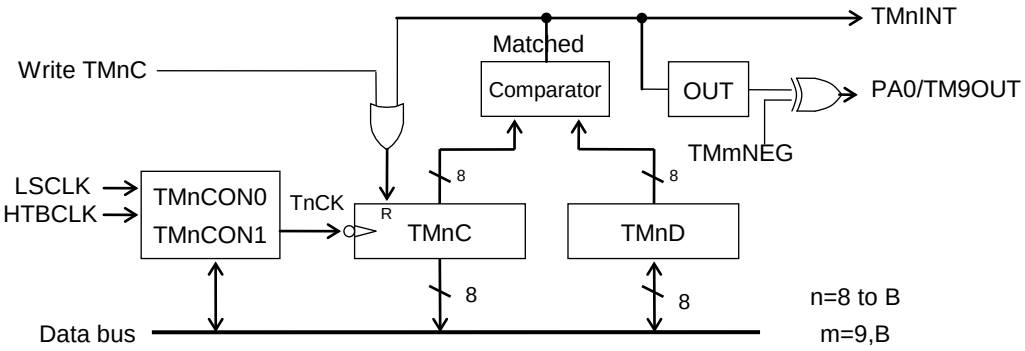
This LSI includes 6 channels of 8-bit timers.
For the input clock, see Chapter 6, "Clock Generation Circuit".

8.1.1 Features

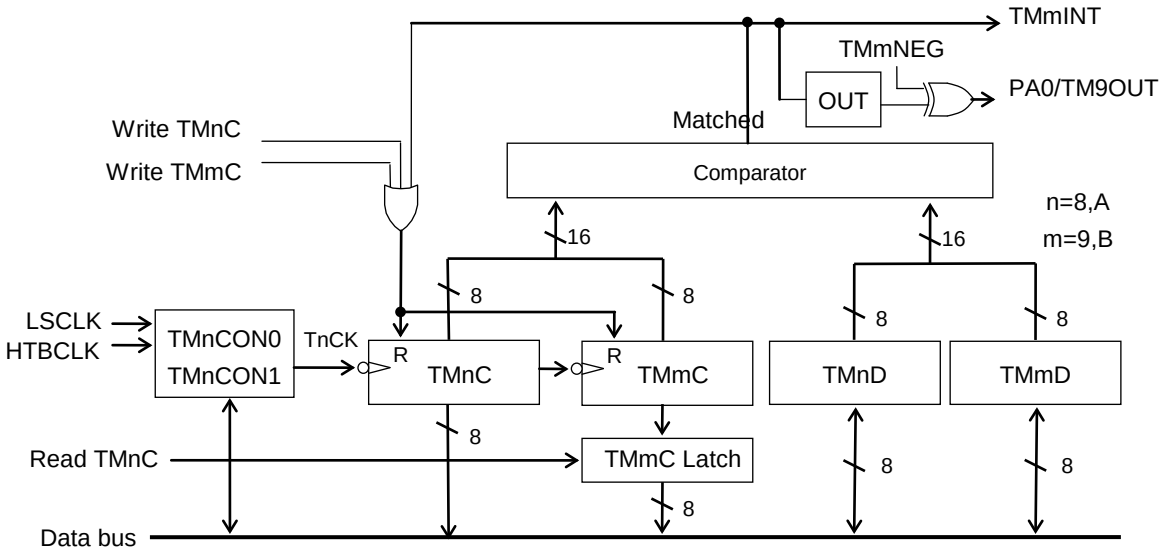
- The timer interrupt (TMnINT) is generated when the values of timer counter register (TMnC, n=8 to B, E, F) and timer data register (TMnD) coincide.
- A timer configured by combining timer 8 and timer 9 or timer A and timer B or timer E and timer F can be used as a 16-bit timer.
- For the timer clock, the low-speed clock (LSCLK), high-speed time base clock (HTBCLK) can be selected.
- The timer out signal of a timer 9 and Timer F (TM9OUT, TMFOUT) can be outputted.
- Positive logic or negative logic can be selected for the output logic of TM9OUT, TMFOUT signal.
- Auto reload timer mode and one shot timer mode can be selected.
- Timer E and Timer F can be started and stopped by the external trigger input.

8.1.2 Configuration

Figure 8-1 shows the configuration of the timers



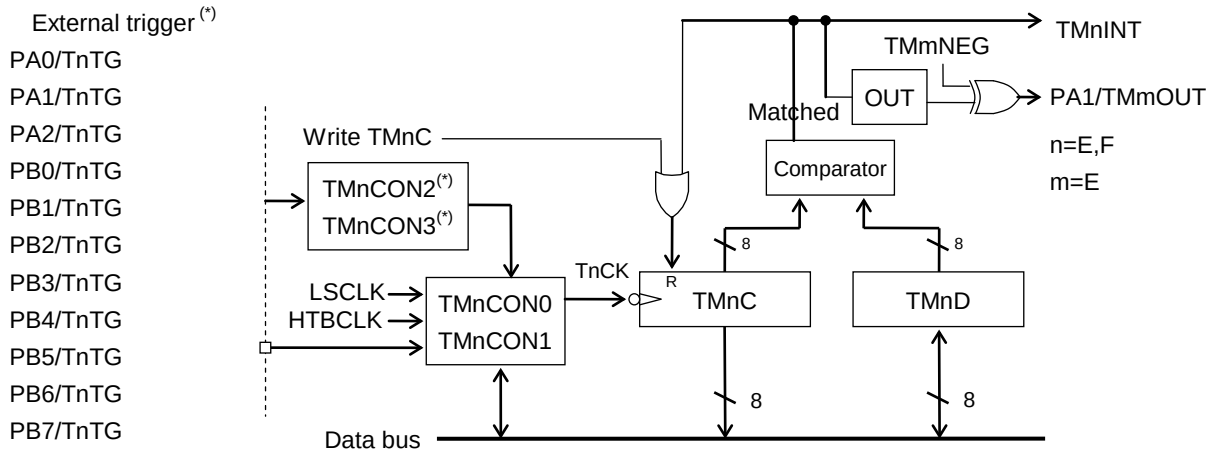
（a）In 8-bit Timer Mode（Timers 8 to B）



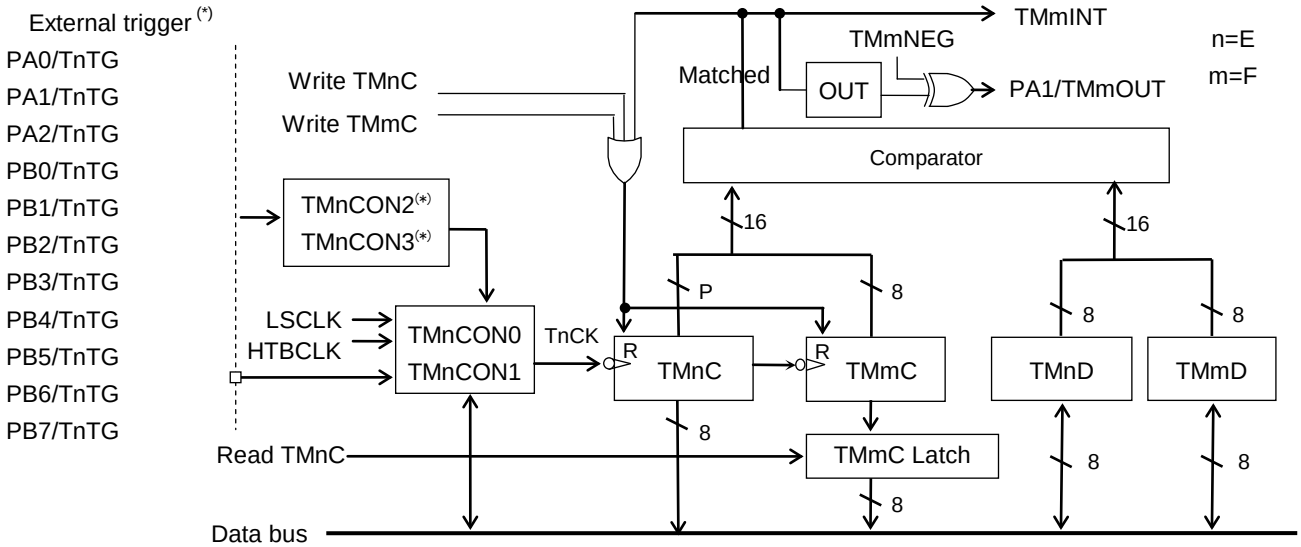
（b）In 16-bit Timer Mode（Timer 8 to B）

TMnCON0 : Timer control register 0
TMnCON1 : Timer control register 1
TMmD、TMnD : Timer data register
TMmC、TMnC : Timer counter register

Figure 8-1 the configuration of timers



（c） In 8-bit Timer Mode（Timer E, F）



TMnCON0 : Timer control register 0
TMnCON1 : Timer control register 1
TMnCON2 : Timer control register 2
TMnCON3 : Timer control register 3
TMmD、TMnD : Timer data register
TMmC、TMnC : Timer counter register

（d）In 16-bit Timer Mode（Timer E, F）

Figure 8-1 the configuration of timers

8.2 Description of Registers

8.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F8E0H	Timer 8 data register	TM8D	TM8DC	R/W	8/16	0FFH
0F8E1H	Timer 8 counter register	TM8C		R/W	8	00H
0F8E2H	Timer 8 control register 0	TM8CON0	TM8CON	R/W	8/16	00H
0F8E3H	Timer 8 control register 1	TM8CON1		R/W	8	00H
0F8E4H	Timer 9 data register	TM9D	TM9DC	R/W	8/16	0FFH
0F8E5H	Timer 9 counter register	TM9C		R/W	8	00H
0F8E6H	Timer 9 control register 0	TM9CON0	TM9CON	R/W	8/16	00H
0F8E7H	Timer 9 control register 1	TM9CON1		R/W	8	00H
0F8E8H	Timer A data register	TMAD	TMADC	R/W	8/16	0FFH
0F8E9H	Timer A counter register	TMAC		R/W	8	00H
0F8EAH	Timer A control register 0	TMACON0	TMACON	R/W	8/16	0A0H
0F8EBH	Timer A control register 1	TMACON1		R/W	8	00H
0F8ECH	Timer B data register	TMBD	TMBDC	R/W	8/16	0FFH
0F8EDH	Timer B counter register	TMBC		R/W	8	00H
0F8EEH	Timer B control register 0	TMBCON0	TMBCON	R/W	8/16	00H
0F8EFH	Timer B control register 1	TMBCON1		R/W	8	00H
0F360H	Timer E data register	TMED	TMEDC	R/W	8/16	0FFH
0F361H	Timer E counter register	TMEC		R/W	8	00H
0F362H	Timer E control register 0	TMECON0	TMECON	R/W	8/16	00H
0F363H	Timer E control register 1	TMECON1		R/W	8	00H
0F364H	Timer E control register 2	TMECON2	TMECON23	R/W	8/16	00H
0F365H	Timer E control register 3	TMECON3		R/W	8	00H
0F368H	Timer F data register	TMFD	TMFDC	R/W	8/16	0FFH
0F369H	Timer F counter register	TMFC		R/W	8	00H
0F36AH	Timer F control register 0	TMFCON0	TMFCON	R/W	8/16	00H
0F36BH	Timer F control register 1	TMFCON1		R/W	8	00H
0F36CH	Timer F control register 2	TMFCON2	TMFCON23	R/W	8/16	00H
0F36DH	Timer F control register 3	TMFCON3		R/W	8	00H

8.2.2 Timer 8 Data Register (TM8D)

Address: 0F8E0H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM8D	T8D7	T8D6	T8D5	T8D4	T8D3	T8D2	T8D1	T8D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM8D is a special function register (SFR) to set the value to be compared with the Timer 8 counter register (TM8C) value.

Note:
Set TM8D when the timer stops (When T8STAT bit of TM8CON1 register is "0").
In 8-bit timer mode, writing "00H" to TM8D sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TM8D and the high-order TM9D sets the low-order TM8D to "01H" and the high-order TM9D to "00H".

8.2.3 Timer 9 Data Register (TM9D)

Address: 0F8E4H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM9D	T9D7	T9D6	T9D5	T9D4	T9D3	T9D2	T9D1	T9D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM9D is a special function register (SFR) to set the value to be compared with the value of the Timer 9 counter register (TM9C).

Note:
Set TM9D when the timer stops (When T9STAT bit of TM9CON1 register is "0").
In 8-bit timer mode, writing "00H" to TM9D sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TM8D and the high-order TM9D sets the low-order TM8D to "01H" and the high-order TM9D to "00H".

8.2.4 Timer A Data Register (TMAD)

Address: 0F8E8H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMAD	TAD7	TAD6	TAD5	TAD4	TAD3	TAD2	TAD1	TAD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMAD is a special function register (SFR) to set the value to be compared with the Timer A counter register (TMAC) value.

Note:
Set TMAD when the timer stops (When TASTAT bit of TMACON1 register is "0").
In 8-bit timer mode, writing "00H" to TMAD sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMAD and the high-order TMBD sets the low-order TMAD to "01H" and the high-order TMBD to "00H".

8.2.5 Timer B Data Register (TMBD)

Address: 0F8ECH
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMBD	TBD7	TBD6	TBD5	TBD4	TBD3	TBD2	TBD1	TBD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMBD is a special function register (SFR) to set the value to be compared with the value of the Timer B counter register (TMBC).

Note:
Set TMBD when the timer stops (When TBSTAT bit of TMBCON1 register is "0").
In 8-bit timer mode, writing "00H" to TMBD sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMAD and the high-order TMBD sets the low-order TMAD to "01H" and the high-order TMBD to "00H".

8.2.6 Timer E Data Register (TMED)

Address: 0F360H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMED	TED7	TED6	TED5	TED4	TED3	TED2	TED1	TED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMED is a special function register (SFR) to set the value to be compared with the Timer E counter register (TMEC) value.

Note:
Set TMED when the timer stops (When TESTAT bit of TMECON1 register is "0").
In 8-bit timer mode, writing "00H" to TMED sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMED and the high-order TMFD sets the low-order TMED to "01H" and the high-order TMFD to "00H".

8.2.7 Timer F Data Register (TMFD)

Address: 0F368H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TMFD	TFD7	TFD6	TFD5	TFD4	TFD3	TFD2	TFD1	TFD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMFD is a special function register (SFR) to set the value to be compared with the value of the Timer F counter register (TMFC).

Note:
Set TMFD when the timer stops (When TFSTAT bit of TMFCON1 register is "0").
In 8-bit timer mode, writing "00H" to TMFD sets it to "01H".
In 16-bit timer mode, writing "00H" to both the low-order TMED and the high-order TMFD sets the low-order TMED to "01H" and the high-order TMFD to "00H".

8.2.8 Timer 8 Counter Register (TM8C)

Address: 0F8E1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8C	T8C7	T8C6	T8C5	T8C4	T8C3	T8C2	T8C1	T8C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM8C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM8C is performed, TM8C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TM8C or high-order TM9C, both the low-order and the high-order are set to "0000H".

During timer operation, the contents of TM8C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-1 shows whether a TM8C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-1 TM8C Read Enable/Disable during Timer Operation

Timer clock T8CK	System clock SYSCLK	TM8C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM8C twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled

8.2.9 Timer 9 Counter Register (TM9C)

Address: 0F8E5H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9C	T9C7	T9C6	T9C5	T9C4	T9C3	T9C2	T9C1	T9C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM9C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM9C is performed, TM9C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TM8C or high-order TM9C, both the low order and the high order are set to "0000H".
When reading TM9C in 16-bit timer mode, be sure to read TM8C first since the count value of TM9C is stored in the TM9C latch when TM8C is read.

During timer operation, the contents of TM9C may not be read depending on the conditions of the timer clock and the system clock.
Table 8-2 shows whether a TM9C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-2 TM9C Read Enable/Disable during Timer Operation

Timer clock T9CK	System clock SYSCLK	TM9C read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM9C twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled

8.2.10 Timer A Counter Register (TMAC)

Address: 0F8E9H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMAC	TAC7	TAC6	TAC5	TAC4	TAC3	TAC2	TAC1	TAC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMAC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMAC is performed, TMAC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TMAC or high-order TMBC, both the low-order and the high-order are set to "0000H".

During timer operation, the contents of TMAC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-3 shows whether a TMAC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-3 TMAC Read Enable/Disable during Timer Operation

Timer clock TACK	System clock SYSCLK	TMAC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TMAC twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled

8.2.11 Timer B Counter Register (TMBC)

Address: 0F8EDH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBC	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMBC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMBC is performed, TMBC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TMAC or high-order TMBC, both the low order and the high order are set to "0000H".
When reading TMBC in 16-bit timer mode, be sure to read TMAC first since the count value of TMBC is stored in the TMBC latch when TMAC is read.

During timer operation, the contents of TMBC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-4 shows whether a TMBC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-4 TMBC Read Enable/Disable during Timer Operation

Timer clock TBCK	System clock SYSCLK	TMBC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TMBC twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled

8.2.12 Timer E Counter Register (TMEC)

Address: 0F361H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMEC	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMEC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMEC is performed, TMEC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TMEC or high-order TMFC, both the low-order and the high-order are set to "0000H".

During timer operation, the contents of TMEC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-5 shows whether a TMEC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-5 TMEC Read Enable/Disable during Timer Operation

Timer clock TECK	System clock SYSCLK	TMEC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TMEC twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled

8.2.13 Timer F Counter Register (TMFC)

Address: 0F369H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFC	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFC is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TMFC is performed, TMFC is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if write operation is performed to either the low-order TMEC or high-order TMFC, both the low order and the high order are set to "0000H".
When reading TMFC in 16-bit timer mode, be sure to read TMEC first since the count value of TMFC is stored in the TMFC latch when TMEC is read.

During timer operation, the contents of TMFC may not be read depending on the conditions of the timer clock and the system clock.
Table 8-6 shows whether a TMFC read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 8-6 TMFC Read Enable/Disable during Timer Operation

Timer clock TFCK	System clock SYSCLK	TMFC read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TMFC twice and check that the results match.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled

8.2.14 Timer 8 Control Register 0 (TM8CON0)

Address: 0F8E2H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8CON0	T8OST	—	T89M16	—	—	—	T8CS1	T8CS0
R/W	R/W	R	R/W	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM8CON0 is a special function (SFR) to control a Timer 8.
Rewrite TM8CON0 while the Timer 8 is stopped (T8STAT of the TM8CON1 register is "0").

[Description of Bits]

- **T8CS1, T8CS0** (bits 1, 0)
  The T8CS1 and T8CS0 bits are used for selecting the operation clock of Timer 8. LSCLK, HTBCLK, or 1/64 HTBCLK, or 1/16HTBCLK can be selected by these bits.

T8CS1	T8CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	1/64 HTBCLK
1	1	1/16 HTBCLK

- **T89M16** (bit 5)
  The T89M16 bit is used for selecting the operating mode of Timer 8 and Timer 9. When the T89M16 bit is set to "1", timer 8 and timer 9 are connected and they operate as a 16-bit timer.
  In 8-bit timer mode, each of Timer 8 and Timer 9 operates independently as a 8-bit timer.
  In 16-bit timer mode, Timer 8 and Timer 9 are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, Timer 9 is incremented by a Timer 8 overflow signal. A Timer 8 interrupt (TM8INT) is not generated.

T89M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

- **T8OST** (bit 7)
  The T8OST bit is used for the operation mode of timer 8 for 8-bit timer mode or timer 8 and timer 9 for 16-bit timer mode. If T8OST is set to "1", one shot timer mode can be used. In one shot timer mode, when the timer counter (TM8C) and the timer data register (TM8D) coincide, the timer counter (TM8C) is reset to "00H" and a timer count stop.
  When 16-bit timer mode (T89M16 of the TM8CON0 register is "1") is chosen, in one shot timer mode, the timer counter (TM8C, TM9D) and the timer data register (TM8D, TM9D) coincide, the timer counter (TM8C, TM9D) is reset to "00H" and a timer count stop.

T8OST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.15 Timer 9 Control Register 0 (TM9CON0)

Address: 0F8E6H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9CON0	T9OST	T9NEG	—	—	—	—	T9CS1	T9CS0
R/W	R/W	R/W	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM9CON0 is a special function (SFR) to control a Timer 9.
Rewrite TM9CON0 while the Timer 9 is stopped (T9STAT of the TM9CON1 register is "0").

[Description of Bits]

- **T9CS1, T9CS0** (bits 1, 0)
  The T9CS1 and T9CS0 bits are used for selecting the operation clock of Timer 9. LSCLK, HTBCLK, or 1/64 HTBCLK, or 1/16 HTBCLK can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting T89M16 of TM8CON to "1", the values of T9CS1 and T9CS0 are invalid.

T9CS1	T9CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	1/64 HTBCLK
1	1	1/16 HTBCLK

- **T9NEG** (bit 6)
  The T9NEG bit selects the output logic of TM9OUT. TM9OUT output is "0" in positive logic, and "1" in negative logic.

T9NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **T9OST** (bit 7)
  The T9OST bit is used for the operation mode of timer 8 for 8-bit timer mode. If T9OST is set to "1", one shot timer mode can be used. In one shot timer mode, when the timer counter (TM9C) and the timer data register (TM9D) coincide, the timer counter (TM9C) is reset to "00H" and a timer count stop.
  When 16-bit timer mode (T89M16 of the TM8CON0 register is "1") is chosen, in one shot timer mode, the value of T9OST becomes invalid.

T9OST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.16 Timer A Control Register 0 (TMACON0)

Address: 0F8EAH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMACON0	TAOST	—	TABM16	—	—	—	TACS1	TACS0
R/W	R/W	R	R/W	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMACON0 is a special function (SFR) to control a Timer A.
Rewrite TMACON0 while the Timer A is stopped (TASTAT of the TMACON1 register is "0").

[Description of Bits]

- **TACS1, TACS0** (bits 1, 0)
  The TACS1 and TACS0 bits are used for selecting the operation clock of Timer A. LSCLK, HTBCLK, or 1/64 HTBCLK, or 1/16HTBCLK can be selected by these bits.

TACS1	TACS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	1/64 HTBCLK
1	1	1/16 HTBCLK

- **TABM16** (bit 5)
  The TABM16 bit is used for selecting the operating mode of Timer A and Timer B.
  In 8-bit timer mode, each of Timer A and Timer B operates independently as a 8-bit timer.
  In 16-bit timer mode, Timer A and Timer B are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, Timer B is incremented by a Timer A overflow signal. A Timer A interrupt (TMAINT) is not generated.

TABM16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

- **TAOST** (bit 7)
  The TAOST bit is used for the operation mode of timer A for 8-bit timer mode or timer A and timer B for 16-bit timer mode. If TAOST is set to "1", one shot timer mode can be used. In one shot timer mode, when the timer counter (TMAC) and the timer data register (TMAD) coincide, the timer counter (TMAC) is reset to "00H" and a timer count stop.
  When 16-bit timer mode (TABM16 of the TMACON0 register is "1") is chosen, in one shot timer mode, the timer counter (TMAC, TMBD) and the timer data register (TMAD, TMBD) coincide, the timer counter (TMAC, TMBD) is reset to "00H" and a timer count stop.

TAOST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.17 Timer B Control Register 0 (TMBCON0)

Address: 0F8EEH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBCON0	TBOST	—	—	—	—	—	TBCS1	TBCS0
R/W	R/W	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMBCON0 is a special function (SFR) to control a Timer B.
Rewrite TMBCON0 while the Timer B is stopped (TBSTAT of the TMBCON1 register is "0").

[Description of Bits]

- **TBCS1, TBCS0** (bits 1, 0)
  The TBCS1 and TBCS0 bits are used for selecting the operation clock of Timer B. LSCLK, HTBCLK, or 1/64 HTBCLK, or 1/16 HTBCLK can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting TABM16 of TMACON to "1", the values of TBCS1 and TBCS0 are invalid.

TBCS1	TBCS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	1/64 HTBCLK
1	1	1/16 HTBCLK

- **TBOST** (bit 7)
  The TBOST bit is used for the operation mode of timer A for 8-bit timer mode. If TBOST is set to "1", one shot timer mode can be used. In one shot timer mode, when the timer counter (TMBC) and the timer data register (TMBD) coincide, the timer counter (TMBC) is reset to "00H" and a timer count stop.
  When 16-bit timer mode (TABM16 of the TMACON0 register is "1") is chosen, in one shot timer mode, the value of TBOST becomes invalid.

TBOST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

8.2.18 Timer E Control Register 0 (TMECON0)

Address: 0F362H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON0	—	—	—	—	—	TEFM16	TECS1	TECS0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON0 is a special function (SFR) to control a Timer E.
Rewrite TMECON0 while the Timer E is stopped (TESTAT of the TMECON1 register is "0").

[Description of Bits]

- **TECS1, TECS0** (bits 1, 0)
  The TECS1 and TECS0 bits are used for selecting the operation clock of Timer E. LSCLK, HTBCLK, or 1/64 HTBCLK, or 1/16HTBCLK can be selected by these bits.

TECS1	TECS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	1/64 HTBCLK
1	1	1/16 HTBCLK

- **TEFM16** (bit 2)
  The TEFM16 bit is used for selecting the operating mode of Timer E and Timer F.
  In 8-bit timer mode, each of Timer E and Timer F operates independently as a 8-bit timer.
  In 16-bit timer mode, Timer E and Timer F are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, Timer F is incremented by a Timer E overflow signal. A Timer E interrupt (TMEINT) is not generated.

TEFM16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

8.2.19 Timer F Control Register 0 (TMFCON0)

Address: 0F36AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON0	—	—	—	—	—	—	TFCS1	TFCS0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON0 is a special function (SFR) to control a Timer F.
Rewrite TMFCON0 while the Timer F is stopped (TFSTAT of the TMFCON1 register is "0").

[Description of Bits]

- **TFCS1, TFCS0** (bits 1, 0)
  The TFCS1 and TFCS0 bits are used for selecting the operation clock of Timer F. LSCLK, HTBCLK, or 1/64 HTBCLK, or 1/16 HTBCLK can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting TEFM16 of TMECON to "1", the values of TFCS1 and TFCS0 are invalid.

TFCS1	TFCS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	1/64 HTBCLK
1	1	1/16 HTBCLK

8.2.20 Timer 8 Control Register 1 (TM8CON1)

Address: 0F8E3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM8CON1	T8STAT	—	—	—	—	—	—	T8RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM8CON1 is a special function register (SFR) to control a Timer 8.

[Description of Bits]

- **T8RUN** (bit 0)
  The T8RUN bit is used for controlling stop/start of Timer 8.

T8RUN	Description
0	Stops counting.
1	Starts counting.

- **T8STAT** (bit 7)
  The T8STAT bit is used for indicating "counting stopped"/"counting in progress" of Timer 8.

T8STAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.21 Timer 9 Control Register 1 (TM9CON1)

Address: 0F8E7H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM9CON1	T9STAT	—	—	—	—	—	—	T9RUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TM9CON1 is a special function register (SFR) to control a Timer 9.

[Description of Bits]

- **T9RUN** (bit 0)
  The T9RUN bit is used for controlling count stop/start of Timer 9.
  In 16-bit timer mode, be sure to set this bit to "0". Timer 9 is incremented caused by a Timer 8 overflow signal regardless of the value of T9RUN.

T9RUN	Description
0	Stops counting.
1	Starts counting.

- **T9STAT** (bit 7)
  The T9STAT bit is used for indicating "counting stopped"/"counting in progress" of Timer 9.
  In 16-bit timer mode, this bit will read "0".

T9STAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.22 Timer A Control Register 1 (TMACON1)

Address: 0F8EBH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMACON1	TASTAT	—	—	—	—	—	—	TARUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TMACON1 is a special function register (SFR) to control a Timer A.

[Description of Bits]

- **TARUN** (bit 0)
  The TARUN bit is used for controlling stop/start of Timer A.

TARUN	Description
0	Stops counting.
1	Starts counting.

- **TASTAT** (bit 7)
  The TASTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer A.

TASTAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.23 Timer B Control Register 1 (TMBCON1)

Address: 0F8EFH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMBCON1	TBSTAT	—	—	—	—	—	—	TBRUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

TMBCON1 is a special function register (SFR) to control a Timer B.

[Description of Bits]

- **TBRUN** (bit 0)
  The TBRUN bit is used for controlling count stop/start of Timer B.
  In 16-bit timer mode, be sure to set this bit to "0". Timer B is incremented caused by a Timer A overflow signal regardless of the value of TBRUN.

TBRUN	Description
0	Stops counting.
1	Starts counting.

- **TBSTAT** (bit 7)
  The TBSTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer B.
  In 16-bit timer mode, this bit will read "0".

TBSTAT	Description
0	Counting stopped.
1	Counting in progress.

8.2.24 Timer E Control Register 1 (TMECON1)

Address: 0F363H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON1	TESTAT	—	—	—	—	—	TETGEN	TERUN
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON1 is a special function register (SFR) to control a Timer E.

[Description of Bits]

- **TERUN** (bit 0)
  The TERUN bit is used for controlling stop/start of Timer E.

TERUN	Description
0	Stops counting.
1	Starts counting.

- **TETGEN** (bit 1)
  The TETGEN bit is enable flag of timer E stop/start by the external trigger input.

TDTGEN	Description
0	Timer E stop/start by the external trigger is disabled (Initial value)
1	Timer E stop/start by the external trigger is enabled

- **TESTAT** (bit 7)
  The TESTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer E.

TESTAT	Description
0	Counting stopped.
1	Counting in progress.

Note:
For normal (continuous) timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TERUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TERUN bit shows "1" as is controlled to start (keep) counting. Therefore, reading TERUN bit can be used for recognizing which interrupt occurred.
For one shot timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TERUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TERUN bit also shows "0" as is controlled to stop counting. To recognizing which interrupt occurred, read timer count register and timer data register and check if the timer count register value is consistent timer data register value.
When the timer count is stopped by the external trigger and TERUN bit shows "0", make sure to start the next operation after TESTAT bit shows "0" as the timer count is halted.

8.2.25 Timer F Control Register 1 (TMFCON1)

Address: 0F36BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON1	TFSTAT	—	—	—	—	—	TFTGEN	TFRUN
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON1 is a special function register (SFR) to control a Timer F.

[Description of Bits]

- **TFRUN** (bit 0)
  The TFRUN bit is used for controlling count stop/start of Timer F.
  In 16-bit timer mode, be sure to set this bit to "0". Timer F is incremented caused by a Timer E overflow signal regardless of the value of TFRUN.

TFRUN	Description
0	Stops counting.
1	Starts counting.

- **TFTGEN** (bit 1)
  The TFTGEN bit is enable flag of timer F stop/start by the external trigger input.
  In cases where the 16-bit timer mode has been selected by setting TEFM16 of TMECON to "1", the value of TFTGEN is invalid.

TDTGEN	Description
0	Timer F stop/start by the external trigger is disabled (Initial value)
1	Timer F stop/start by the external trigger is enabled

- **TFSTAT** (bit 7)
  The TFSTAT bit is used for indicating "counting stopped"/"counting in progress" of Timer F.
  In 16-bit timer mode, this bit will read "0".

TFSTAT	Description
0	Counting stopped.
1	Counting in progress.

Note:
For normal (continuous) timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TFRUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TFRUN bit shows "1" as is controlled to start (keep) counting. Therefore, reading TARUN bit can be used for recognizing which interrupt occurred.
For one shot timer mode, when the timer count is stopped by the external trigger input and the interrupt is generated, TFRUN bit shows "0" as is controlled to stop counting. When the timer count register coincides with the timer data register and the interrupt is generated, TFRUN bit also shows "0" as is controlled to stop counting. To recognizing which interrupt occurred, read timer count register and timer data register and check if the timer count register value is consistent timer data register value.
When the timer count is stopped by the external trigger and TFRUN bit shows "0", make sure to start the next operation after TFSTAT bit shows "0" as the timer count is halted.

8.2.26 Timer E Control Register 2 (TMECON2)

Address: 0F364H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON2	TEOST	—	TETRM1	TETRM0	—	—	TEST1	TEST0
R/W	R/W	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON2 is a special function (SFR) to control a Timer E.
Rewrite TMECON2 while the Timer E is stopped (TESTAT of the TMECON1 register is "0") and the Timer E stop/start by the external trigger is disabled (TETGEN of the TMECON1 register is "0").

※When rewrite TMECON2 while the Timer E stop/start by the external trigger is enabled (TETGEN of the TMECON1 register is "1"), refer to the following "Note".

[Description of Bits]

- **TEST1, TEST0** (bits 1, 0)
  The TEST1 and TEST0 bits are used to select the start/stop mode of the timer E counter.

TEST1	**TEST0**	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

- **TETRM1, TETRM0** (bits 5, 4)
  The TETRM1 and TETRM0 bits are used to select the start mode of the timer E counter.This is valid only when the external input start and stop modes are selected. When the timer count is stopped by the external input, an interrupt is generated.

TETRM1	**TETRM0**	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

- **TEOST** (bit 7)
  The TEOST bit is used for the operation mode of timer E for 8-bit timer mode or timer E and timer F for 16-bit timer mode. If TEOST is set to "1", one shot timer mode can be used. In one shot timer mode, when the timer counter (TMEC) and the timer data register (TMED) coincide, the timer counter (TMEC) is reset to "00H" and a timer count stop.
  When 16-bit timer mode (TEFM16 of the TMECON0 register is "1") is chosen, in one shot timer mode, the timer counter (TMEC, TMFD) and the timer data register (TMED, TMFD) coincide, the timer counter (TMEC, TMFD) is reset to "00H" and a timer count stop.

TEOST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

Note:
The note point of when rewrite TMECON2 while the Timer E stop/start by the external trigger is enabled (TETGEN of the TMECON1 register is "1").

- When rewrite the TEST1 and TEST0 bits, rewrite TEST0 while the Timer E is run (TESTAT of the TMECON1 register is "1") and rewrite TEST1 while the Timer E is stopped (TESTAT of the TMECON1 register is "0").
- When rewrite the TETRM1 and TETRM0 bits, rewrite TETRM0 while the Timer E is run (TESTAT of the TMECON1 register is "1") and rewrite TETRM1 while the Timer E is stopped (TESTAT of the TMECON1 register is "0").
- When rewrite the TEOST bit, rewrite TEOST while the Timer E is run (TESTAT of the TMECON1 register is "1").

8.2.27 Timer F Control Register 2 (TMFCON2)

Address: 0F36CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON2	TFOST	TFNEG	TFTRM1	TFTRM0	—	—	TFST1	TFST0
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON2 is a special function (SFR) to control a Timer F.
Rewrite TMFCON2 while the Timer F is stopped (TFSTAT of the TMFCON1 register is "0") and the Timer F stop/start by the external trigger is disabled (TFTGEN of the TMFCON1 register is "0").

※When rewrite TMFCON2 while the Timer F stop/start by the external trigger is enabled (TFTGEN of the TMFCON1 register is "1"), refer to the following "Note".

[Description of Bits]

- **TFST1, TFST0** (bits 1, 0)
  The TFST1 and TFST0 bits are used for selecting the operation clock of Timer F. LSCLK, HTBCLK, or 1/64 HTBCLK, or 1/16 HTBCLK can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting TEFM16 of TMECON to "1", the values of TFST1 and TFST0 are invalid.

TEST1	**TEST0**	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

- **TFTRM1, TFTRM0** (bits 5, 4)
  The TFTRM1 and TFTRM0 bits are used to select the start mode of the timer F counter.This is valid only when the external input start and stop modes are selected. When the timer count is stopped by the external input, an interrupt is generated.
  When TEFM16 of TMECON0 has chosen "1" and 16 bit timer mode is selected, the value of TFTRM1 and TFTRM0 becomes invalid.

TFTRM1	**TFTRM0**	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

- **TFNEG** (bit 6)
  The TFNEG bit selects the output logic of TMFOUT. TMFOUT output is "0" in positive logic, and "1" in negative logic.

TFNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **TFOST** (bit 7)
  The TFOST bit is used for the operation mode of timer F for 8-bit timer mode. If TFOST is set to "1", one shot timer mode can be used. In one shot timer mode, when the timer counter (TMFC) and the timer data register (TMFD) coincide, the timer counter (TMFC) is reset to "00H" and a timer count stop.
  When 16-bit timer mode (TEFM16 of the TMECON0 register is "1") is chosen, in one shot timer mode, the value of TFOST becomes invalid.

TFOST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

Note:
The note point of when rewrite TMFCON2 while the Timer F stop/start by the external trigger is enabled (TFTGEN of the TMFCON1 register is "1").

・When rewrite the TFST1 and TFST0 bits, rewrite TFST0 while the Timer F is run (TFSTAT of the TMFCON1 register is "1") and rewrite TFST1 while the Timer F is stopped (TFSTAT of the TMFCON1 register is "0").
・When rewrite the TFTRM1 and TFTRM0 bits, rewrite TFTRM0 while the Timer F is run (TFSTAT of the TMFCON1 register is "1") and rewrite TFTRM1 while the Timer F is stopped (TFSTAT of the TMFCON1 register is "0").
・When rewrite the TFOST bit, rewrite TFOST while the Timer F is run (TFSTAT of the TMFCON1 register is "1").

8.2.28 Timer E Control Register 3 (TMECON3)

Address: 0F365H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMECON3	—	—	—	—	TESTSS	TESTS2	TESTS1	TESTS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMECON3 is a special function register (SFR) to control the Timer E.
Rewrite TMECON3 while the timer E is stopped (TESTAT of the TMECON1 register is "0") and the Timer E stop/start by the external trigger is disabled (TETGEN of the TMECON1 register is "0").

[Description of Bits]

- **TESTSS, TESTS2, TESTS1**, **TESTS0** (bits 3~0)
  TESTSS, TESTS2, TESTS1, and TESTS0 bits are used to select the external input start/stop pins of the timer E. To use these bits to select the Port A and B pins, use the Port A and B mode registers 0,1 (PnMOD0, PnMOD1) to select the primary function and use the Port A and B direction (PnDIR) to set the input mode for the appropriate pins. (n=A,B)

TESTS2	TESTS1	TESTS0	Description	
			When TESTSS="0" (initial value)	When TESTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	Prohibited (*)	PB3 pin
1	0	0	Prohibited (*)	PB4 pin
1	0	1	Prohibited (*)	PB5 pin
1	1	0	Prohibited (*)	PB6 pin
1	1	1	Prohibited (*)	PB7 pin

(*) Because no external trigger signal will be input, external triggers cannot start/stop the timer.

8.2.29 Timer F Control Register 3 (TMFCON3)

Address: 0F36DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMFCON3	—	—	—	—	TFSTSS	TFSTS2	TFSTS1	TFSTS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMFCON3 is a special function register (SFR) to control the Timer F.
Rewrite TMFCON3 while the timer F is stopped (TFSTAT of the TMFCON1 register is "0") and the Timer F stop/start by the external trigger is disabled (TFTGEN of the TMFCON1 register is "0").

[Description of Bits]

- **TFSTSS, TFSTS2, TFSTS1**, **TFSTS0** (bits 3~0)
  TFSTSS, TFSTS2, TFSTS1, and TFSTS0 bits are used to select the external input start/stop pins of the timer F. To use these bits to select the Port A and B pins, use the Port A and B mode registers 0,1 (PnMOD0, PnMOD1) to select the primary function and use the Port A and B direction (PnDIR) to set the input mode for the appropriate pins. (n=A,B)
  When TEFM16 of TMECON0 has chosen "1" and 16 bit timer mode is selected, the value of TFSTSS and TFSTS2 and TFSTS1 and TFSTS0 becomes invalid.

TFSTS2	TFSTS1	TFSTS0	Description	
			When TFSTSS="0" (initial value)	When TFSTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	Prohibited (*)	PB3 pin
1	0	0	Prohibited (*)	PB4 pin
1	0	1	Prohibited (*)	PB5 pin
1	1	0	Prohibited (*)	PB6 pin
1	1	1	Prohibited (*)	PB7 pin

(*) Because no external trigger signal will be input, external triggers cannot start/stop the timer.

8.3 Description of Operation

When the TnRUN bit of timer 8 to B,E,F control register 1 (TMnCON1) is set to "1", the timer counter (TMnC) is set to an operating state (TnSTAT is set to "1") on the first falling edge of the timer clock (TnCK) being selected by the Timer 8 to B,E,F control register 0 (TMnCON0). Then, the timer counter (TMnC) starts incrementing on the 2nd falling edge.

When the count value of TMnC and the timer 8 to B,E,F data register (TMnD) coincide, timer 8 to B,E,F interrupt (TMnINT) occurs on the next timer clock falling edge and at the same time, TMnC is reset to "00H" and continues incrementing.

Whenever the value of the count value of TMnC and the preset value of a timer n data register (TMnD) is in agreement, the output value of timer out (TM9OUT, TMFOUT) is reversed. This timer out can be outputted outside as fourthly function of a port A. Timer out is set to "0" to the time of system reset, and a timer count stop.

When the TnRUN bit is set to "0", TMnC stops incrementing after counting the falling of the timer clock (TnCK) once. Confirm that TMnC has been stopped by checking that the TnSTAT bit of the Timer 8 to B,E,F control register 1 (TMnCON1) is "0". When the TnRUN bit is set to "1" again, TMnC restarts incrementing from the previous value. To initialize TMnC to "00H", perform a write operation to TMnC.
The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n = 8 \text{ to } B,E,F)$$

TMnD: Timer 8 to B,E,F data register (TMnD) setting value (01H to 0FFH)
TnCK: Clock frequency selected by the Timer 8 to B,E,F control register 0 (TMnCON0)

After the TnRUN bit is set to "1", the timer is synchronized by the timer clock to start counting. Therefore, an error of a maximum of 1 clock period occurs until the first timer interrupt occurs. The timer interrupt periods from the second time onward are constant.
Figure 8-2 shows the operation timing diagram of Timer 8 to B,E,F.

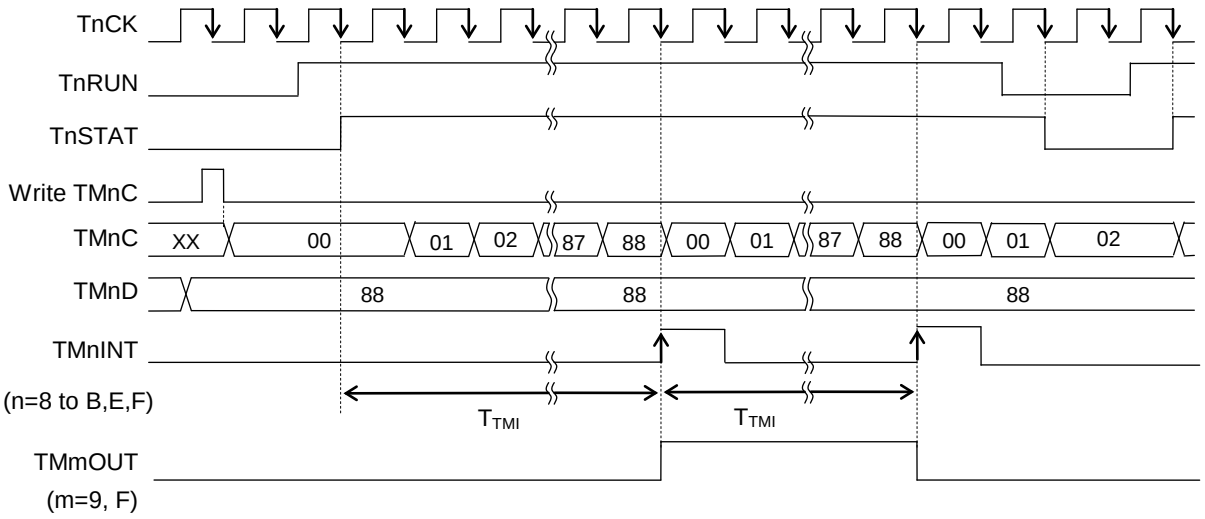


Figure 8-2 Operation Timing Diagram of Timer 8 to B,E,F

Note:
Even if "0" is written to the TnRUN bit, counting operation continues up to the falling edge (the timer 8 to B,E,F status flag (TnSTA) is in a "1" state) of the next timer clock pulse. Therefore, the timer 8 to B,E,F interrupt (TMnINT) may occur.
During a timer stop, an external-triggering stop becomes invalid until TnSTAT will be set to "1", if a TnRUN bit is set "1". Moreover, when the timer is running, an external-triggering start becomes invalid until TnSTAT will be set to "0", if a TnRUN bit is set "0".

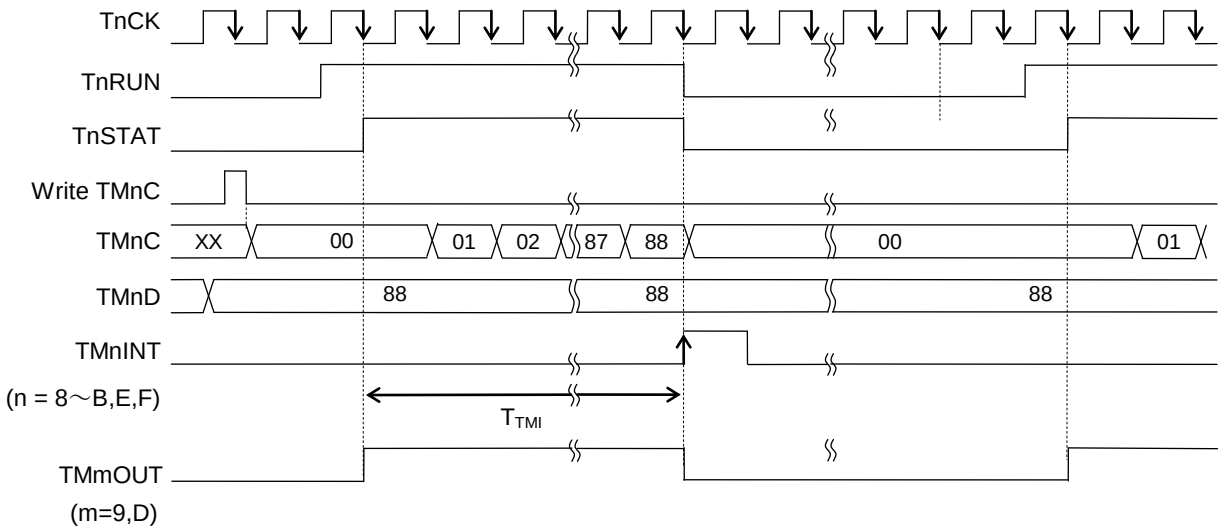
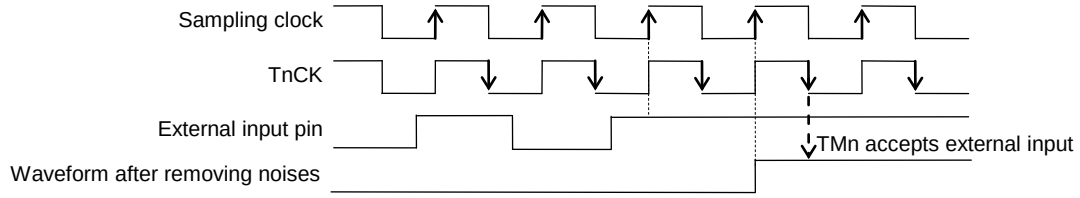


Figure 8-3 One-shot timer mode Operation Timing Diagram of Timer 8 to B,E,F

Note:
When the count value of TMnC and the value of a timer 8 to B,E,F data register (TMnD) are in agreement, a TnRUN bit is cleared automatically.

8.3.1 The external timer start/stop operation

For the external timer start/stop operation of the timer E,F, the external timer start/stop is enabled when the external input is selected on timer control register 2(TMnCON2) and the timer control register 3(TMnCON3) and TnTGEN bit of timer control register 1(TMnCON1) is set as "1". From the external input, pulses shorter than one sampling clock are removed as noises. The sampling clock is selected by the TnCS1 and TnCS0 bits.



Note:
When the external input pulses shorter than one sampling clock is inputted, it is removed as noises and don't operate start or stop. And when the external input pulses longer than one sampling clock less than two sampling clocks, the external trigger may not be recognized certainly. It begins to read the condition of the port(PnD, n=A,B) and the condition of the timer E,F(TnSTAT, n=E,F) by the port interruption, and confirming that the timer operate normally is recommended. Refer to the concrete example in the following.

When "H" pulse width is measured, set rising-edge start and falling-edge stop.
It begins to read the condition of the port(PnD, n=A,B) and the condition of the timer E,F(TnSTAT, n=E,F) by the port interruption, it is recommended that stop the timer and clear the timer counter(TnC, n=E,F) and measure again because the timer doesn't stop in the case of PnD = "L" and TnSTAT = "H" and it can't be measured correctly.

When "L" pulse width is measured, set falling-edge start and rising-edge stop.
It begins to read the condition of the port(PnD, n=A,B) and the condition of the timer E,F(TnSTAT, n=E,F) by the port interruption, it is recommended that stop the timer and clear the timer counter(TnC, n=E,F) and measure again because the timer doesn't stop in the case of PnD = "H" and TnSTAT = "H" and it can't be measured correctly.

When a pulse period is measured, measure "H" pulse width at first, and it confirms that pulse width is longer than two sampling clocks.

When the "H" pulse width longer than two sampling clocks, set rising-edge start and falling-edge stop and measure it. When the "H" pulse width shorter than two sampling clocks, it may not be able to measure certainly. In this case, don't use the external timer start/stop operation and it is recommended that start or stop the timer by the port interruption.

8.3.2 The external timer operation

For the external timer start/stop operation of the timer E,F, the external timer start/stop is enabled when the external input is selected on timer control register 2(TMnCON2) and the timer control register 3(TMnCON3) and TnTGEN bit of timer control register 1(TMnCON1) is set as "1". If the rising or falling of an external input pin occur in this state, the TnRUN bit of the timer control register 1 (TMnCON1) will be set to "1" by hardware.The timer counter (TMnC) is set to an operating state (TnSTAT is set to "1") on the first falling edge of the timer clock (TnCK) being selected by the Timer E,F control register 0 (TMnCON0). Then, the timer counter (TMnC) starts incrementing on the 2nd falling edge.

When the count value of TMnC and the timer E,F data register (TMnD) coincide, timer E,F interrupt (TMnINT) occurs on the next timer clock falling edge and at the same time, TMnC is reset to "00H" and continues incrementing. When stop timer by an external input is selected, if the rising edge/falling edge of the external input selected by TMnCON2 happen, TMnINT will be generated in the falling edge of the next timer clock, and the counting of TMnC will be stopped.

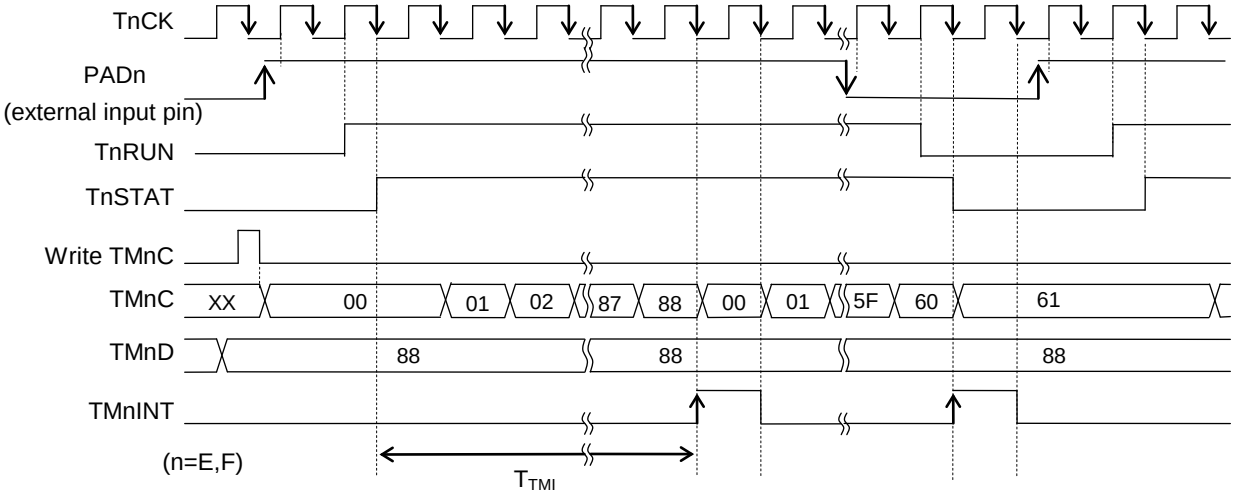


Figure 8-4(a) Normal mode Operation Timing Diagram of Timer E,F

（timer count is started by the external input rising edge、timer count is stoped by the external input falling edge.）

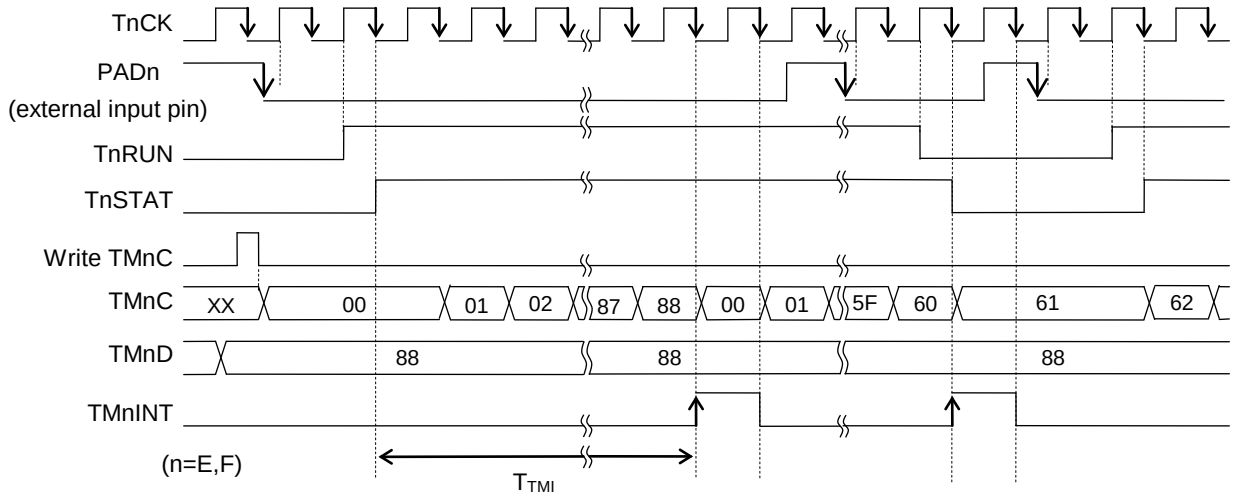


Figure 8-4(b) Normal mode Operation Timing Diagram of Timer E,F

（timer count is started by the external input falling edge、timer count is stoped by the external input falling edge.）

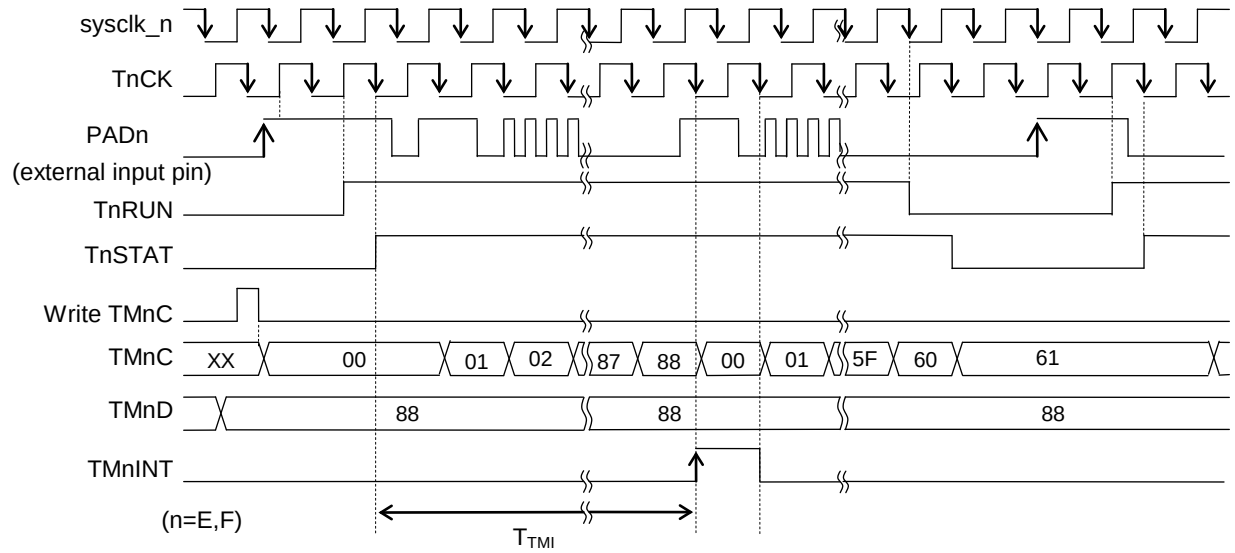


Figure 8-4(c) Normal mode Operation Timing Diagram of Timer E,F

（timer count is started by the external input rising edge、timer count is stoped by software.）

Note:
Although "0" is written in TnRUN, since TnSTAT continues a counting operation to the falling edge of the next timer clock in the status of "1", TMnINT may occur.

Chapter 9

Watchdog Timer

9 Watchdog Timer

9.1 Overview

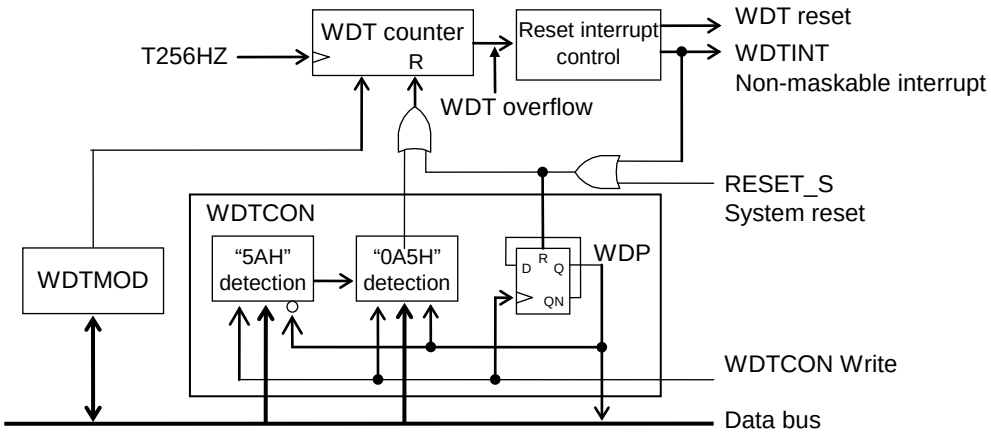
This LSI incorporates a watchdog timer (WDT) that operates at a system reset unconditionally (free-run operation) in order to detect an undefined state of the MCU and return from that state.
If the WDT counter overflows due to the failure of clearing of the WDT counter within the WDT overflow period, the watchdog timer requests a WDT interrupt (non-maskable interrupt). When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 5, "Interrupts," and for WDT interrupt see Chapter 3, "Reset Function".

9.1.1 Features

- Free running (cannot be stopped)
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s) selectable by software
- Non-maskable interrupt by the first overflow
- Reset generated by the second overflow

9.1.2 Configuration

Figure 9-1 shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register

Figure 9-1 Configuration of Watchdog Timer

9.2 Description of Registers

9.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H

9.2.2 Watchdog Timer Control Register (WDTCON)

Address: 0F00EH
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to clear the WDT counter.
When WDTCON is read, the value of the internal pointer (WDP) is read from bit 0.

[Description of Bits]

- **WDP/d0** (bit 0)
  The value of the internal pointer (WDP) is read from this bit. The WDP is reset to "0" at the system reset or Watch Dog Timer overflow and is inverted every writing to WDTCON.

- **d7-d0** (bits 7-0)
  This bit is used to write data to clear the WDT counter. Write "5AH" on the condition of WDP is "0" and write "0A5H" on the condition of WDP is "1".

Note:
When the WDT interrupt (WDTINT) occurs by the first WDT counter overflow, the counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15.25us). During the time period that they are initialized, writing to WDTCON is disable and the logic of WDP does not change. Therefore, in the case of that you have program codes handle to clear the WDT when the first overflow WDT interrupt occurs and also the codes run at high-speed system clock, please check the WDP gets reversed after writing to WDTCON to see if the writing was surely successful. For example of the program code, see Section 9.3.1, "Handling example when you do not want to use the watch dog timer".

9.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: W
Access size: 8 bits
Initial value: 02H

	7	6	5	4	3	2	1	0
WDTMOD	—	—	—	—	—	—	WDT1	WDT0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of the watchdog timer.

[Description of Bits]

- **WDT1-0** (bits 1-0)
  These bits are used to select an overflow period of the watchdog timer.
  The WDT1 and WDT0 bits set a overflow period (TWOV) of the WDT counter. One of 125ms, 500ms, 2s, and 8s can be selected.

WDT1	WDT0	Description
0	0	125 ms
0	1	500 ms
1	0	2 s (initial value)
1	1	8 s

9.3 Description of Operation

The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start..
Write "5AH" when the internal pointer (WDP) is "0"and then the WDT counter is cleared by writing "0A5H" when WDP is "1".
WDP is reset to "0" at the time of system reset or when the WDT counter overflows and is inverted whenever data is written to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (T_{WOV}), a watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period (TWOV) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter shown in Table 9-1.

Table 9-1 Clear Period of WDT Counter

WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	125 ms	Approx. 121 ms
0	1	500 ms	Approx. 496 ms
1	0	2000 ms	Approx. 1996 ms
1	1	8000 ms	Approx. 7996 ms

Figure 9-2 shows an example of watchdog timer operation.

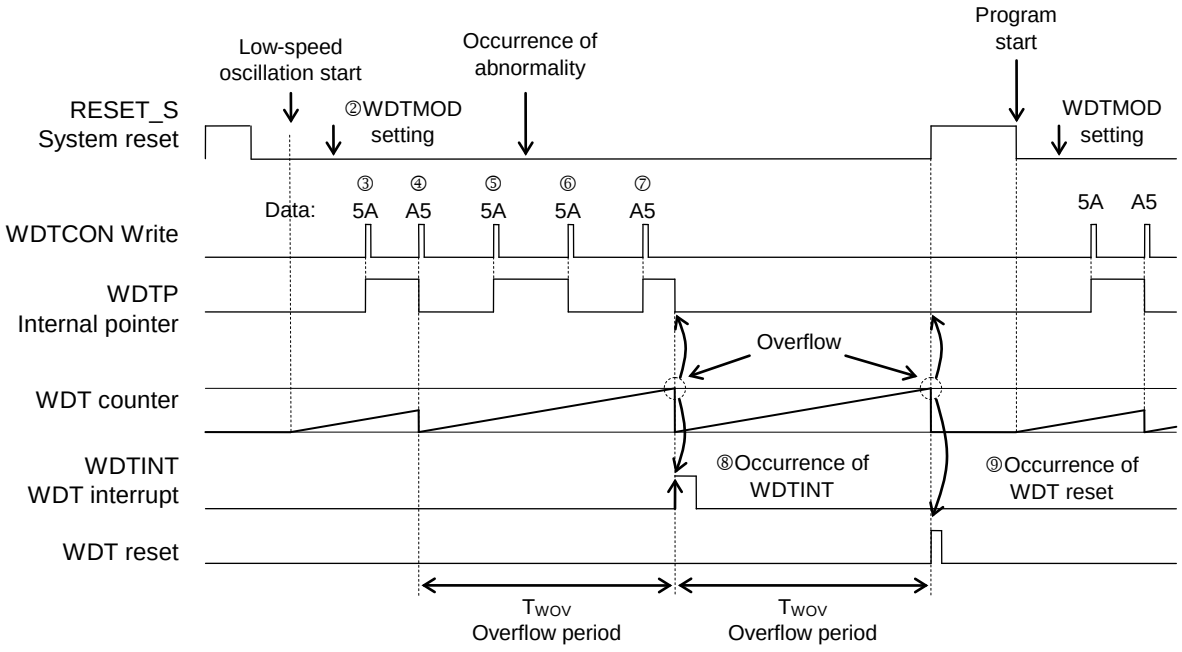


Figure 9-2 Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
② The overflow period of the WDT counter (TWOV) is set to WDTMOD.
③ "5AH" is written to WDTCON. (Internal pointer 0→1)
④ "0A5H" is written to WDTCON and the WDT counter is cleared. (Internal pointer 1→0)
⑤ "5AH" is written o WDTCON. (Internal pointer 0→1)
⑥ When "5AH" is written to WDTCON after the occurrence of abnormality, it cannot be accepted as the internal pointer is set to "1". (Internal pointer 1→0)
⑦ Although "0A5H" is written to WDTCON, the WDT counter is not cleared since the internal pointer is "0" and the writing of "5AH" is not accepted in ⑥. (Internal pointer 0→1)
⑧ The WDT counter overflows and a watchdog timer interrupt request (WDTINT) is generated. In this case,, the WDT counter and the internal pointer (WDP) are initialiaed for a half cycle of low speed clock (about 15.26us).
⑨ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

Note:
- In STOP mode, the watchdog timer operation also stops.
- In HALT mode, the watchdog timer operation does not stop. When the WDT interrupt occurs, the HALT mode is released.
- The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

9.3.1 Handling example when you do not want to use the watch dog timer

WDT counter is a free-run counter that starts count-up automatically after the system reset released and the low-speed clock (LSCLK) starts oscillating. If the WDT counter gets overflow, the WDT non-maskable interrupt occurs and then a system reset occurs. Therefore, it is needed to clear the WDT counter even if you do not want to use the WDT as a fale-safe function.
See following example programming codes to clear the WDT counter in the interrupt routine.

Example programming code:

```
__DI();                    // Disable multi-interrupts
do
{
   WDTCON = 0x5a;
} while(WDP != 1)
WDTCON = 0xa5;
 __EI();
```

Chapter 10

PWM

10 PWM

10.1 Overview

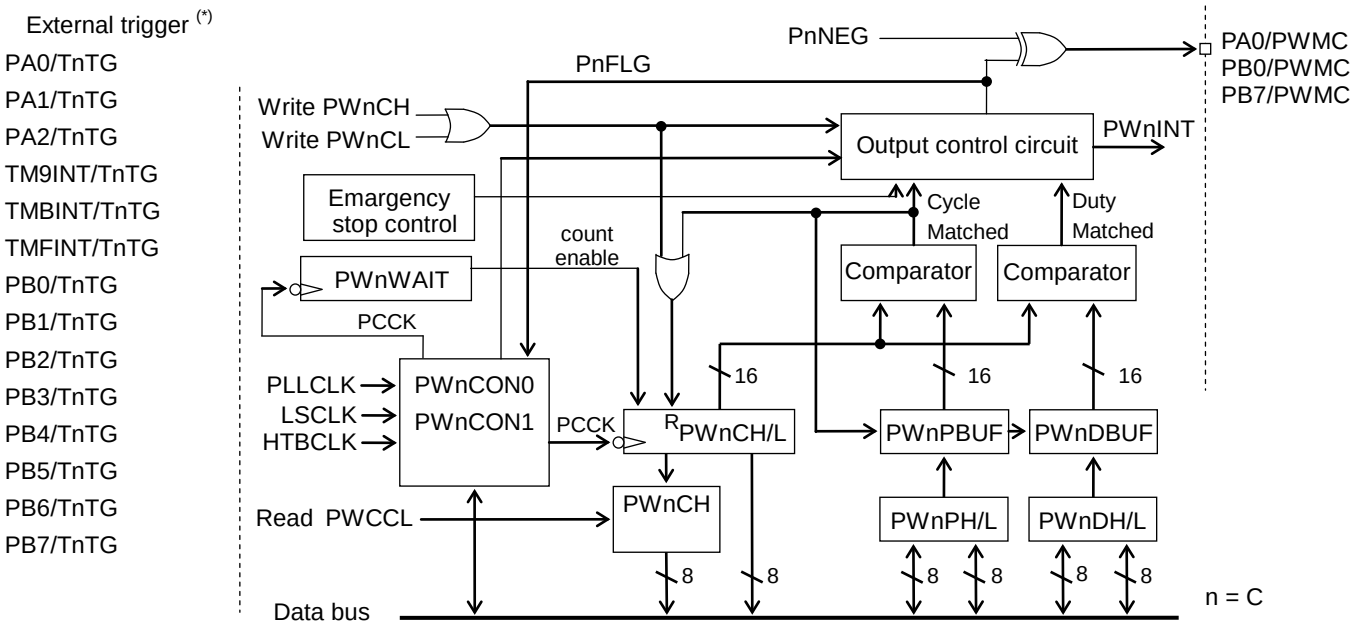
This LSI includes one channel of 16-bit PWM (Pulse Width Modulation).
The PWM output (PWM0) function is assigned to the secondary function of the PA0(Port A) or the secondary function of the PB0(Port B) or the fourthly function of the PB7(Port B).
For the functions of port A and port B, see Chapter 12, "Port A" and Chapter 13, "Port B".

10.1.1 Features

- The PWM signals with the periods of approximately 122 ns (@PLLCLK=16.384MHz) to 2s (@LSCLK=32.768kHz) can be generated and output outside of the LSI.
- The output logic of the PWM signal can be switched to the positive or negative logic.
- A PWM interruption (PWnINT) is caused at the time of a cycle & duty match at the time of a duty match at the time of a cycle match of a PWM signal.
- For the PWM clock, a low-speed clock (LSCLK), and a high-speed time base clock (HTBCLK), and a PLL oscillating clock (PLLCLK) are available.
- It is possible to set up the attack time of PWM.
- A changeover in repetition mode / one-shot mode is possible.
- PWM start/stop by the external trigger input (LSI input pin or Timer interrupt request can be selected as the external trigger input).
- An external input can generate an emergency stop and emergency stop interrupt.

10.1.2 Configuration

Figure 10 - 1 shows the configuration of the PWM circuit.



PWnPL: PWMn period register L
PWnPH: PWMn period register H
PWnPBUF: PWMn period buffer
PWnDL: PWMn duty register L
PWnDH: PWMn duty register H
PWnDBUF: PWMn duty buffer
PWnCL: PWMn counter register L
PWnCH: PWMn counter register H
PWnCON0: PWMn control register 0
PWnCON1: PWMn control register 1
PWnWAIT PWMn wait register

(n = C)

Figure 10-1 Configuration of PWM Circuit

10.1.3 List of Pins

Pin name	I/O	Description
PA0/ TnTG/ PWMC	I/O	External trigger input PWMC output pin Used for the secondary function of the PA0 pin.
PA1/ TnTG	I/O	External trigger input
PA2/ TnTG	I/O	External trigger input
CMP0/ TnTG	I	External trigger input Emergency stop input
CMP1/ TnTG	I	External trigger input Emergency stop input
TM9INT/ TnTG	I	External trigger input
TMBINT/ TnTG	I	External trigger input
TMFINT/ TnTG	I	External trigger input
PB0/ TnTG/ PWMC	I/O	External trigger input Emergency stop input PWMC output pin Used for the secondary function of the PB0 pin.
PB1/ TnTG	I/O	External trigger input
PB2/ TnTG	I/O	External trigger input
PB3/ TnTG	I/O	External trigger input
PB4/ TnTG	I/O	External trigger input
PB5/ TnTG	I/O	External trigger input
PB6/ TnTG	I/O	External trigger input
PB7/ TnTG/ PWMC	I/O	External trigger input PWMC output pin Used for the fourthly function of the PB70 pin.

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F910H	PWMC period register L	PWCPL	PWCP	R/W	8/16	0FFH
0F911H	PWMC period register H	PWCPH		R/W	8	0FFH
0F912H	PWMC duty register L	PWCDL	PWCD	R/W	8/16	00H
0F913H	PWMC duty register H	PWCDH		R/W	8	00H
0F914H	PWMC counter register L	PWCCL	PWCC	R/W	8/16	00H
0F915H	PWMC counter register H	PWCCH		R/W	8	00H
0F916H	PWMC control register 0	PWCCON0	PWCCON	R/W	8/16	00H
0F917H	PWMC control register 1	PWCCON1		R/W	8	40H
0F918H	PWMC control register 2	PWCCON2	PWCCON23	R/W	8/16	00H
0F919H	PWMC control register 3	PWCCON3		R/W	8	00H
0F91AH	PWMC wait register	PWCWAIT	−	R/W	8	00H

10.2.2 PWMC Period Registers (PWCPL, PWCPH)

Address: 0F910H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWCPL	PCP7	PCP6	PCP5	PCP4	PCP3	PCP2	PCP1	PCP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

Address: 0F911H
Access: R/W
Access size: 8 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
PWCPH	PCP15	PCP14	PCP13	PCP12	PCP11	PCP10	PCP9	PCP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	1	1	1	1	1	1	1	1

PWCPH and PWCPL are special function registers (SFRs) to set the PWMC periods.

Note:
When PWCPH or PWCPL is set to "0000H", the PWMC period buffer (PWCPBUF) is set to "0001H".
A word type transfer instruction should be used for register setting.

10.2.3 PWMC Duty Registers (PWCDL, PWCDH)

Address: 0F912H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCDL	PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F913H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCDH	PCD15	PCD14	PCD13	PCD12	PCD11	PCD10	PCD9	PCD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

PWCDH and PWCDL are special function registers (SFRs) to set the duties of PWMC.

Note:
Set PWCDH and PWCDL to values smaller than those to which PWCPH and PWCPL are set.
Please refer to "10.3 Description of operation" for the update of PWCDH,Lin a PWM busy.

10.2.4 PWMC Counter Registers (PWCCH, PWCCL)

Address: 0F914H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCL	PCC7	PCC6	PCC5	PCC4	PCC3	PCC2	PCC1	PCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

Address: 0F0915H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCDH	PCC15	PCC14	PCC13	PCC12	PCC11	PCC10	PCC9	PCC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

PWCCL and PWCCH are special function registers (SFRs) that function as 16-bit binary counters.
When data is written to either PWCCL or PWCCH, PWCCL and PWCCH is set to "0000H". The data that is written is meaningless.
When data is read from PWCCL, the value of PWCCH is latched. When reading PWCCH and PWCCL, use a word type instruction or pre-read PWCCL.

The contents of PWCCH and PWCCL during PWM operation cannot be read depending on the combination of the PWM clock and system clock. Table 10-1 shows PWCCH and PWCCL read enable/disable for each combination of the PWM clock and system clock.

Table 10-1 PWCCH and PWCCL Read Enable/Disable during PWMC Operation

PWM clock PCCK	System clock SYSCLK	PWCCH and PWCCL read enable/disable
LSCLK	LSCLK	Read enabled
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during counting, read consecutively PWCCH or PWCCL twice until the last data coincides the previous data.
HTBCLK	LSCLK	Read disabled
HTBCLK	HSCLK	Read enabled
PLL clock (16MHz)	LSCLK	Read disabled
	HSCLK	

10.2.5 PWMC Control Register 0 (PWCCON0)

Address: 0F916H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCON0	—	—	PCSDN	PCNEG	PCIS1	PCIS0	PCCS1	PCCS0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

PWCCON0 is a special function register (SFR) to control PWM.

[Description of Bits]

- **PCCS1, PCCS0** (bits 1, 0)
  The PCCS1 and PCCS0 bits are used to select the PWMC operation clocks. LSCLK, HTBCLK, or PLLCK can be selected.

PCCS1	PCCS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	PLLCK (16MHz)
1	1	Prohibited

- **PCIS1, PCIS0** (bits 3, 2)
  The PCIS1 and PCIS0 bits are used to select the point at which the PWMC interrupt occurs. "When the periods coincide", "when the duties coincide", or "when the periods and duties coincide" can be selected.

PCIS1	PCIS0	Description
0	0	When the periods coincide. (Initial value)
0	1	When the duties coincide.
1	*	When the periods and duties coincide.

- **PCNEG** (bit 4)
  The PCNEG bit is used to select the output logic. When the positive logic is selected, the initial value of PWMC output is "1", and when the negative logic is selected, the initial value of PWMC output is "0".

PCNEG	Description
0	Positive logic (initial value)
1	Negative logic

- **PCSDN** (bit 5)
  The PCSDN bit is used to select the forced stop of PWMC.

PCNEG	Description
0	PWMC normal operation (initial value)
1	PWMC forced stop

10.2.6 PWMC Control Register 1 (PWCCON1)

Address: 0F917H
Access: R/W
Access size: 8 bits
Initial value: 40H

	7	6	5	4	3	2	1	0
PWCCON1	PCSTAT	PCFLG	PCSDST	—	—	—	PCTGEN	PCRUN
R/W	R	R/W	R/W	R	R	R	R/W	R/W
At reset	0	1	0	0	0	0	0	0

PWCCON1 is a special function register (SFR) to control PWMC.

[Description of Bits]

- **PCRUN** (bit 0)
  The PCRUN bit is used to control count stop/start of PWMC.

PCRUN	Description
0	Stops counting. (Initial value)
1	Starts counting.

- **PCTGEN** (bit 1)
  The PCTGEN is a enable flag of the count stop/start by the external input of PWMC.

PCRUN	Description
0	The count stop/start by an external input is disabled. (Initial value)
1	The count stop/start by an external input is enabled.

- **PCSDST** (bit 5)
  The PCSDST bit indicates that an emergency stop interrupt has occurred.
  Write "1" to this bit to clear it.

PCSDST	Description
0	No emergency stop interrupt has occurred. (initial value)
1	An emergency stop interrupt has occurred.

- **PCFLG** (bit 6)
  The PCFLG bit is used to read the output flag of PWMC.
  This bit is set to "1" when write operation to PWCCH or PWCCL is performed,

PCFLG	Description
0	PWMC output flag = "0"
1	PWMC output flag = "1" (initial value)

- **PCSTAT** (bit 7)
  The PCSTAT bit indicates "counting stopped or "counting in progress" of PWMC.

PCSTAT	Description
0	Counting stopped. (Initial value)
1	Counting in progress.

Note:

For normal (continuous) PWM mode, when the PWM count is stopped by the external trigger input and the interrupt is generated, PCRUN bit shows "0" as is controlled to stop counting. When the PWM duty or period interrupt is generated, PCRUN bit shows "1" as is controlled to start (keep) counting. Therefore, reading PCRUN bit can be used for recognizing which interrupt occurred.

For one shot PWM mode, when the PWM count is stopped by the external trigger input and the interrupt is generated, PCRUN bit shows "0" as is controlled to stop counting. When the PWM period interrupt is generated, PCRUN bit also shows "0" as is controlled to stop counting. To recognizing which interrupt occurred, read timer PWM counter register and PWM period register and check if the PWM counter register value is consistent with PWM period register value. When the PWM duty interrupt is generated, PCRUN bit also shows "1" as is controlled to start (keep) counting. Therefore, reading PCRUN bit can be used for recognizing which interrupt occurred.

When the PWM count is stopped by the external trigger and PCRUN bit shows "0", make sure to start the next operation after PCSTAT bit shows "0" as the PWM count is stopped.

10.2.7 PWMC Control Register 2 (PWCCON2)

Address: 0F918H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCON2	PCOST	—	PCTRM1	PCTRM0	—	PCEXCL	PCST1	PCST0
R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

PWCCON2 is a special function register (SFR) to control PWM.
Rewrite PWCCON2 while the PWMC is stopped (PCSTAT of the PWCCON1 register is "0") and the PWM C stop/start by the external trigger is disabled (PCTGEN of the PWCCON1 register is "0").

※When rewrite PWCCON2 while the PWM C stop/start by the external trigger is enabled (PCTGEN of the PWCCON1 register is "1"), refer to the following "Note".

[Description of Bits]

- **PCST1, PCST0** (bits 1, 0)
  The PCST1 and PCST0 bits are used to select the start/stop mode of the PWMC counter.

PCST1	**PCST0**	Description
		Counter operation using the external input
0	0	Do not operate (initial value)
0	1	Start counting
1	0	Stop counting
1	1	Start/stop counting

- **PCEXCL** (bit 2)
  The PCEXCL bit is used to select whether or not to clear the PWMC counter when stopped by the external input (PCST1 is set to "1"). Set PCEXCL to "1" to clear the counter when stopped by the external input.

PCEXCL	Description
0	Does not clear the counter when it is stopped by the external trigger. (initial value)
1	Clears the counter when it is stopped by the external trigger.

- **PCTRM1, PCTRM0** (bits 5, 4)
  The PCTRM1 and PCTRM0 bits are used to select the count start/stop mode of PWMC.
  This is valid only when the external input start and stop are selected.
  When the timer interrupt (TM9INT/TMBINT/TMFINT) is selected for the external input with the PWCCON3 register, be sure to select the rising edge start and the rising edge stop (set PCTRM1 to "0" and PCTRM0 "0"). Do not use other settings (The operation cannot be guaranteed because they may cause the count start/stop at timings other than interrupts).

PCTRM1	**PCTRM0**	Description	
		Rising edge	Falling edge
0	0	Start/stop (initial value)	—
0	1	Stop	Start
1	0	Start	Stop
1	1	—	Start/stop

- **PCOST** (bit 7)
  The PCOST bit is used for the operation mode of the PWMC.
  If PCOST is set as "1", one-shot PWM mode can be used.

PCOST	Description
0	Normal timer mode (initial value)
1	One shot timer mode

Note:
The note point of when rewrite PWCCON2 while the PWM C stop/start by the external trigger is enabled (PCTGEN of the PWCCON1 register is "1").

- When rewrite the PCST1 and PCST0 bits, rewrite PCST0 while the PWM C is run (PCSTAT of the PWCCON1 register is "1") and rewrite PCST1 while the PWM C is stopped (PCSTAT of the PWCCON1 register is "0").
- When rewrite the PCTRM1 and PCTRM0 bits, rewrite PCTRM0 while the PWM C is run (PCSTAT of the PWCCON1 register is "1") and rewrite PCTRM1 while the PWM C is stopped (PCSTAT of the PWCCON1 register is "0").
- When rewrite the PCOST bit, rewrite PCOST while the PWM C is run (PCSTAT of the PWCCON1 register is "1").

10.2.8 PWMC Control Register 3 (PWCCON3)

Address: 0F919H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCCON3	—	—	PCSDE1	PCSDE0	PCSTSS	PCSTS2	PCSTS1	PCSTS0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

PWCCON3 is a special function register (SFR) to control PWM.
Rewrite PWCCON3 while the PWMC is stopped (PCSTAT of the PWCCON1 register is "0") and the PWM C stop/start by the external trigger is disabled (PCTGEN of the PWCCON1 register is "0").

[Description of Bits]

- PCSTSS, PCSTS2, PCSTS1, PCSTS0 (bits 3 to 0)
  The PCSTSS, PCSTS2, PCSTS1, and PCSTS0 bits are used to select the external input start/stop pins of PWMC.

PCSTS2	**PCSTS1**	**PCSTS0**	Description	
			When PCSTSS="0" (initial value)	When PCSTSS="1"
0	0	0	PA0 pin (initial value)	PB0 pin
0	0	1	PA1 pin	PB1 pin
0	1	0	PA2 pin	PB2 pin
0	1	1	Prohibited (*)	PB3 pin
1	0	0	Prohibited (*)	PB4 pin
1	0	1	TM9INT (Timer 9 interrupt)	PB5 pin
1	1	0	TMBINT (Timer B interrupt)	PB6 pin
1	1	1	TMFINT (Timer F interrupt)	PB7 pin

(*) Because no external trigger signal will be input, external triggers cannot start/stop the timer.
(*1) When a timer interrupt request is set as the external trigger signal, there are some restrictions on the edge selection of the PWM start/stop triggers. For details, see the description of the PWCCON2 register. The timer interrupt requests (TM9INT/TMBINT/TMFINT) are interrupt request signals from the timer 9/timer B/timer F, independent of the interrupt enable/disable settings by the interrupt enable registers 3/5 (IE3/5).

- **PCSDE1, PCSDE0** (bits 5 to 4)
  The PSDE1, PSDE0 bits are used to select the emergency stop input pins of PWMC.

PCSDE1	PCSDE0	Description
0	0	Disables the emergency stop (initial value)
0	1	Rising edge of the CMP0 (Comparator 0)
1	0	Rising edge of the CMP1 (Comparator 1)
1	1	Rising edge of PB0

Note:

For normal (continuous) PWM mode, when the PWM count is stopped by the external trigger input and the interrupt is generated, PCRUN bit shows "0" as is controlled to stop counting.

The external trigger input pin and the emergency stop input pins aren't to select the same pin. When it is selected, PWM doesn't operate.

10.2.9 PWMC Wait Register (PWCWAIT)

Address: 0F91AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PWCWAIT	PCW7	PCW6	PCW5	PCW4	PCW3	PCW2	PCW1	PCW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0

PWCCON0 is a special function register (SFR) to control PWM.
PWCWAIT is a special function register (SFR) to set the time for PWMC to actually start operating after the PWCCON1 PCRUN bit is set.
When the PCRUN bit is set, the 8-bit binary counter starts operating to count up to the PWCWAIT value. When the 8-bit binary counter reaches the PWCWAIT value, PWMC starts operating.
The operation clock of the 8-bit binary counter is selected by PWCCON0 PCCS1,0.
This function is enabled when PWCWAIT is set to a value other than 00H. When PWCWAIT is set to 00H, the PCRUN bit starts the PWMC operation.
While PWMWAIT is valid (until PnSTAT is set to "1"), the external input stop is invalid. But, the emergency stop function is valid.

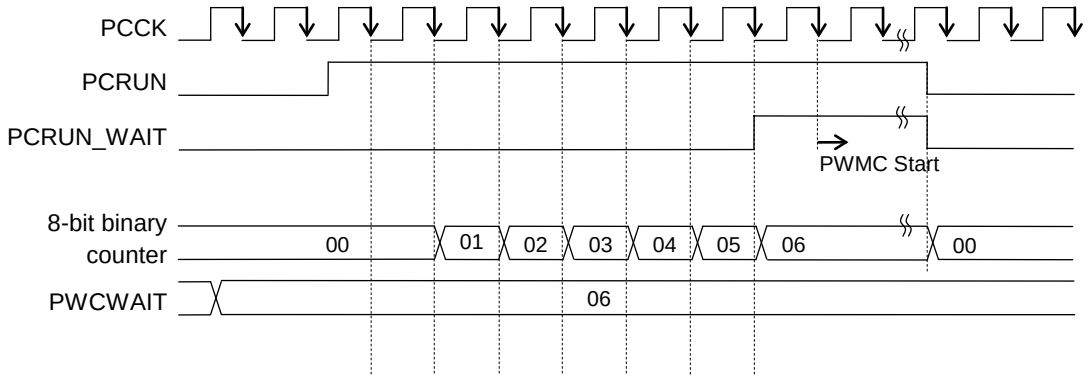


Figure 10-2 Operation Timing Diagram of PWCWAIT

10.3 Description of Operation

When the PnRUN bit of the PWMn control register 1 (PWnCON1) is set to "1", the PWMn counters (PWnCH, PWnCL) are set to an operating state (PnSTAT is set to "1") on the first falling edge of the PWMn clock (PnCK) that is selected by the PWMn control register 0 (PWnCON0) and increment the count value on the 2nd falling edge.

When the count value of the PWnCH and PWnCL counter registers coincides the value of the PWMn duty buffer (PWnDBUF), the PWMn flag (PnFLG) is set to "0" on the next timer clock falling edge of PnCK.
When the PWnCH and PWnCL count values coincide the PWMn period buffer value (PWnPBUF), the PnFLG becomes "1" at the next PnCK falling edge, and the PWnCH and PWnCL are reset to "0000H" to continue counting. At the same time, the value of the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF) and the value of PWMn period register (PWnPH, PWnPL) to the PWMn period buffer (PWnPBUF).

When the PnRUN bit is set to "0", the PWnCH and PWnCL counter registers stop counting after counting once the falling of the PWMn clock (PnCK). To confirm that PWnCH and PWnCL are stopped, check that the PnSTAT bit of the PWMn control register 1 (PWnCON1) is "0". When the PnRUN bit is set to "1" again, the PWnCH and PWnCL counter registers restarts incremental counting from the previous value on the falling edge of PnCK.

To initialize the PWnCH and PWnCL counter registers to "0000H", perform write operation in either of PWnCH or PWnCL. At that time, PnFLG is also set to "1".
During count stop (PnRUN is "0"), data written in the PWMn duty register (PWnDH, PWnDL) is transferred to the PWMn duty buffer (PWnDBUF), and data written in the PWMn period register (PWnPH, PWnPL) is transferred to the PWMn period buffer (PWnPBUF).

The PWMn clock, the point at which an interrupt of PWMn occurs, and the logic of the PWMn output are selected by PWMn control register 0 (PWnCON0).

The period of the PWMn signal (TPWP) and the first half duration (TPWD) of the duty are expressed by the following equations.

$$T_{PWP} = \frac{PWnP + 1}{PnCK\ (Hz)}$$

$$T_{PWP} = \frac{PWnD + 1}{PnCK\ (Hz)}$$

PWnP: PWMn period registers (PWnPH, PWnPL) setting value (0001H to 0FFFFH)
PWnD: PWMn duty registers (PWnDH, PWnDL) setting value (0000H to 0FFFEH)
PnCK: Clock frequency selected by the PWMn control register 0 (PWnCON0)

(n=C)

After the PnRUN bit is set to "1", counting starts in synchronization with the PWMn clock. This causes an error of up to 1 clock pulse to the time the first PWMn interrupt is issued. The PWMn interrupt period from the second time is fixed.
Figure 10-3 shows the operation timing of PWMn.
For the timing chart of PnRUN_WAIT, see Figure 10-2.

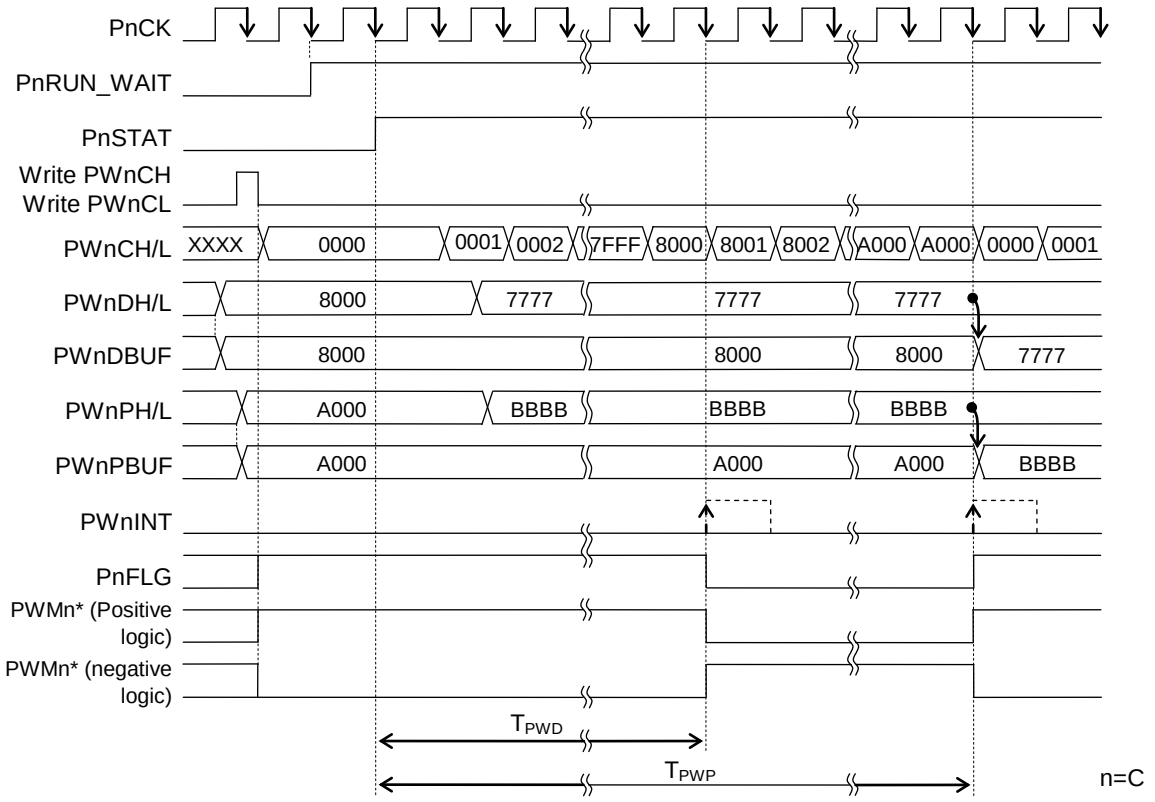


Figure 10-3 (1/2) Operation Timing Diagram of PWMC

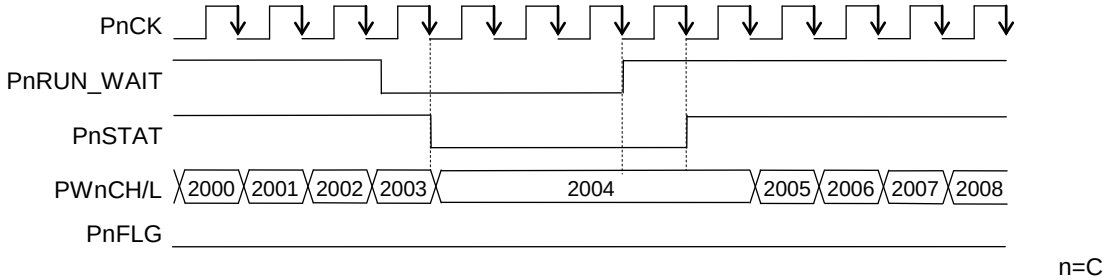


Figure 10-3 (2/2) Operation Timing Diagram of PWMC

Note:
Even if "0" is written to the PnRUN bit, counting operation continues up to the falling edge (the PWMn status flag (PnSTAT) is in a "1" state) of the next PWMn clock pulse. Therefore, the PWMn interrupt (PWnINT) may occur.
An external-triggering stop becomes invalid after setting a PnRUN bit during a PWM stop "1" until PnSTAT is set to "1." Moreover, an external-triggering start becomes invalid after making a PnRUN bit a PWM busy "0" until PnSTAT is set to "0."

10.3.1 Start, Stop, and Clear Operations of PWMC by External Input Control

For the external timer start/stop operation of the PWMC, the external timer start/stop is enabled when the external input is selected on PWMn control register 2(PWnCON2) and the PWMn control register 3(PWnCON3) and PnTGEN bit of PWMn control register 1(PWnCON1) is set as "1". From the external input, pulses shorter than one sampling clock are removed as noises. The sampling clock is selected by the PnCS1 and PnCS0 bits.
Figure 10-4 shows the timing of sampling of the external input.

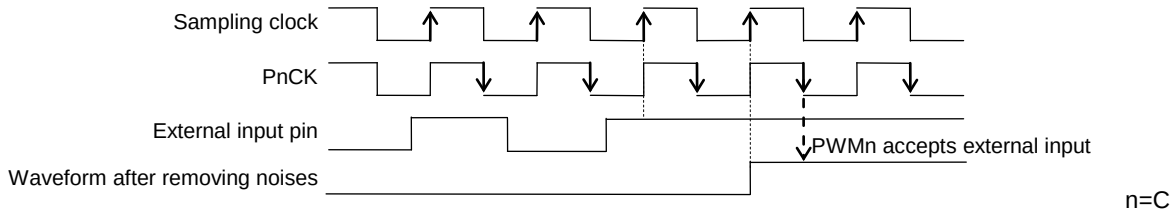


Figure 10-4 Timing Diagram of sampling of the external input

10.3.2 Emergency Stop Operation

Setting the PnSDE1 and PnSDE0 bits of the PWMn control register 3 (PWnCON3) enables the emergency stop function.

When the external input gets an edge input, the emergency stop flag (PnSDST) is set to "1", an emergency stop interrupt (PWnINT) is generated, and the PWM counter is stopped/cleared. Because the PWM flag output (PnFLG) is cleared, the PWMn outputs are turned off simultaneously.

To release the emergency stop flag, write "1" to PnSDST of the PWMn control register 3 (PWnCON3).
Figure 10-5 shows the operation timing.

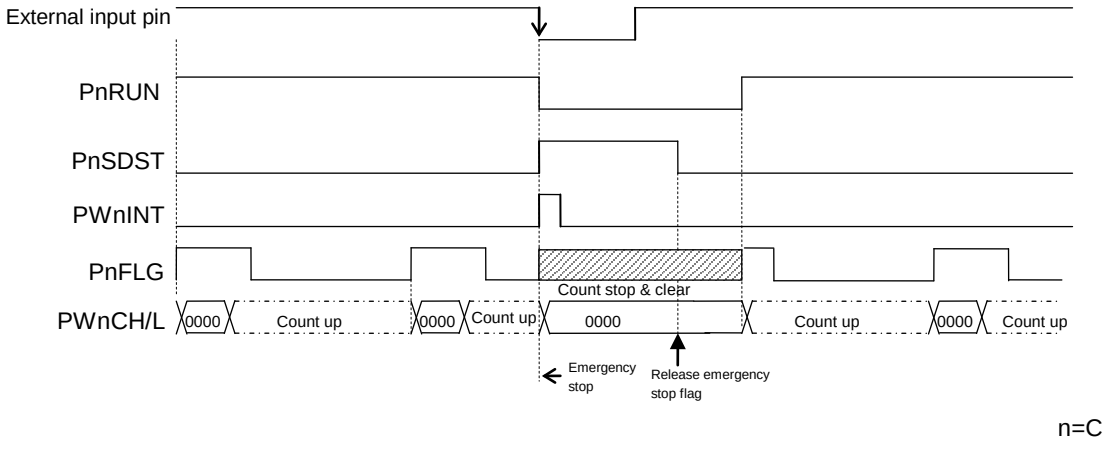


Figure 10-5 Operation Timing Diagram by Emergency Stop

10.4 Specifying port registers

To enable the PWM function, the applicable bit of each related port register needs to be set. See Chapter 12, "Port A" and Chapter 13, "Port B" for detail about the port registers.

10.4.1 Functioning PA0 (PWMC) as the PWM output

Set PA0MD1 bit (bit0 of PAMOD1 register) to "0", and set PA0MD0 bit (bit0 of PAMOD0 register) to "1" and set PA0DIR bit(bit0 of PADIR register) to "0", for specifying the PWM output as the secondary function of PA0.

Reg. name	PAMOD1 register (Address: 0F255H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	PA2MD1	PA1MD1	**PA0MD1**
Data	-	-	-	-	-	*	*	**0**

Reg. name	PAMOD1 register (Address: 0F254H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	PA2MD0	PA1MD0	**PA0MD0**
Data	-	-	-	-	-	*	*	**1**

Set PA0C1 bit (bit0 of PACON1 register) to "1" and set PA0C0 bit(bit0 of PACON0 register) to "1", for specifying the PA0 as CMOS output.

Reg. name	PACON1 register (Address: 0F253H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	PA2C1	PA1C1	**PA0C1**
Data	-	-	-	-	-	*	*	**1**

Reg. name	PACON0 register (Address: 0F252H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	PA2C0	PA1C0	**PA0C0**
Data	-	-	-	-	-	*	*	**1**

Reg. name	PADIR register (Address: 0F251H)							
Bit	7	**6**	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	PA2DIR	PA1DIR	**PA0DIR**
Data	-	-	-	-	-	*	*	**0**

Data of PA0D bit (bit0 of PAD register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	PAD register (Address: 0F250H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	PA2D	PA1D	**PA0D**
Data	-	-	-	-	-	*	*	**

- : Bit does not exist.
* : Bit not related to the PWM function
** : Don't care the data.

10.4.2 Functioning PB0 (PWMC) as the PWM output

Set PB0MD1 bit (bit0 of PBMOD1 register) to "0", and set PB0MD0 bit (bit0 of PBMOD0 register) to "1" for specifying the PWM output as the secondary function of PB0

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	**PB0MD0**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	**PB0MD1**
Data	*	*	*	*	*	*	*	**0**

Set PB0C1 bit (bit0 of PBCON1 register) to "1", set PB0C0 bit(bit0 of PBCON0 register) to "1" and set PB0DIR bit(bit0 of PBDIR register) to "0", for specifying the PB0 as CMOS output.

Reg. name	PBCON1 register (Address: 0F23BH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C1	PB6C1	P35C1	PB4C1	PB3C1	PB2C1	PB1C1	**PB0C1**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBCON0 register (Address: 0F23AH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	**PB0C0**
Data	*	*	*	*	*	*	*	**1**

Reg. name	PBDIR register (Address: 0F239H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PBBDIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	**PB0DIR**
Data	*	*	*	*	*	*	*	**0**

Data of PB0D bit (bit0 of PBD register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F238H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	**PB0D**
Data	*	*	*	*	*	*	*	******

- : Bit does not exist.
* : Bit not related to the PWM function
** : Don't care the data.

10.4.3 Functioning PB7 (PWMC) as the PWM output

Set PB7MD1 bit (bit7 of PBMOD1 register) to "1", and set PB7MD0 bit (bit7 of PBMOD0 register) to "1" for specifying the PWM output as the fourthly function of PB7

Reg. name	PBMOD0 register (Address: 0F25CH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7MD0**	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBMOD1 register (Address: 0F25DH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7MD1**	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Data	**1**	*	*	*	*	*	*	*

Set PB7C1 bit (bit7 of PBCON1 register) to "1", set PB7C0 bit(bit7 of PBCON0 register) to "1" and set PB7DIR bit(bit7 of PBDIR register) to "0", for specifying the PB7 as CMOS output.

Reg. name	PBCON1 register (Address: 0F25BH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C1**	PB6C1	P35C1	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBCON0 register (Address: 0F25AH)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7C0**	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
Data	**1**	*	*	*	*	*	*	*

Reg. name	PBDIR register (Address: 0F259H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PBBDIR**	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Data	**0**	*	*	*	*	*	*	*

Data of PB7D bit (bit7 of PBD register) does not affect to the PWM output function, so don't care the data for the function.

Reg. name	PBD register (Address: 0F258H)							
Bit	**7**	6	5	4	3	2	1	0
Bit name	**PB7D**	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	PB0D
Data	******	*	*	*	*	*	*	*

- : Bit does not exist.
* : Bit not related to the PWM function
** : Don't care the data.

Chapter 11

UART

11 UART

11.1 Overview

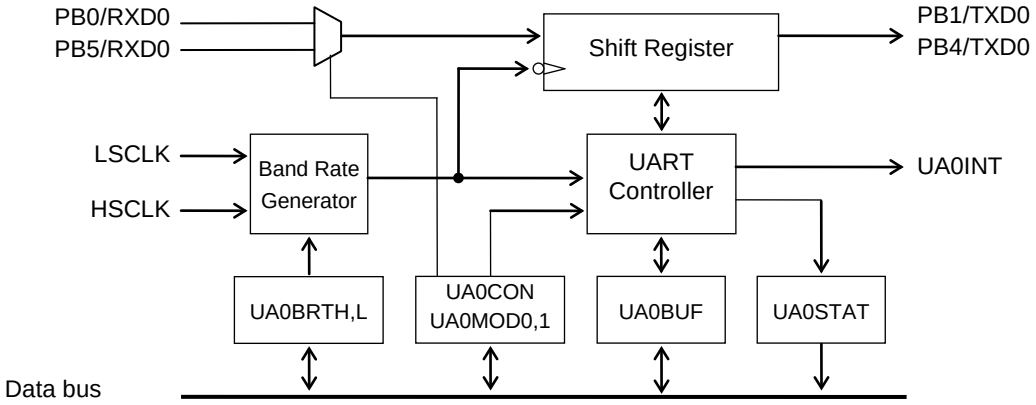
This LSI includes 1 channel of UART (Universal Asynchronous Receiver Transmitter) which is an asynchronous serial interface.
For the input clock, see Chapter 6, "Clock Generation Circuit".
The use of UART requires setting of the tertiary functions of Port B. For the tertiary functions of Port B, see Chapter 13, "Port B".

11.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable.
- Odd parity, even parity, or no parity selectable.
- 1 stop bit or 2 stop bits selectable.
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic.
- LSB first or MSB first selectable as a communication direction.
- Communication speed: Settable within the range of 200bps to 38400bps.
- Built-in baud rate generator.

11.1.2 Configuration

Figure 11-1 shows the configuration of the UART.



UA0BUF : UART0 transmit/receive buffer
UA0BRTH,L : UART0 baud rate H and L are:
UA0CON : UART0 control register
UA0MOD0,1 : UART0 mode registers 0 and 1
UA0STAT : UART0 status register

Figure 11-1 Configuration of UART

11.1.3 List of Pins

Pin name	I/O	Function
PB0/RXD0	I	UART0 data input pin Used for the primary function of the PB0 pin.
PB5/RXD0	I	UART0 data input pin Used for the primary function of the PB5 pin.
PB1/TXD0	O	UART0 data output pin Used for the tertiary function of the PB1 pin.
PB4/TXD0	O	UART0 data output pin Used for the tertiary function of the PB4 pin.

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F290H	UART0 transmit/receive buffer	UA0BUF	−	R/W	8	00H
0F291H	UART0 control register	UA0CON	−	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	−	R/W	8	00H

11.2.2 UART0 Transmit/Receive Buffer (UA0BUF)

Address: 0F290H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) to store the transmitted/received data of the UART.
In transmit mode, write transmission data to UA0BUF. To transmit the data consecutively, confirm the U0FUL flag of the UART0 status register (UA0STAT) becomes "0", then write the next transmitted data to the UA0BUF. Any value written to UA0BUF can be read.
In receive mode, since data received at termination of reception is stored in UA0BUF, read the contents of UABUF using the UART0 interrupt at termination of reception. At continuous reception, BA0BUF is updated whenever reception terminates. Any write to BA0BUF is disabled in receive mode.
The bits, which are not required when any of the 5- to 8-bit data length is selected, become invalid in transmit mode and are set to “0” in receive mode.

Note:
For operation in transmit mode, be sure to set the transmit mode (UA0MOD0 and UA0MOD1) before setting the transmitted data in UAOBUF.

11.2.3 UART0 Control Register (UA0CON)

Address: 0F291H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	—	—	—	—	—	—	—	U0EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) to start/stop communication of the UART.

[Description of Bits]

- **U0EN** (bit 0)
  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate reception, set the bit to "0" by software.

U0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

11.2.4 UART0 Mode Register 0 (UA0MOD0)

Address: 0F292H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD0	−	−	−	U0RSEL	−	U0CK1	U0CK0	U0IO
R/W	R	R	R	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD0 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0IO** (bit 0)
  The U0IO bit is used to select transmit or receive mode.

U0IO	Description
0	Transmit mode (initial value)
1	Receive mode

- **U0CK1, U0CK0** (bits 2, 1)
  The U0CK1 and U0CK0 bits are used to select the clock to be input to the baud rate generator of the UART0.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	LSCLK
1	*	HSCLK

- **U0RSEL** (bit 4)
  The U0RSEL bit is used to select the received data input pin for the UART0.

U0RSEL	Description
0	Selects the PB0 pin. (Initial value)
1	Selects the PB5 pin.

Note:
・Always set the UA0MOD0 register while communication is stopped, and do not rewrite it during communication.

11.2.5 UART0 Mode Register 1 (UA0MOD1)

Address: 0F293H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD1	—	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD1 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]

- **U0LG1, U0LG0** (bits 1, 0)
  The U0LG1 and U0LG0 bits are used to specify the data length in the communication of the UART.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U0PT1, U0PT0** (bits 3, 2)
  The U0PT1 and U0PT0 bits are used to select “even parity”, odd parity”, or “no parity” in the communication of the UART.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0STP** (bit 4)
  The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bits

- **U0NEG** (bit 5)
  The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0DIR** (bit 6)
  The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
Always set the UA0MOD1 register while communication is stopped, and do not rewrite it during communication.

11.2.6 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH)

Address: 0F294H
Access: R/W
Access size: 8/16 bit
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F295H
Access: R/W
Access size: 8-bit
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA0BRTH	—	—	—	—	U0BR11	U0BR10	U0BR9	U0BR8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRTL and UA0BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 11.3.2, “Baud Rate”.

Note:
Always set the UA0BRTL and UA0BRTH registers while communication is stopped, and do not rewrite them during communication.

11.2.7 UART0 Status Register (UA0STAT)

Address: 0F296H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	—	—	—	—	U0FUL	U0PER	U0OER	U0FER
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART.
When any data is written to UA0STAT, all the flags are initialized to "0".

[Description of Bits]

- **U0FER** (bit 0)
  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U0FER bit is set to "1". This bit is updated each time reception is completed.
  The U0FER bit is fixed to "0" in transmit mode.

U0FER	Description
0	No framing error (initial value)
1	With framing error

- **U0OER** (bit 1)
  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" if the previously received data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U0OER bit is fixed to "0" in transmit mode.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0PER** (bit 2)
  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U0PER is updated whenever data is received.
  The U0PER bit is fixed to "0" in transmit mode.

U0PER	Description
0	No parity error (initial value)
1	Parity error

- **U0FUL** (bit 3)
  The U0FUL bit is used to indicate the state of the transmit/receive buffer of the UART.
  When the transmitted data is written in UA0BUF in transmit mode, this bit is set to “1” and when this transmitted data is transferred to the shift register, this bit is set to “0”. To transmit the data consecutively, confirm the U0FUL flag becomes "0", then write the next transmitted data to the UA0BUF.
  The U0FUL bit is fixed to “0” in receive mode.

U0FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

11.3 Description of Operation

11.3.1 Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, “with parity bit”, “without parity bit”, “even parity”, or “odd parity” can be selected. For the stop bit, “1 stop bit” or “2 stop bits” are available and for the transfer direction, “LSB first” or “MSB first” are available for selection. For serial input/output logic, positive logic or negative logic can be selected.
All these options are set with the UART0 mode register (UA0MOD1).
Figure 11-2 and Figure 11-3 show the positive logic input/output format and negative logic input/output format, respectively.

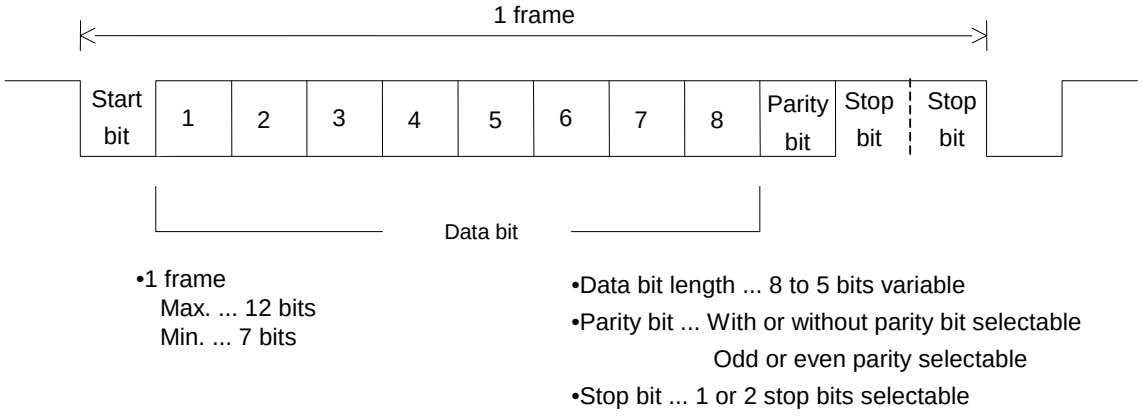


Figure 11-2 Positive Logic Input/Output Format

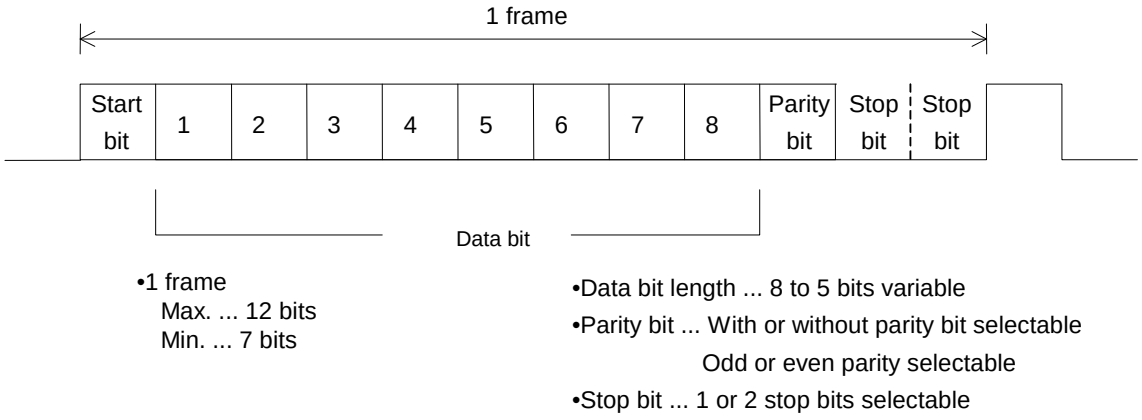


Figure 11-3 Negative Logic Input/Output Format

11.3.2 Baud rate

Baud rates are generated by the baud generator.
The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (U0CK1, U0CK0) of the UART0 mode register 0 (UA0MOD0). The count value of the baud rate generator can be set by writing it in the UART0 baud rate register H or L (UA0BRTH, UA0BRTL). The maximum count is 4096.
The setting values of UA0BRTH and UA0BRTL are expressed by the following equation.

$$\text{UA0BRTH, L} = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 11-2 lists the count values for typical baud rates.

Table 11-2 Count Values for Typical Baud Rates

Baud rate	Baud rate generator Clock selection			Baud rate generator counter value				Error [%]
	Baud rate Clock	U0CK1	U0CK0	Count value	Period of one bit	UA0BRTH	UA0BRTL	
1200bps	32.768kHz	0	0	27	Approximately 824us	00H	1AH	1.1
2400bps	32.768kHz	0	0	14	Approximately 427us	00H	0DH	-2.5
	8.192MHz	1	*	3413	Approximately 412us	0DH	054H	0.01
4800bps	8.192M Hz	1	*	1707	Approximately 208us	06H	0AAH	-0.02
9600bps	8.192M Hz	1	*	853	Approximately 104us	03H	054H	0.04
19200bps	8.192M Hz	1	*	427	Approximately 52us	01H	0AAH	-0.08
38400bps	8.192M Hz	1	*	213	Approximately 26us	00H	0D4H	0.16

Note:
When UA0BRTH or UA0BRTL is set to a value equal to less than “0007H”, the value set is read from UA0BRTH or UA0BRTL but the value of the baud rate clock counter is the same as the value when UA0BRTH or UA0BRTL is set to “0008H”.

11.3.3 Transmitted Data Direction

Figure 11-4 shows the relationship between the transmit/receive buffer and the transmitted/received data.

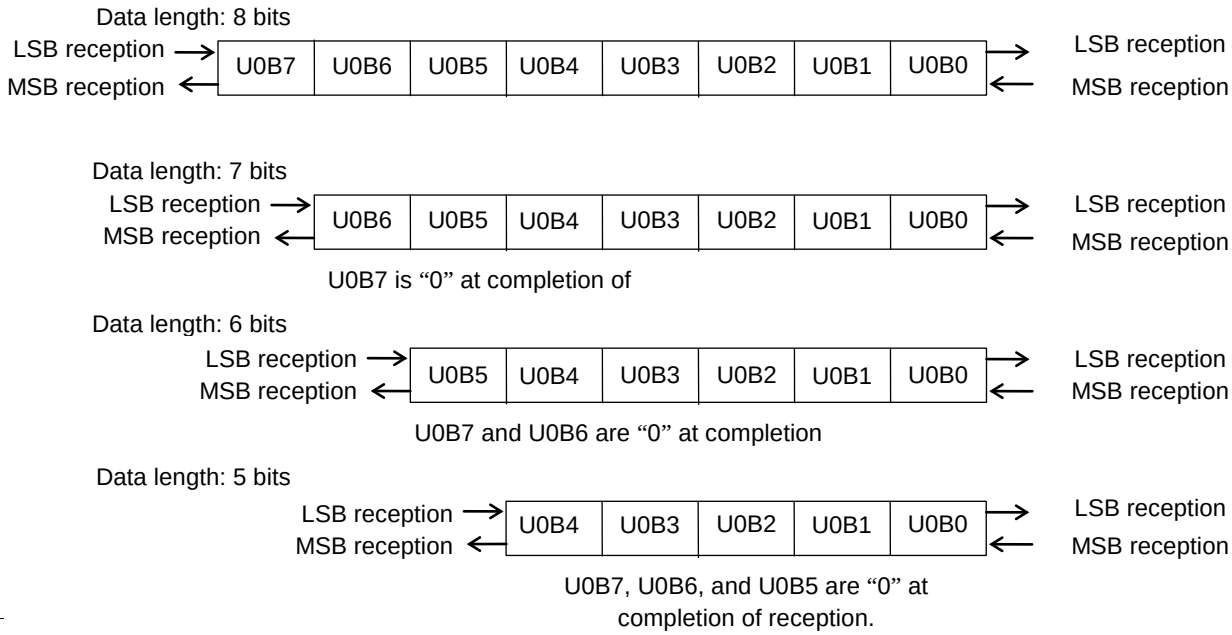


Figure 11-4 Relationship between Transmit/Receive Buffer and Transmitted/Received Data

Note:
When the TXD0 pin is set to serve the secondary function output in receive mode, "H" level is output from the TXD0 output.

11.3.4 Transmit Operation

Transmission is started by setting the U0IO bit of the UART0 mode register 0 (UA0MOD0) to "0" to select transmit mode and setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 11-5 shows the operation timing for transmission.

When the U0EN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmission.
The start bit is output to the TXD0 pin by the falling edge of the internal transfer clock (②). Subsequently, the transmitted data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UART0 interrupt is requested. In the UART0 interrupt routine, the next data to be transmitted is written to the transmit/receive buffer (UA0BUF).
When the next data to be transmitted is written to the transmit/receive buffer (UA0OBUF), the transmit buffer status flag (U0FUL) is set to "1" (③) and a UART0 interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. If the UART0 interrupt routine is terminated without writing the next data to the transmit/receive buffer, the U0FUL bit is not set to "1" (⑤) and transmission continues up to the transmission of the stop bit, then the U0EN bit is reset to "0" and a UART0 interrupt is requested.
The valid period for the next transmit data to be written to the transmit/receive buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)

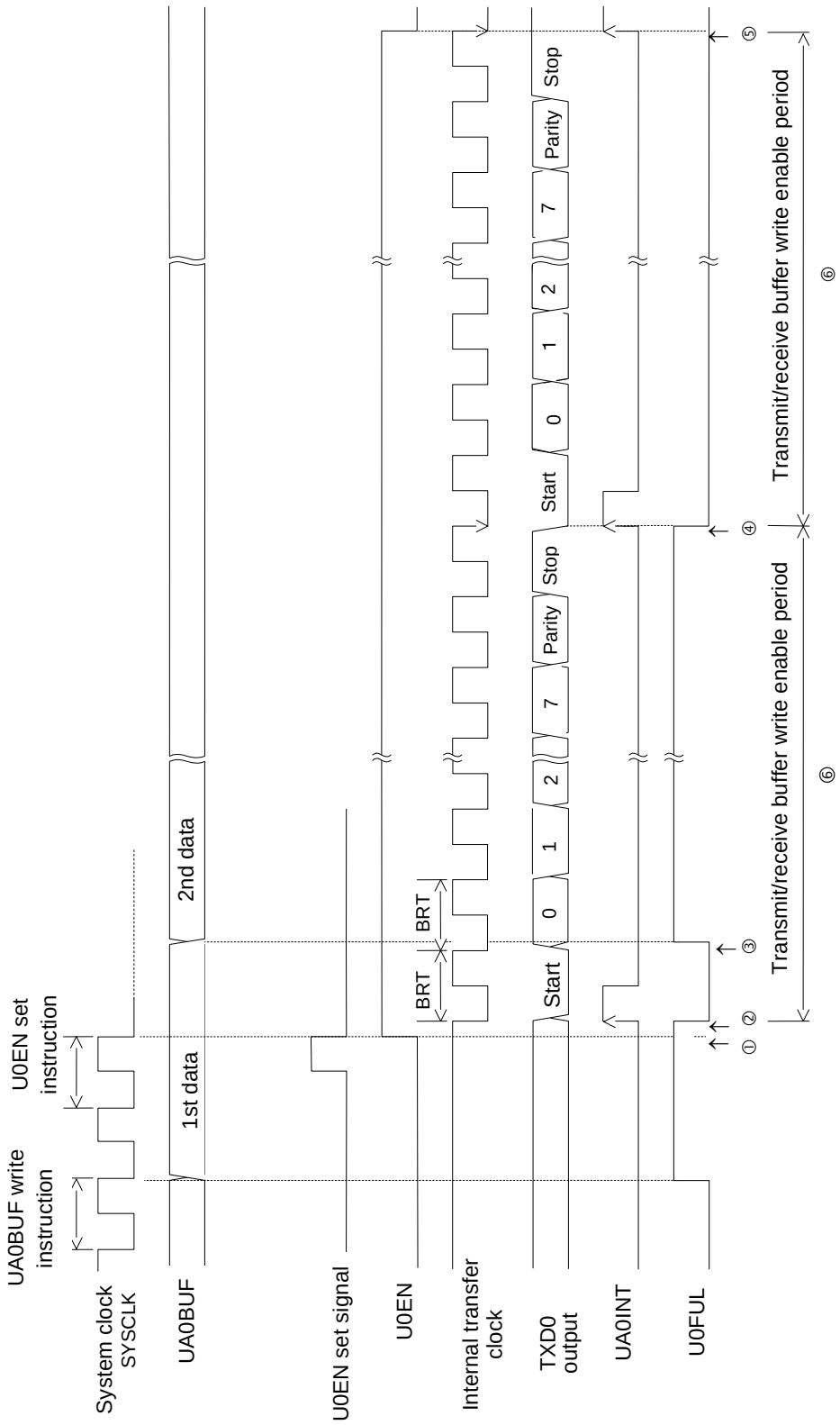


Figure 11-5 Operation Timing in Transmission

11.3.5 Receive Operation

Select the received data pin using the U0RSEL bit of the UART0UART0 mode register 0 (UA0MOD0). Select the receive mode by setting the U0IO bit of the UART0 mode register 0 (UA0MOD0) to "1". Then, set the U0EN bit of the UART0 control register (UA0CON) to "1" to start receiving data.
Figure 11-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXD0 and waits for the arrival of a start bit.
When detecting a start bit (①), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXD on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit received data is transferred to the transmit/receive buffer (UA0BUF) concurrently with the fall of the internal transfer clock of ③.
The LSI requests a UART0 interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UART0 status register (UA0STAT) to “1”.

Parity error : S0PER ＝“1”
Overrun error : S0OER ＝“1”
Framing error : S0FER ＝“1”

As shown in Figure 11-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
Reception continues until the U0EN bit is reset to “0” by the program. When the U0EN bit is reset to “0” during reception, the received data may be destroyed. When the U0EN bit is reset to “0” during the “U0EN reset enable period” in Figure 11-6, the received data is protected.

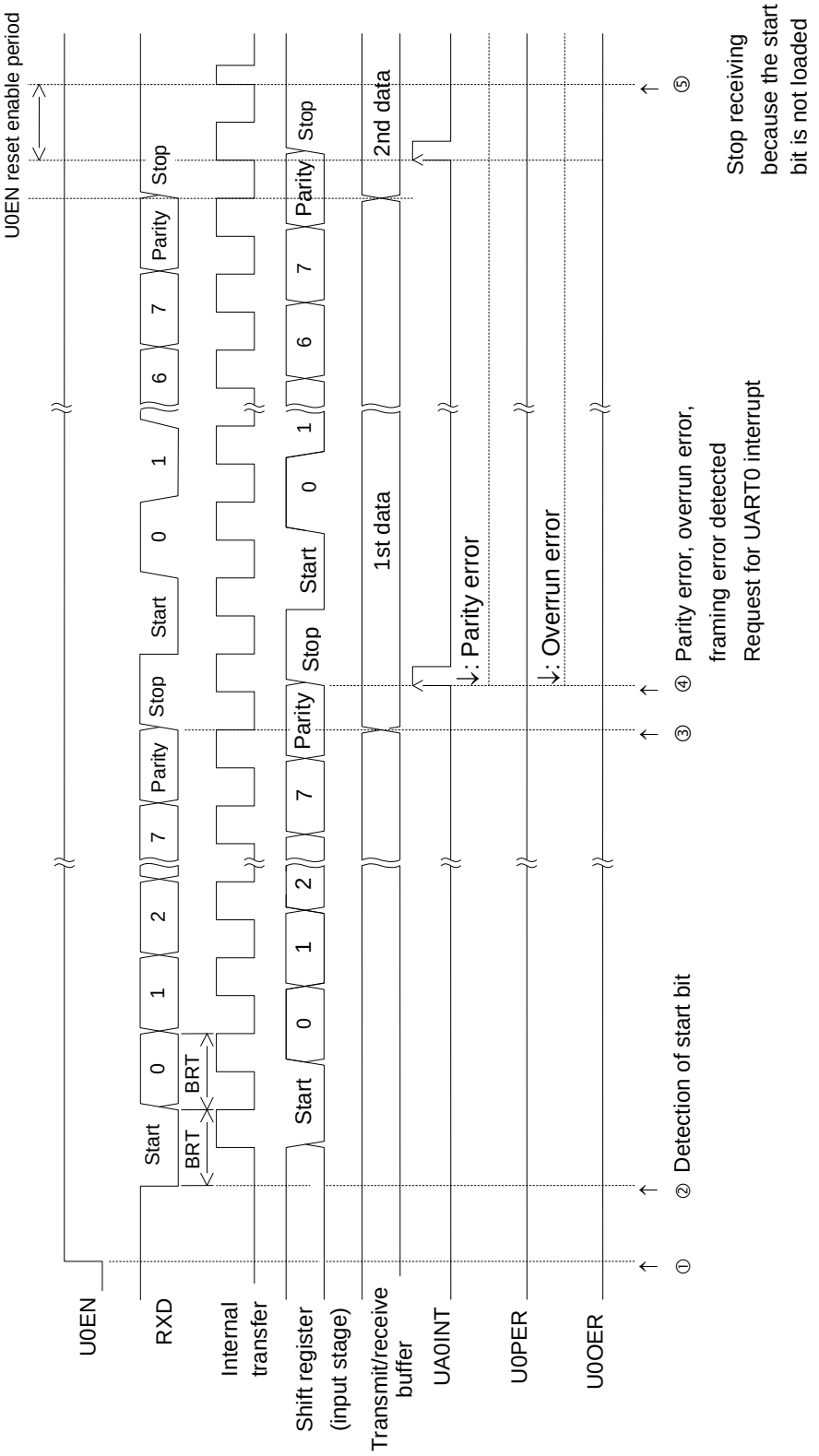


Figure 11-6 Operation Timing in Reception

11.3.5.1 Detection of Start Bit

The Start bit is sampled using the baud rate generator clock (LSCLK, HSCLK) selected by the U0CK1 and U0CK0 bits of the UARTn mode register 0 (UA0MOD0). Therefore, the start bit detection may be delayed for one cycle of the baud rate generate clock at the maximum.
Figure 11-7 shows the start bit detection timing.

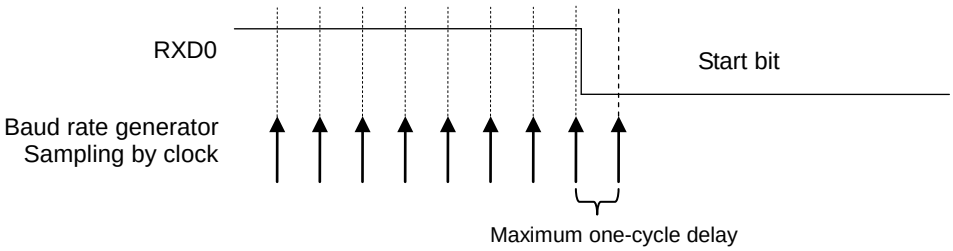


Figure 11-7 Start Bit Detection Timing (Positive Logic)

11.4 Specifying port registers

To enable the UART function, the applicable bit of each related port register needs to be set. See Chapter 13, “Port B” for detail about the port registers.

11.4.1 Functioning PB1(TXD0) and PB0(RXD0) as the UART

Set the PB1MD1 bit(bit1 of PBMOD1 register) to “0” and set the PB0MD1(bit0 of PBMOD1 register) to “1”, and set the PB1MD0-PB0MD0 bits(bit1-bit0 of PBMOD0 register) to “0”, for specifying the UART as the tertiary function of PB1 and the primary function of PB0.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	**PB1MD1**	**PB0MD1**
Setting value	*	*	*	*	*	*	**1**	**0**

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	**PB1MD0**	**PB0MD0**
Setting value	*	*	*	*	*	*	**0**	**0**

Set the PB1C1 bit (bit1 of PBCON1 register) to "1", the PB1C0 bit (bit1 of PBCON0 register) to "1", and the PB1DIR bit (bit1 of PBDIR register) to "0" for specifying the state mode of the PB1 pin to CMOS output.
Set the PB0DIR bit (bit0 of PBDIR register) to “1” for specifying the PB0 as an input pin.
The set value ($) is arbitrary for the PB0C1 and PB0C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB0 pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7C1	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	**PB1C1**	**PB0C1**
Setting value	*	*	*	*	*	*	**1**	**$**

Register name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	**PB1C0**	**PB0C0**
Setting value	*	*	*	*	*	*	**1**	**$**

Register name	PBDIR register (Address: 0F259H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7DIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	**PB1DIR**	**PB0DIR**
Setting value	*	*	*	*	*	*	**0**	**$**

The PB1D, PB0D bits (bit1-bit0 of PBD register) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	**PB1D**	**PB0D**
Setting value	*	*	*	*	*	*	**	**

* : Bit not related to the UART function
** : Don't care $: Optional

[Note:]
The receive pin (RXD) is selected by U0RSEL bit (bit4 of UA0MOD0 register). The initial value "0" selects the PB0 and the value "1" selects the PB5.

11.4.2 Functioning PB4(TXD0) and PB5(RXD0) as the UART

Set the PB5MD1 bit (bit5 of PBMOD1 register) to “0” and set the PB4MD1(bit4 of PBMOD1 register) to “1”, and set the PB5MD0-PB4MD0 bits(bit5-bit4 of PBMOD0 register) to “0”, for specifying the UART as the primary function of PB5 and the tertiary function of PB4.

Register name	PBMOD1 register (Address: 0F25DH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7MD1	PB6MD1	**PB5MD1**	**PB4MD1**	PB3MD1	PB2MD1	PB1MD1	PB0MD1
Setting value	*	*	**0**	**0**	*	*	*	*

Register name	PBMOD0 register (Address: 0F25CH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7MD0	PB6MD0	**PB5MD0**	**PB4MD0**	PB3MD0	PB2MD0	PB1MD0	PB0MD0
Setting value	*	*	**0**	**1**	*	*	*	*

Set the PB4C1 bit (bit4 of PBCON1 register) to "1", the PB4C0 bit (bit4 of PBCON0 register) to "1", and the PB4DIR bit (bit4 of PBDIR register) to "0" for specifying the state mode of the PB4 pin to CMOS output.
Set the PB5DIR bit (bit5 of PBDIR register) to “1” for specifying the PB5 as an input pin.
The set value ($) is arbitrary for the PB5C1 and PB5C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the PB0 pin is connected.

Register name	PBCON1 register (Address: 0F25BH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7C1	PB6C1	**PB5C1**	**PB4C1**	PB3C1	PB2C1	PB1C1	PB0C1
Setting value	*	*	**$**	**1**	*	*	*	*

Register name	PBCON0 register (Address: 0F25AH)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7C0	PB6C0	**PB5C0**	**PB4C0**	PB3C0	PB2C0	PB1C0	PB0C0
Setting value	*	*	**$**	**1**	*	*	*	*

Register name	PBDIR register (Address: 0F259H)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7DIR	PB6DIR	**PB5DIR**	**PB4DIR**	PB3DIR	PB2DIR	PB1DIR	PB0DIR
Setting value	*	*	**1**	**0**	*	*	*	*

The PB3D bit (PBD register bit 3) data can either be "0" or "1" (not need to be set).

Register name	PBD register (Address: 0F258H)							
Bit	7	6	**5**	**4**	3	2	1	0
Bit name	PB7D	PB6D	**PB5D**	**PB4D**	PB3D	PB2D	PB1D	PB0D
Setting value	*	*	****	****	*	*	*	*

* : Bit not related to the UART function
** : Don’t care $: Optional

Note:
•The receive pin (RXD) is selected by U0RSEL bit (bit4 of UA0MOD0 register). The initial value "0" selects the PB0 and the value "1" selects the PB5.
•Even if the PB5 pin is selected as RXD0 by the PB5MD1, PB5MD0, PB5C1, PB5C0, and PB5IDR bits, the PB0 pin will be selected as RXD0 when the U0RSEL bit of the UA0MOD0 register is "0".

Chapter 12

Port A

12 Port A

12.1 Overview

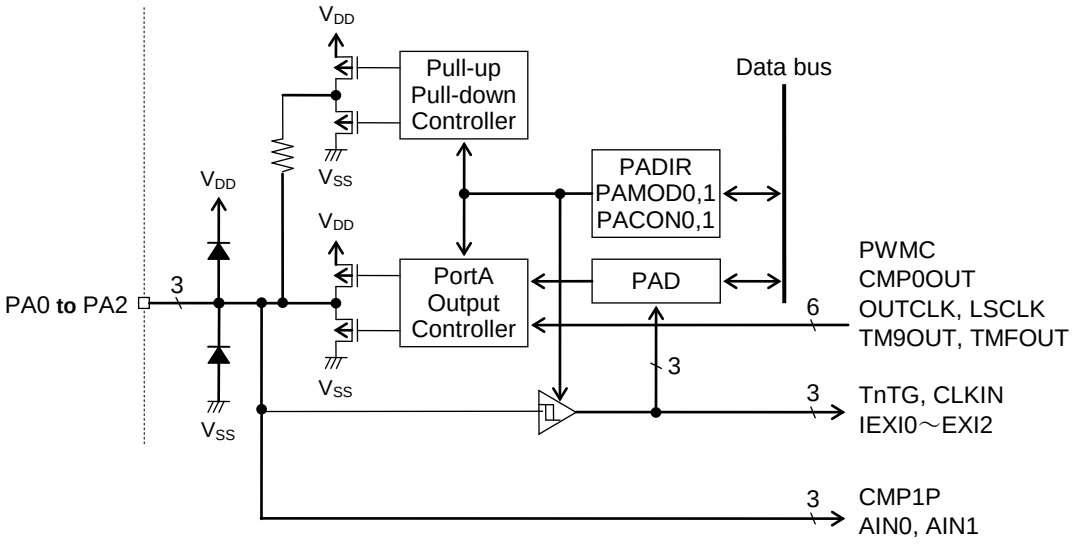
This LSI includes Port A (PA0 to PA2) which is an 3-bit input/output port.
Port A can have external interrupt, input of comparator and input of Successive Approximation Type A/D Converter. And, port A can have PWM, UART, Timers, output of comparator, input of external clock, output of clock functions as secondary function tertiary and fourthly functions.
For the PWM, see Chapter 10, "PWM", for the comparator, see Chapter 17, "Analog Comparator "; for the Successive Approximation Type A/D Converter, see Chapter 15, "Successive Approximation Type A/D Converter", for the external clock and output of clock, see Chapter 6, "Clock Generation Circuit", For the Timers, see Chapter 8, "Timers".

12.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The external interrupt pins (EXI0 to EXI2), comparator input pin (CMP1P), and analog input pin of Successive Approximation Type A/D Converter (AIN0, AIN1) can be used.
  The PWM pin (PWMC), comparator output pins (CMP0OUT), Timers output pin (TM9OUT,TMFOUT), external clock pin (CLKIN), clock output pin can be used as secondary, tertiary and fourthly functions.

12.1.2 Configuration

Figure 12-1 shows the configuration of Port A.



PAD	: Port A data register
PADIR	: Port A direction register
PACON0	: Port A control register 0
PACON1	: Port A control register 1
PAMOD0	: Port A mode register 0
PAMOD1	: Port A mode register 1

Figure 12-1 Configuration of Port A

Note:
PA0 – PA1 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.
PA1 is assigned to the input of Analog Comparator. When used as an analog input of Analog Comparator, set an applicable port as a high impedance output state.

12.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Fourthly function
PA0/ EXI0/ AIN0	I/O	Input/output port, External 0 interrupt, SA-ADC 0 input	PWMC output (PWMC)	High-speed clock output (OUTCLK)	Timer 9 out (TM9OUT)
PA1/ EXI1/ AIN1/ CMP1P	I/O	Input/output port, External 1 interrupt, SA-ADC 1 input Analog comparator 1 inverted input	—	Low-speed clock output (LSCLK)	Timer F out (TMFOUT)
PA2/ EXI2	I/O	Input/output port, External 2 interrupt	—	External clock input (CLKIN)	Comparator 0 output (CMP0OUT)

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F250H	Port A data register	PAD	—	R/W	8	00H
0F251H	Port A direction register	PADIR	—	R/W	8	00H
0F252H	Port A control register 0	PACON0	PACON	R/W	8/16	00H
0F253H	Port A control register 1	PACON1		R/W	8	00H
0F254H	Port A mode register 0	PAMOD0	PAMOD	R/W	8/16	00H
0F255H	Port A mode register 1	PAMOD1		R/W	8	00H

12.2.2 Port A Data Register (PAD)

Address: 0F250H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PAD	—	—	—	—	—	PA2D	PA1D	PA0D
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PAD is a special function register (SFR) to set the value to be output to the Port A pin or to read the input level of the Port A. In output mode, the value of this register is output to the Port A pin. The value written to PAD is readable. In input mode, the input level of the Port A pin is read when PAD is read. Output mode or input mode is selected by using the port direction register (PADIR) described later.

[Description of Bits]

- **PA2D-PA0D** (bits 2-0)
  The PA2D to PA0D bits are used to set the output value of the Port A pin in output mode and to read the pin level of the Port A pin in input mode.

PA2D	Description
0	Output or input level of the PA2 pin: "L"
1	Output or input level of the PA2 pin: "H"

PA1D	Description
0	Output or input level of the PA1 pin: "L"
1	Output or input level of the PA1 pin: "H"

PA0D	Description
0	Output or input level of the PA0 pin: "L"
1	Output or input level of the PA0 pin: "H"

12.2.3 Port A Direction Register (PADIR)

Address: 0F251H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PADIR	—	—	—	—	—	PA2DIR	PA1DIR	PA0DIR
R/W	R	R	R/	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PADIR is a special function register (SFR) to select the input/output mode of Port A.

[Description of Bits]

- **PA2DIR-PA0DIR** (bits 2-0)
  The PA2DIR to PA0DIR pins are used to set the input/output direction of the Port A pin.

PA2DIR	Description
0	PA2 pin: Output (initial value)
1	PA2 pin: Input

PA1DIR	Description
0	PA1 pin: Output (initial value)
1	PA1 pin: Input

PA0DIR	Description
0	PA0 pin: Output (initial value)
1	PA0 pin: Input

12.2.4 Port A Control Registers 0, 1 (PACON0, PACON1)

Address: 0F252H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PACON0	—	—	—	—	—	PA2C0	PA1C0	PA0C0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F253H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PACON1	—	—	—	—	—	PA2C1	PA1C1	PA0C1
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PACON0 and PACON1 are special function registers (SFRs) to select input/output state of the Port A pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PADIR register.

[Description of Bits]

- **PA2C1-PA0C1, PA2C0-PA0C0** (bits 2-0)
  The PA2C1 to PA0C1 pins and the PA2C0 to PA0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of PA2 pin		When output mode is selected (PA2DIR bit = "0")	When input mode is selected (PA2DIR bit = "1")
PA2C1	**PA2C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA1 pin		When output mode is selected (PA1DIR bit = "0")	When input mode is selected (PA1DIR bit = "1")
PA1C1	**PA1C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PA0 pin		When output mode is selected (PA0DIR bit = "0")	When input mode is selected (PA0DIR bit = "1")
PA0C1	**PA0C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

12.2.5 Port A Mode Registers 0 (PAMOD0, PAMOD1)

Address: 0F254H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PAMOD0	—	—	—	—	—	PA2MD0	PA1MD0	PA0MD0
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F255H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PAMOD1	—	—	—	—	—	PA2MD1	PA1MD1	PA0MD1
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PAMOD0 and PAMOD1 are special function register (SFR) to select the primary, secondary, tertiary and fourthly function of Port A.

[Description of Bits]

- **PA2MD1, PA2MD0** (bit 2)
  The PA2MD1 and PA2MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PA2 pin.

PA2MD1	PA2MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	External clock (CLKIN) input
1	1	Comparator 0 (CMP0OUT) output

- **PA1MD1, PA1MD0** (bit 1)
  The PA1MD1 and PA1MD0 bits are used to select the primary, secondary tertiary and fourthly functions of the PA1 pin.

PA1MD1	PA1MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Low-speed clock (LSCLK) output
1	1	Timer F (TMFOUT) out

- **PA0MD1, PA0MD0** (bit 0)
  The PA0MD1 and PA0MD0 bits are used to select the primary, secondary tertiary and fourthly functions of the PA0 pin.

PA0MD1	PA0MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWMC output
1	0	High-speed clock (OUTCLK) output
1	1	Timer 9 (TM9OUT) out

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the port A is specified to output mode (selected in portA control register), status of corresponding pin is fixed, regardless the contents of PortA register (PAD)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

12.3 Description of Operation

12.3.1 Input/Output Port Functions

For each pin of Port A, either output or input is selected by setting the Port A direction register (PADIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port A control registers 0 and 1 (PACON0 and PACON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port A control registers 0 and 1 (PACON0 and PACON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port A depending on the value set by the Port A data register (PAD).
In input mode, the input level of each pin of Port A can be read from the Port A data register (PAD).

12.3.2 Secondary tertiary and fourthly functions

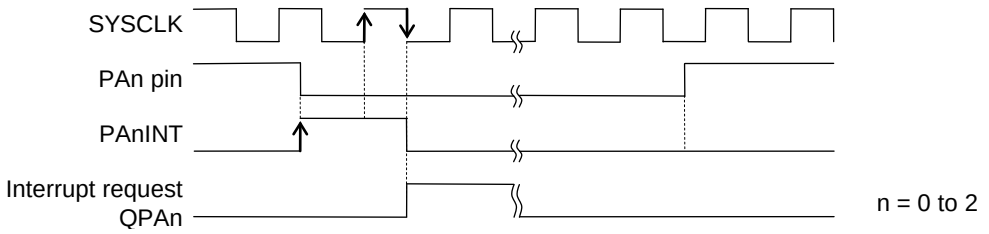
Port A is assigned to the PWM pin (PWMC), comparator output pins (CMP0OUT), Timers output pin (TM9OUT, TMFOUT), external clock pin (CLKIN), clock output pin as its secondary, tertiary and fourthly functions. These pins can be used in secondary, tertiary and fourthly functions mode by setting the PA2MD0 to PA0MD0 bits and the PA2MD1 to PA0MD1 bits of the Port A mode registers (PAMOD0, PAMOD1).

12.3.3 External Interrupt

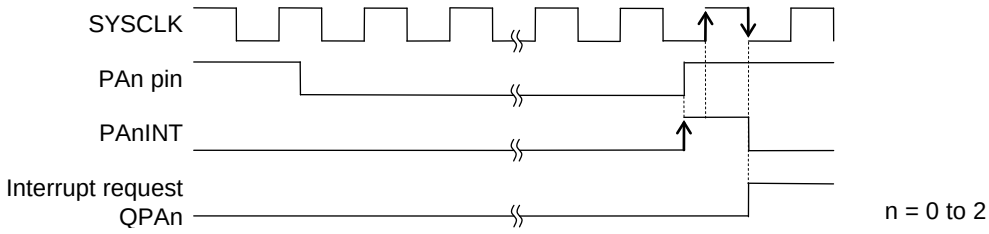
The Port A pins (PA0 to PA2) can be used for PA0 to PA2 interrupts (PA0INT to PA2INT). The PA0 to PA2 interrupts are maskable and interrupt enable or disable can be selected. For details of interrupts, see Chapter 5, "Interrupts".

12.3.4 Interrupt Request

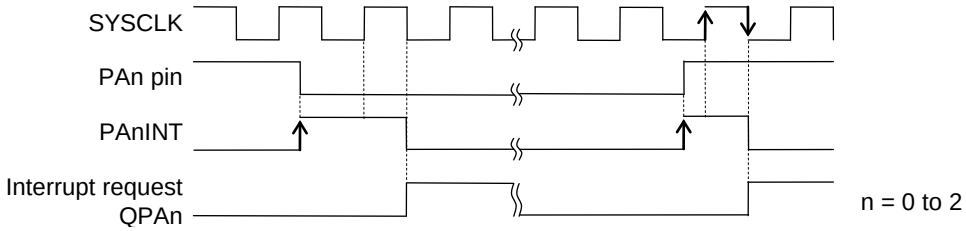
When an interrupt edge selected by the port AB interrupt control registers 0, 1, 2 (PABICON0, PABICON1, PABICON2) occurs at a Port A pin, the corresponding maskable Pxx (PA0 to PA2) interrupt (PA0INT–PA2INT) occurs.
For details of port AB interrupts, see Chapter 14, "Port AB Interrupts".
Figure 12-2 shows the PA0–PA2 interrupt generation timing in rising-edge interrupt mode, falling-edge interrupt mode, and both-edges interrupt mode, each without sampling, and the PA0 to PA2 interrupt generation timing in rising-edge interrupt mode with sampling.



(a) When "falling-edge interrupt; without sampling" is selected

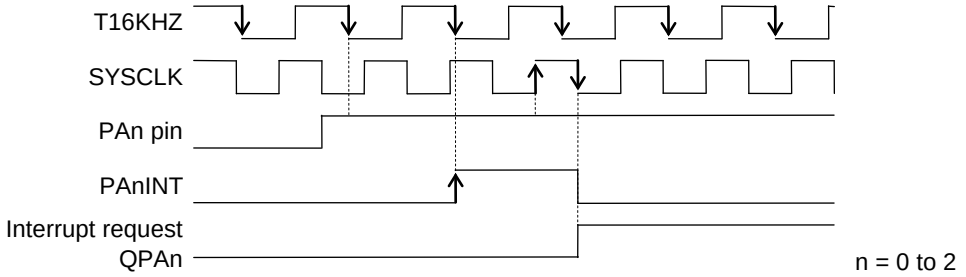


(b) When "rising-edge interrupt; without sampling" is selected



(c) When "both-edges interrupt; without sampling" is selected

When "rising-edge interrupt; with sampling" is selected, The input level of PAn pins are checked by a T16kHz negative going edge. An interrupt condition will be satisfied if an input level is "H" consecutive two times.
An interrupt request occurs to the timing of the SYSCLK negative going edge after the 2nd T16kHz negative going edge.



(d) When "rising-edge interrupt; with sampling" is selected

Figure 13-2 PA0 to PA2 Interrupt Generation Timing

Chapter 13

Port B

13 Port B

13.1 Overview

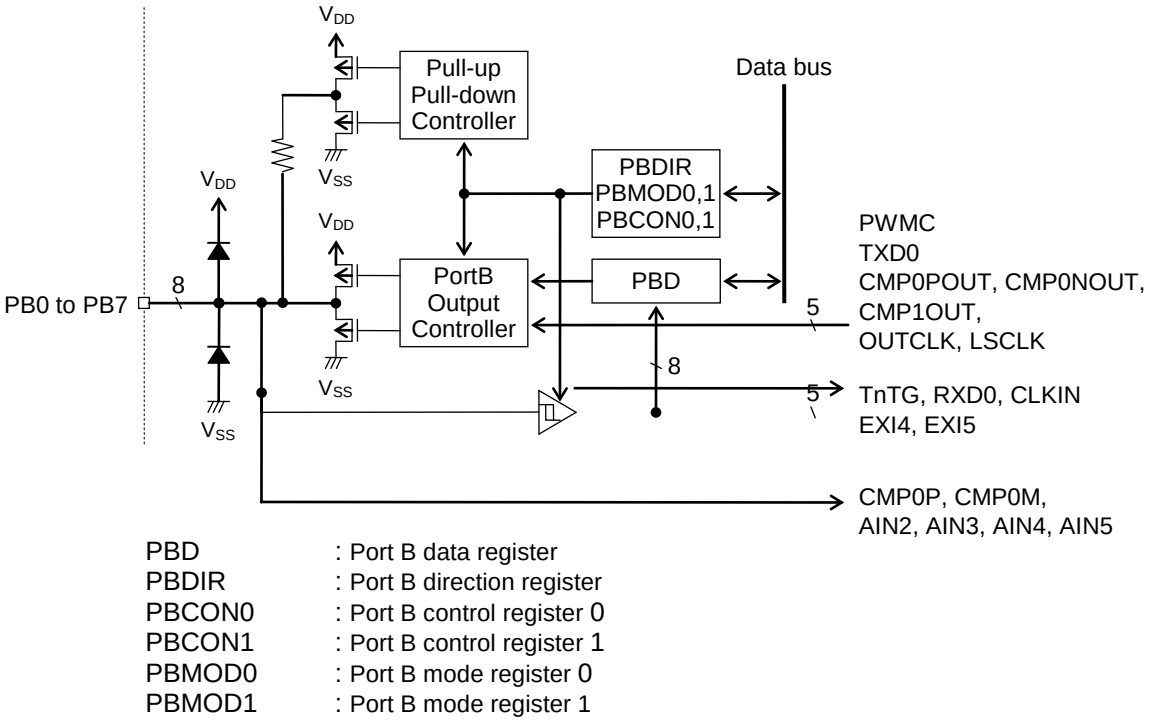
This LSI includes Port B (PB0 to PB7) which is an 8-bit input/output port.
Port B can have external interrupt, input of comparator and input of Successive Approximation Type A/D Converter.
And, port B can have PWM, output of comparator, UART, input of external clock, output of clock functions as secondary function tertiary and fourthly functions.
For the PWM, see Chapter 10, "PWM", for the comparator, see Chapter 17, "Analog Comparator "; for the Successive Approximation Type A/D Converter, see Chapter 15, "Successive Approximation Type A/D Converter" , for the UART, see Chapter 11, "UART", for the external clock and output of clock, see Chapter 6, "Clock Generation Circuit".

13.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The external interrupt pins (EXI4, EXI5), comparator input pin (CMP0P,CMP0M), analog input pin of Successive Approximation Type A/D Converter (AIN2～5), and UART input pin (RXD0) can be used.
  The PWM pin (PWMC), comparator input pins (CMP0P,CMP0M), UART output pin (TXD0), external clock pin (CLKIN), clock output pin (OUTCLK, LSCLK) can be used as the secondary, tertiary and fourthly functions.

13.1.2 Configuration

Figure 13-1 shows the configuration of Port B.



PBD : Port B data register
PBDIR : Port B direction register
PBCON0 : Port B control register 0
PBCON1 : Port B control register 1
PBMOD0 : Port B mode register 0
PBMOD1 : Port B mode register 1

Figure 13-1 Configuration of Port B

Note:
PB0, PB1, PB6, PB7 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.
PB4, PB5 are assigned to the input of Analog Comparator. When used as an analog input of Analog Comparator, set an applicable port as a high impedance output state.

13.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function		
PB0/ EXI4/ AIN2/ RXD0	I/O	Input/output port External 4 interrupt, SA-ADC 2 input, UART0 data input	PWMC output (PWMC)	High-speed clock output (OUTCLK)	Comparator 1 output (CMP1OUT)
PB1/ EXI5/ AIN3	I/O	Input/output port External 5 interrupt, SA-ADC 3 input	—	UART0 data output	—
PB2	I/O	Input/output port	—	—	Comparator 0 output (CMP0POUT)
PB3	I/O	Input/output port	—	—	Comparator 0 output (CMP0NOUT)
PB4/ CMP0P	I/O	Input/output port, Analog comparator 0 non-inverted input	—	UART0 data output	—
PB5/ RXD0/ CMP0M	I/O	Input/output port, UART0 data input, Analog comparator 0 inverted input pin	—	—	—
PB6/ AIN4	I/O	Input/output port	External clock input (CLKIN)	—	—
PB7/ AIN5	I/O	Input/output port	Low-speed clock output (LSCLK)	—	PWMC output (PWMC)

13.2 Description of Registers

13.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F258H	Port B data register	PBD	—	R/W	8	00H
0F259H	Port B direction register	PBDIR	—	R/W	8	00H
0F25AH	Port B control register 0	PBCON0	PBCON	R/W	8/16	00H
0F25BH	Port B control register 1	PBCON1		R/W	8	00H
0F25CH	Port B mode register 0	PBMOD0	PBMOD	R/W	8/16	00H
0F25DH	Port B mode register 1	PBMOD1		R/W	8	00H

13.2.2 Port B Data Register (PBD)

Address: 0F258H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBD	PB7D	PB6D	PB5D	PB4D	PB3D	PB2D	PB1D	PB0D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBD is a special function register (SFR) to set the value to be output to the Port B pin or to read the input level of the Port B. In output mode, the value of this register is output to the Port B pin. The value written to PBD is readable. In input mode, the input level of the Port B pin is read when PBD is read. Output mode or input mode is selected by using the port direction register (PBDIR) described later.

[Description of Bits]

- **PB7D-PB0D** (bits 7-0)
  The PB7D to PB0D bits are used to set the output value of the Port B pin in output mode and to read the pin level of the Port B pin in input mode.

PB7D	Description
0	Output or input level of the PB7 pin: "L"
1	Output or input level of the PB7 pin: "H"

PB6D	Description
0	Output or input level of the PB6 pin: "L"
1	Output or input level of the PB6 pin: "H"

PB5D	Description
0	Output or input level of the PB5 pin: "L"
1	Output or input level of the PB5 pin: "H"

PB4D	Description
0	Output or input level of the PB4 pin: "L"
1	Output or input level of the PB4 pin: "H"

PB3D	Description
0	Output or input level of the PB3 pin: "L"
1	Output or input level of the PB3 pin: "H"

PB2D	Description
0	Output or input level of the PB2 pin: "L"
1	Output or input level of the PB2 pin: "H"

PB1D	Description
0	Output or input level of the PB1 pin: "L"
1	Output or input level of the PB1 pin: "H"

PB0D	Description
0	Output or input level of the PB0 pin: "L"
1	Output or input level of the PB0 pin: "H"

13.2.3 Port B Direction Register (PBDIR)

Address: 0F259H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBDIR	PB7DIR	PB6DIR	PB5DIR	PB4DIR	PB3DIR	PB2DIR	PB1DIR	PB0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBDIR is a special function register (SFR) to select the input/output mode of Port B.

[Description of Bits]

- **PB7DIR-PB0DIR** (bits 7-0)
  The PB7DIR to PB0DIR pins are used to set the input/output direction of the Port B pin.

PB7DIR	Description
0	PB7 pin: Output (initial value)
1	PB7 pin: Input

PB6DIR	Description
0	PB6 pin: Output (initial value)
1	PB6 pin: Input

PB5DIR	Description
0	PB5 pin: Output (initial value)
1	PB5 pin: Input

PB4DIR	Description
0	PB4 pin: Output (initial value)
1	PB4 pin: Input

PB3DIR	Description
0	PB3 pin: Output (initial value)
1	PB3 pin: Input

PB2DIR	Description
0	PB2 pin: Output (initial value)
1	PB2 pin: Input

PB1DIR	Description
0	PB1 pin: Output (initial value)
1	PB1 pin: Input

PB0DIR	Description
0	PB0 pin: Output (initial value)
1	PB0 pin: Input

13.2.4 Port B Control Registers 0, 1 (PBCON0, PBCON1)

Address: 0F25AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBCON0	PB7C0	PB6C0	PB5C0	PB4C0	PB3C0	PB2C0	PB1C0	PB0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F25BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBCON1	PB7C1	PB6C1	PB5C1	PB4C1	PB3C1	PB2C1	PB1C1	PB0C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBCON0 and PBCON1 are special function registers (SFRs) to select input/output state of the Port B pin. The input/output state is different between input mode and output mode. Input or output is selected by using the PBDIR register.

[Description of Bits]

- **PB7C1-PB0C1, PB7C0-PB0C0** (bits 7-0)
  The PB7C1 to PB0C1 pins and the PB7C0 to PB0C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of PB7 pin		When output mode is selected (PB7DIR bit = "0")	When input mode is selected (PB7DIR bit = "1")
PB7C1	**PB7C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB6 pin		When output mode is selected (PB6DIR bit = "0")	When input mode is selected (PB6DIR bit = "1")
PB6C1	**PB6C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB5 pin		When output mode is selected (PB5DIR bit = "0")	When input mode is selected (PB5DIR bit = "1")
PB5C1	**PB5C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB4 pin		When output mode is selected (PB4DIR bit = "0")	When input mode is selected (PB4DIR bit = "1")
PB4C1	**PB4C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB3 pin		When output mode is selected (PB3DIR bit = "0")	When input mode is selected (PB3DIR bit = "1")
PB3C1	**PB3C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB2 pin		When output mode is selected (PB2DIR bit = "0")	When input mode is selected (PB2DIR bit = "1")
PB2C1	**PB2C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB1 pin		When output mode is selected (PB1DIR bit = "0")	When input mode is selected (PB1DIR bit = "1")
PB1C1	**PB1C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of PB0 pin		When output mode is selected (PB0DIR bit = "0")	When input mode is selected (PB0DIR bit = "1")
PB0C1	**PB0C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

13.2.5 Port B Mode Registers 0 (PBMOD0, PBMOD1)

Address: 0F25CH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBMOD0	PB7MD0	PB6MD0	PB5MD0	PB4MD0	PB3MD0	PB2MD0	PB1MD0	PB0MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F25DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PBMOD1	PB7MD1	PB6MD1	PB5MD1	PB4MD1	PB3MD1	PB2MD1	PB1MD1	PB0MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PBMOD0 and PBMOD1 are special function register (SFR) to select the primary, secondary, tertiary and fourthly function of Port B.

[Description of Bits]

- **PB7MD1, PB7MD0** (bit 7)
  The PB7MD1 and PB7MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB7 pin.

PB7MD1	PB7MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Low-speed clock (LSCLK) output
1	0	Prohibited
1	1	PWMC output

- **PB6MD0, PB6MD0** (bit 6)
  The PB6MD1 and PB6MD0 bits are used to select the primary, secondary tertiary and fourthly functions of the PB6 pin.

PB6MD1	PB6MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	External clock (CLKIN) input
1	0	Prohibited
1	1	Prohibited

- **PB5MD1, PB5MD0** (bit 5)
  The PB5MD1 and PB5MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB5 pin.

PB5MD1	PB5MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

- **PB4MD1, PB4MD0** (bit 4)
  The PB4MD1 and PB4MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB4 pin.

PB4MD1	PB4MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	UART0 data output pin
1	1	Prohibited

- **PB3MD1, PB3MD0** (bit 3)

The PB3MD1 and PB3MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB3 pin.

PB3MD1	PB3MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Comparator 0 (CMP0NOUT) output

- **PB2MD1, PB2MD0** (bit 2)
  The PB2MD1 and PB2MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB2 pin.

PB2MD1	PB2MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Comparator 0 (CMP0POUT) output

- **PB1MD1, PB1MD0** (bit 1)
  The PB1MD1 and PB1MD0 bits are used to select the primary, secondary, tertiary and fourthly functions of the PB1 pin.

PB2MD1	PB1MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	UART0 data output pin
1	1	Prohibited

- **PB0MD1, PB0MD0** (bit 0)
  The PB0MD1 and PB0MD0 bits are used to select the primary, secondary, tertiary and fourthly function of the PB0 pin.

PB0MD1	PB0MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	PWMC output
1	0	High-speed clock (OUTCLK) output
1	1	Comparator 1 (CMP1OUT) output

Note:
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the port B is specified to output mode (selected in portB control register), status of corresponding pin is fixed, regardless the contents of PortB register (PBD)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

13.3 Description of Operation

13.3.1 Input/Output Port Functions

For each pin of Port B, either output or input is selected by setting the Port B direction register (PBDIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port B control registers 0 and 1 (PBCON0 and PBCON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port B control registers 0 and 1 (PBCON0 and PBCON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port B depending on the value set by the Port B data register (PBD).
In input mode, the input level of each pin of Port B can be read from the Port B data register (PBD).

13.3.2 Secondary tertiary and fourthly functions

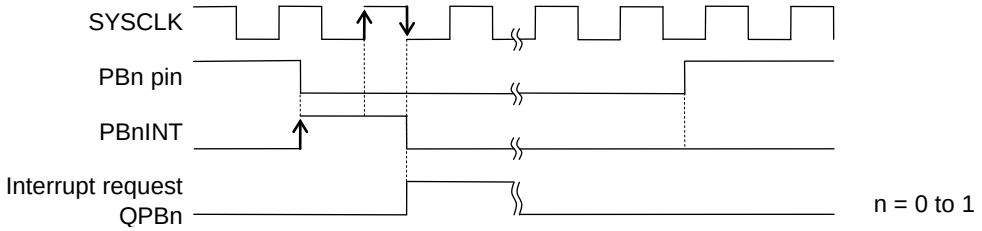
Port B is assigned to PWM pin (PWMC), comparator output pins (CMP0POUT,CMP0NOUT,CMP1OUT), UART output pin (TXD0), external clock pin (CLKIN), clock output pin (OUTCLK, LSCLK) as its secondary, tertiary and fourthly functions. These pins can be used in secondary, tertiary and fourthly functions mode by setting the PB7MD0 to PB0MD0 bits and the PB7MD1 to PB0MD1 bits of the Port B mode registers (PBMOD0, PBMOD1).

13.3.3 External Interrupt

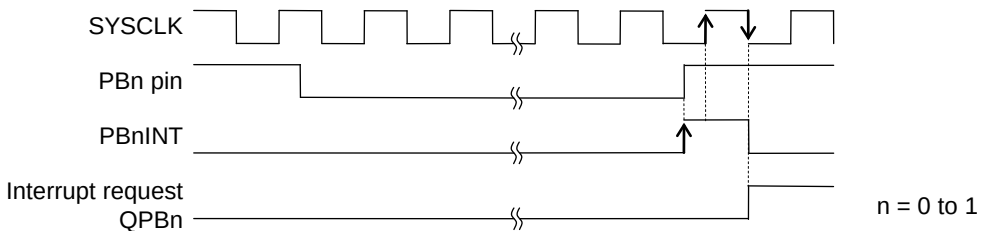
The Port B pins (PB0, PB1) can be used for PB0 to PB1 interrupts (PB0INT to PB1INT). The PB0 to PB1 interrupts are maskable and interrupt enable or disable can be selected. For details of interrupts, see Chapter 5, "Interrupts".

13.3.4 Interrupt Request

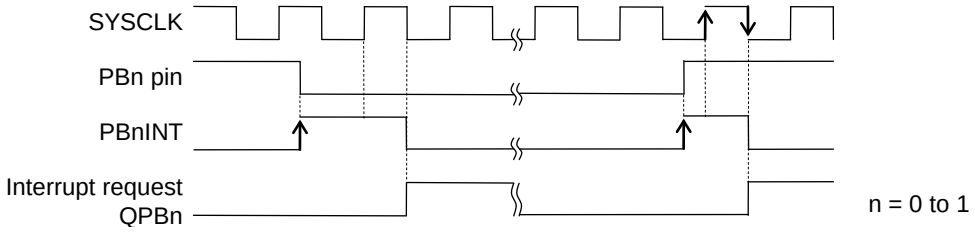
When an interrupt edge selected by the port AB interrupt control registers 0, 1, 2 (PABICON0, PABICON1, PABICON2) occurs at a Port B pin, the corresponding maskable Pxx (PB0 to PB1) interrupt (PB0INT–PB1INT) occurs.
For details of port AB interrupts, see Chapter 14, "Port AB Interrupts".
Figure 13-2 shows the PB0, PB1 interrupt generation timing in rising-edge interrupt mode, falling-edge interrupt mode, and both-edges interrupt mode, each without sampling, and the PB0 to PB1 interrupt generation timing in rising-edge interrupt mode with sampling.



(a) When "falling-edge interrupt; without sampling" is selected

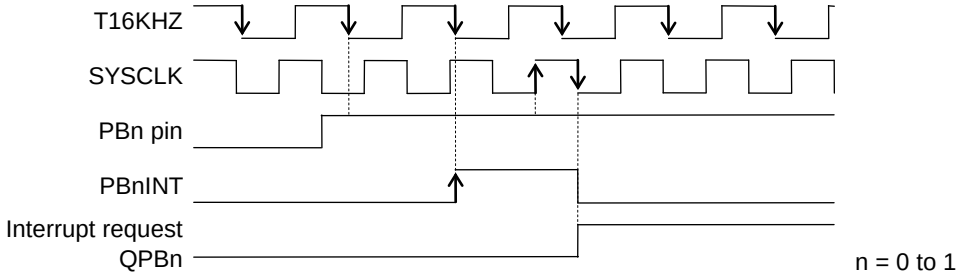


(b) When "rising-edge interrupt; without sampling" is selected



(c) When "both-edges interrupt; without sampling" is selected

When "rising-edge interrupt; with sampling" is selected, The input level of PBn pins are checked by a T16kHz negative going edge. An interrupt condition will be satisfied if an input level is "H" consecutive two times.
An interrupt request occurs to the timing of the SYSCLK negative going edge after the 2nd T16kHz negative going edge.



(d) When "rising-edge interrupt; with sampling" is selected

Figure 13-2 PB0, PB1 Interrupt Generation Timing

Chapter 14

Port AB Interrupts

14 Port AB Interrupts

14.1 Overview

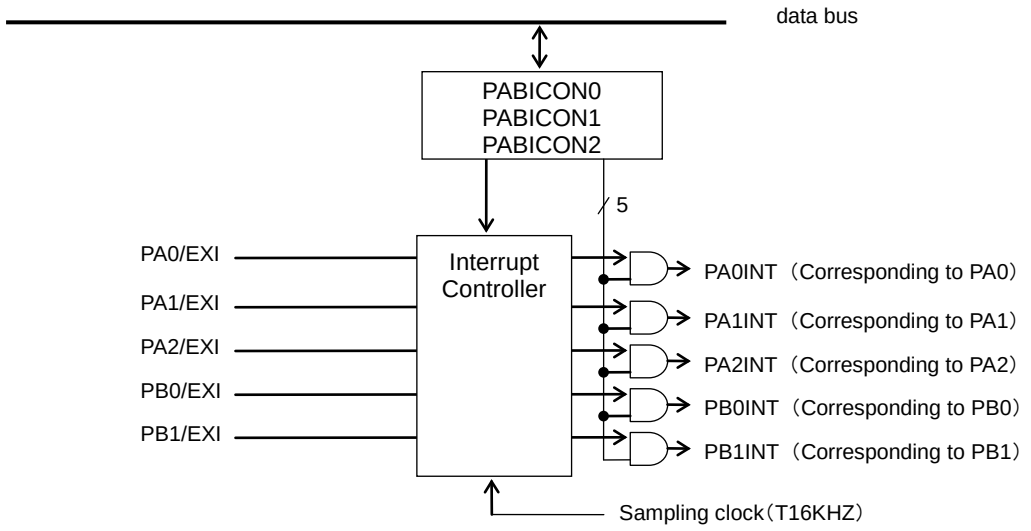
This LSI can have the external Interrupts corresponding to five ports.

14.1.1 Features

- All bits support a maskable interrupt function.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for each bit.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ)

14.1.2 Configuration

Figure 14-1 shows the configuration of Port AB Interrupts Control.



PABICON0 : Port AB interrupt control register 0
PABICON1 : Port AB interrupt control register 1
PABICON2 : Port AB interrupt control register 2

Figure 14-1 Configuration of Port AB Interrupts Control

14.2 Description of Registers

14.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F024H	Port AB interrupt control register 0	PABICON0	—	R/W	8	00H
0F025H	Port AB interrupt control register 1	PABICON1	—	R/W	8	00H
0F026H	Port AB interrupt control register 2	PABICON2	—	R/W	8	00H

14.2.2 Port AB Interrupt Control Registers 0, 1 (PABICON0, PABICON1)

Address: 0F024H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PABICON0	—	—	PB1E0	PB0E0	—	PA2E0	PA1E0	PA0E0
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F025H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PABICON1	—	—	PB1E1	PB0E1	—	PA2E1	PA1E1	PA0E1
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PABICON0 and PABICON1 are special function registers (SFRs) to select an interrupt edge of Port A and Port B.

[Description of Bits]

- **PB1E0-PA0E0, PB1E1-PA0E1** (bits 5 to 0)
  The PB1E0 to PA0E0 bits and the PB1E1 to PA0E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The PnE0 bit and the PnE1 bit determine the interrupt mode of Pn (Example: When PA0E0 = "0" and PA0E1 = "1", PA0 is in rising-edge interrupt mode).

PB1E1-PA0E1	PB1E0-PA0E0	Description
0	0	Interrupt disabled mode (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

14.2.3 Port AB Interrupt Control Register 2 (PABICON2)

Address: 0F026H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PABICON2	—	—	PB1SM	PB0SM	—	PA2SM	PA1SM	PA0SM
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PABICON2 is a special function register (SFR) to select detection of signal edge for interrupts with or without sampling.

[Description of Bits]

- **PB1SM-PA0SM** (bits 5 to 0)
  The PB1SM to PA0SM bits are used to select detection of signal edge for Port A and Port B interrupts with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

PB1SM	Description
0	Detects the input signal edge for a PB1 interrupt without sampling (initial value).
1	Detects the input signal edge for a PB1 interrupt with sampling.

PB0SM	Description
0	Detects the input signal edge for a PB0 interrupt without sampling (initial value).
1	Detects the input signal edge for a PB0 interrupt with sampling.

PA2SM	Description
0	Detects the input signal edge for a PA2 interrupt without sampling (initial value).
1	Detects the input signal edge for a PA2 interrupt with sampling.

PA1SM	Description
0	Detects the input signal edge for a PA1 interrupt without sampling (initial value).
1	Detects the input signal edge for a PA1 interrupt with sampling.

PA0SM	Description
0	Detects the input signal edge for a PA0 interrupt without sampling (initial value).
1	Detects the input signal edge for a PA0 interrupt with sampling.

Note:
In STOP mode, since the 16 kHz sampling clock stops, no sampling is performed regardless of the values set in PB1SM to PA0SM.

Chapter 15

Successive Approximation Type A/D Converter

15 Successive Approximation Type A/D Converter

15.1 Overview

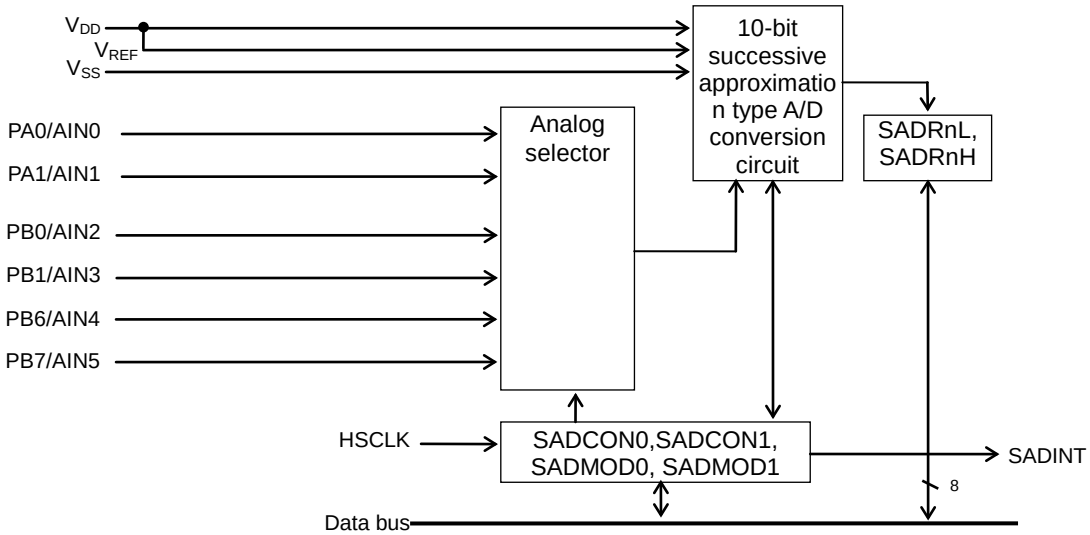
This LSI has a built-in 6-channel successive approximation type A/D converter (SA-ADC).

15.1.1 Features

- Built-in sample/hold 10-bit successive approximation type A-D converter, which enables channel selection from 6 channels

15.1.2 Configuration

Figure 15-1 shows the configuration of SA-ADC.



SADR0L :SA-ADC result register 0L
SADR0H :SA-ADC result register 0H
SADCON0 :SA-ADC control register 0
SADCON1 :SA-ADC control register 1
SADMOD0 :SA-ADC mode register 0

Figure 15-1 Configuration of SA-ADC

15.1.3 List of Pins

Pin name	I/O	Description
V_{DD}	—	Positive power supply pin for the successive approximation type A/D converter
V_{REF}	—	Reference power supply pin for the successive approximation type A/D converter
V_{SS}	—	Negative power supply pin for the successive approximation type A/D converter
PA0/AIN0	I	Successive approximation type A/D converter input pin 0
PA1/AIN1	I	Successive approximation type A/D converter input pin 1
PB0/AIN2	I	Successive approximation type A/D converter input pin 2
PB1/AIN3	I	Successive approximation type A/D converter input pin 3
PB6/AIN3	I	Successive approximation type A/D converter input pin 4
PB7/AIN3	I	Successive approximation type A/D converter input pin 5

Note:
PA0, PA1, PB0, PB1, PB6, PB7 are assigned to the input of SA-ADC.When used as an analog input of SA-ADC, set an applicable port as a high impedance output state.

15.2 Description of Registers

15.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2F1H	SA-ADC control register 1	SADCON1	—	R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	—	R/W	8	00H

15.2.2 SA-ADC Result Register 0L (SADR0L)

Address: 0F2D0H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0L	SAR03	SAR02	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0L is a special function register (SFR) used to store SA-ADC conversion results.
SADR0L is updated after A/D conversion.

[Description of Bits]

- **SAR03-SAR02** (bits 7-6)
  The SAR03–SAR02 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits).

15.2.3 SA-ADC Result Register 0H (SADR0H)

Address: 0F2D1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0H	SAR0B	SAR0A	SAR09	SAR08	SAR07	SAR06	SAR05	SAR04
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0H is a special function register (SFR) used to store SA-ADC conversion results.
SADR0H is updated after A/D conversion.

[Description of Bits]

- **SAR0B-SAR04** (bits 7-0)
  The SAR0B–SAR04 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits).

15.2.4 SA-ADC Control Register 1 (SADCON1)

Address: 0F2F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON1	—	—	—	—	—	—	—	SARUN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON1 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SARUN** (bit 0)

The SARUN bit is used to start or stop SA-ADC conversion. Setting this bit to "1" starts A/D conversion and setting it to "0" stops A/D conversion.

SARUN	Description
0	Stops conversion. (Initial value)
1	Starts conversion.

Note:
Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).
To set SACHn (from SACH0 to SACH5) to "1", set only 1 channel.
Do not start A/D conversion in the state in which bits 0 (SACH0) to bit 5 (SACH5) of SA-ADC mode register 0 are "0" and "0" respectively. When A/D conversion is started in this state, A/D conversion is not done while the A/D converter is activated. Therefore, the SA-ADC result register is not updated, the A/D conversion termination interrupt is not generated, A/D conversion is not terminated automatically, and SARUN remains "1".

15.2.5 SA-ADC Mode Register 0 (SADMOD0)

Address: 0F2F2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD0	—	—	SACH5	SACH4	SACH3	SACH2	SACH1	SACH0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to choose A/D conversion channel(s).

[Description of Bits]

- **SACH0** (bit 0)

SACH0	Description
0	Stops conversion on channel 0. (Initial value)
1	Performs conversion on channel 0.

- **SACH1** (bit 1)

SACH1	Description
0	Stops conversion on channel 1. (Initial value)
1	Performs conversion on channel 1.

- **SACH2** (bit 2)

SACH2	Description
0	Stops conversion on channel 2. (Initial value)
1	Performs conversion on channel 2.

- **SACH3** (bit 3)

SACH3	Description
0	Stops conversion on channel 3. (Initial value)
1	Performs conversion on channel 3.

- **SACH4** (bit 4)

SACH4	Description
0	Stops conversion on channel 4. (Initial value)
1	Performs conversion on channel 4.

- **SACH5** (bit 5)

SACH5	Description
0	Stops conversion on channel 5. (Initial value)
1	Performs conversion on channel 5.

The SACH0 to SACH5 bits are used to select channel on which A/D conversion is performed.
To set SACHn (from SACH0 to SACH5) to "1", set only 1 channel.
Do not start A/D conversion when all the SACHn (from SACH0 to SACH5) set to "0". If conversion is started, the A/D conversion circuit is activated (ON), however, A/D conversion is not done. Therefore, the SA-ADC result register is not updated, A/D conversion termination interrupt does not occur, A/D conversion does not terminate automatically, and consequently, bit 0 (SARUN) of the SA-ADC control register (SADCON1) remains "1".

15.3 Description of Operation

15.3.1 Settings of A/D Conversion Channels

According to the setting of SA-ADC mode register 0 (SADMOD0), A/D conversion is performed as shown below and A/D conversion results are stored in the SA-ADC result register (SADR0H/L).

SA-ADC mode register 0		SA-ADC result register	SA-ADC analog input
SACHn	0/1		
SACH0	0	SADR0	
SACH0	1	SADR0	AIN0 input
SACH1	0	SADR0	
SACH1	1	SADR0	AIN1 input
SACH2	0	SADR0	
SACH2	1	SADR0	AIN2 input
SACH3	0	SADR0	
SACH3	1	SADR0	AIN3 input
SACH4	0	SADR0	
SACH4	1	SADR0	AIN4 input
SACH5	0	SADR0	
SACH5	1	SADR0	AIN5 input

The values of the result register for the sections with a slash mark remain unchanged.
To set SACHn (from SACH0 to SACH5) to "1", set only 1 channel.
Do not start A/D conversion when bit 0 (SACH0) to bit 5 (SACH5) of SA-ADC mode register 0 (SADMOD0) is "0". If A/D conversion is started, the A/D conversion circuit is set to ON. However, as A/D conversion is not performed, the SA-ADC result register is not updated, an A/D conversion termination interrupt is not generated, A/D conversion does not terminate automatically, and bit 0 (SARUN) of the SA-ADC control register (SADCON1) remains "1".

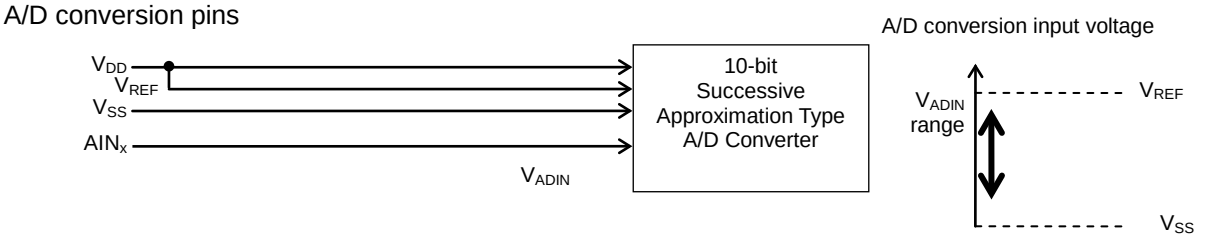


Figure 15-2 The A/D conversion pins and the conversion range

15.3.2 Operation of the Successive Approximation A/D Converter

For direct input, operate SA-ADC in the following procedure.

1. Before starting the SA-ADC, start oscillation of the high-speed clock (HSCLK) and wait until the oscillation stabilizes.
2. Set the SA-ADC mode register 0 (SADMOD0).
3. When bit 0 (SARUN) of SA-ADC control register 1 (SADCON1) is set to "1", the SA-ADC circuit becomes active and performs A/D conversion from the channel that is selected in the SA-ADC mode register (SADMOD0).
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADR0L, SADR0H), and when A/D conversion of the channel that is selected is terminated, an SA-ADC conversion termination interrupt (ADSINT) is generated.

Even if a channel is switched during A/D conversion, the channel that was selected at the start of A/D conversion is used until an A/D conversion termination interrupt occurs.
Figure 15-2 shows the SA-ADC operation timing when channel 0 and channel 1 are selected.

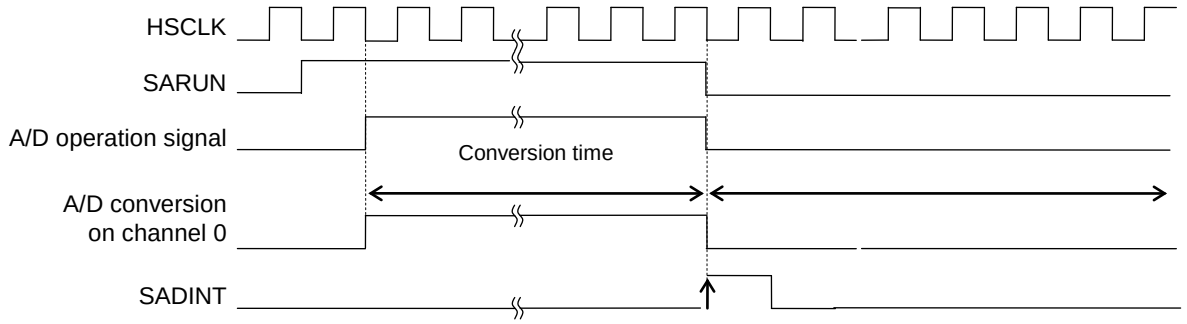


Figure 15-3 SA-ADC Operation Timing

Chapter 16

Voltage Level Supervisor

16 Voltage Level Supervisor

16.1 Overview

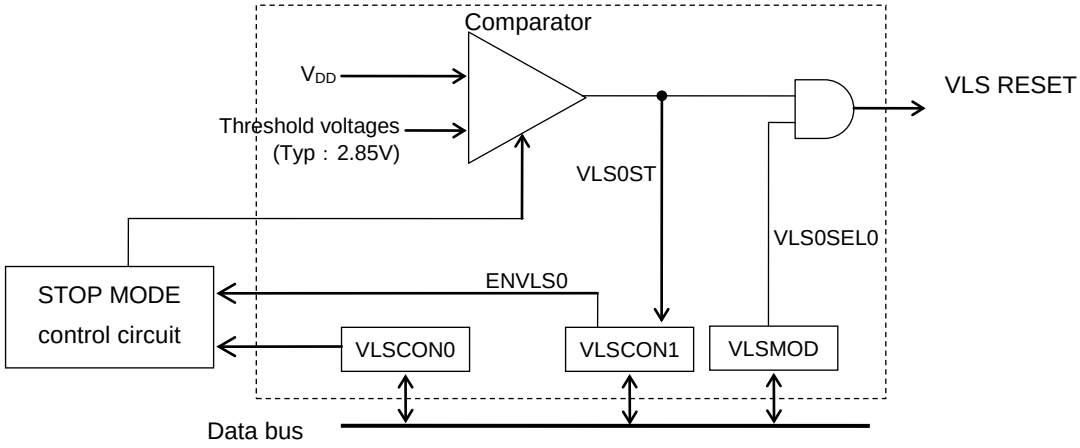
This LSI includes two channels of the voltage level supervisor (VLS).

16.1.1 Features

- The threshold voltages of VLS0 (V_{DD} fall) : 2.85V (typ)
  (V_{DD} rise) : 2.92V (typ)
- The threshold voltages of VLS1 (V_{DD}) : 2 types selectable 3.295V/ 3.625V(typ)
- The voltage level supervisor 0 can be used as the voltage level detector reset(VLS RESET).

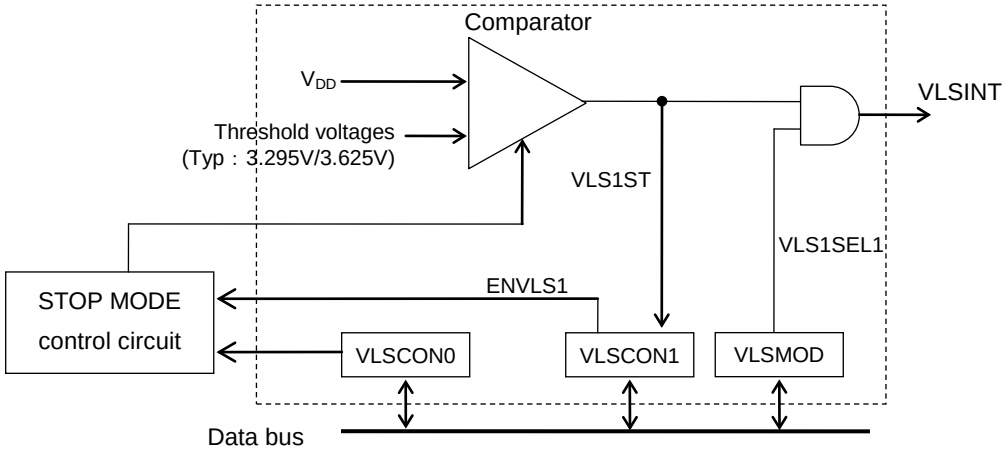
16.1.2 Configuration

VLS consists of the comparator and threshold voltage select circuits.
Figure 16-1 shows the configuration of the voltage level supervisor 0.
Figure 16-2 shows the configuration of the voltage level supervisor 1.



VLSCON0 : Voltage level supervisor control register 0
VLSCON1 : Voltage level supervisor control register 1
VLSMOD : Voltage level supervisor mode register

Figure 16-1 Configuration of Voltage Level Supervisor 0



VLSCON0 : Voltage level supervisor control register 0
VLSCON1 : Voltage level supervisor control register 1
VLSMOD : Voltage level supervisor mode register

Figure 16-2 Configuration of Voltage Level Supervisor 1

16.2 Description of Registers

16.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0D8H	Voltage level supervisor control register 0	VLSCON0	VLSCON	R/W	8/16	00H
0F0D9H	Voltage level supervisor control register 1	VLSCON1		R/W	8	—
0F0DAH	Voltage level supervisor mode register	VLSMOD	−	R/W	8	00H

16.2.2 Voltage Level Supervisor Control Register 0 (VLSCON0)

Address: 0F0D8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VLSCON0	—	—	DVLSSP	—	—	—	—	VLS0
R/W	R	R	R/W	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

VLSCON0 is a special function register (SFR) to control the voltage level supervisor (VLS).

[Description of Bits]

- **DVLSSP** (bit 5)
  The DVLSSP bit is used to control the voltage level supervisor operation during the STOP mode. If the voltage level supervisor is operating with DVLSSP set to "1", it automatically stops when the mode transits to the STOP mode. If the voltage level supervisor is operating with DVLSSP set to "0", it continues operating even when the mode transits to the STOP mode.

DVLSSP	Description
0	Does not control the voltage level supervisor operation during the STOP mode (initial value)
1	Stops the voltage level supervisor automatically during the STOP mode

- **VLS0** (bit 0)
  The VLS0 bit is used to select a threshold voltage of the VLS0.

VLS0	Description
0	3.295V (initial value)
1	3.625V

16.2.3 Voltage Level Supervisor Control Register 1 (VLSCON1)

Address: 0F0D9H
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
VLSCON1	—	—	VLS1ST	ENVLS1	—	—	VLS0ST	ENVLS0
R/W	R	R	R/W	R/W	R	R	R	R/W
Initial value	0	0	X	0	0	0	X	0

VLSCON1 is a special function register (SFR) to control the voltage level supervisor (VLS).

[Description of Bits]

- **ENVLS0** (bit 0)
  ENVLS0 bit is used to control activation (ON) or deactivation (OFF) of the VLS0.
  The VLS0 is activated (ON) and deactivated (OFF) by setting the ENVLS0 bit to "1" and "0", respectively.

ENVLS0	Description
0	VLS0 OFF
1	VLS0 ON（initial value）

- **VLS0ST**（bit 1）
  VLS0ST is the voltage level detection flag 0.
  It becomes "1" if the power supply voltage (V_{DD}) is higher than the threshold voltage and "0" if the power supply voltage is lower than the threshold voltage. When ENVLS0 is "0", VLS0ST is fixed to"0".

VLS0ST	Description
0	Higher than the threshold voltage
1	Lower than the threshold voltage

- **ENVLS1**（bit 4）
  ENVLS1 bit is used to control activation (ON) or deactivation (OFF) of the VLS1.
  The VLS1 is activated (ON) and deactivated (OFF) by setting the ENVLS1 bit to "1" and "0", respectively.

ENVLS1	Description
0	VLS1 OFF
1	VLS1 ON（initial value）

- **VLS1ST**（bit 5）
  VLS1ST is the voltage level detection flag 1.
  It becomes "1" if the power supply voltage (V_{DD}) is higher than the threshold voltage and "0" if the power supply voltage is lower than the threshold voltage. When ENVLS1 is "0", VLS1ST is fixed to"0".

VLS1ST	Description
0	Higher than the threshold voltage
1	Lower than the threshold voltage

16.2.4 Voltage Level Supervisor Mode Register (VLSMOD)

Address: 0F0DAH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VLSMOD	—	—	VLS1SEL	—	—	—	—	VLS0SEL
R/W	R	R	R/W	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

VLSMOD is a special function register (SFR) to select the mode of operation when detecting the voltage level.

[Description of Bits]

- **VLS0SEL0** (bit 0)

The VLS0SEL0 bits is used to control enable/disable of the voltage level detector reset function of VLS0.
If VLS0SEL0 is set to "1", a VLS reset function will be enabled, and if VLS0SEL0 is set to "0", it will be disabled.

VLS0SEL0	Description
0	Voltage level supervisor reset function of VLS0: Disabled (initial value)
1	Voltage level supervisor reset function of VLS0: Enabled

- **VLS1SEL1** (bit 5)

The VLS1SEL1 bits is used to control enable/disable of the interrupt request function of VLS1.
If VLS1SEL1 is set to "1", a VLS reset function will be enabled, and if VLS1SEL1 is set to "0", it will be disabled.

VLS1SEL1	Description
0	Interrupt request function of VLS1: Disabled (initial value)
1	Interrupt request function of VLS1: Enabled

16.3 Description of Operation

16.3.1 Threshold Voltage

The threshold voltage (V_{LSD}) is selected by setting the bits of VLSCON0.
Table 16-1 shows the threshold voltages.

Table 16-1 Threshold Voltages and Accuracy

		Threshold voltage V_{VLS}
VLS 0（V_{DD} fall）		2.85V
VLS 0（V_{DD} rise）		2.92V
VLS 1	VLS0=0	3.295V
	VLS0=1	3.625V

16.3.2 Operation of Voltage Level Supervisor

For the voltage level supervisor, the ENVLSn bit of the voltage level supervisor control register 1 (VLSCON1) controls ON/OFF, and the VLP0SEL0 bit of VLSMOD controls enable/disable of the low level detector reset function of VLS0.
When ENVLSn, the enable control bit of the voltage level supervisor, is set to "1", the supervisor is activated (ON). When ENVLSn is set to "0", the voltage level supervisor is deactivated (OFF) and has no supply current.
The voltage level supervisor requires a settling time. Set the VLS0SEL0, VLS1SEL0 bit to "1" 1ms or more after the ENVLSn bit is set to "1".
Figure 16-3 shows an example of the operation timing diagram with the voltage level detection flag (VLSnST).
Figure 19-4 shows an example of the operation timing diagram with the low level detector reset function enabled.

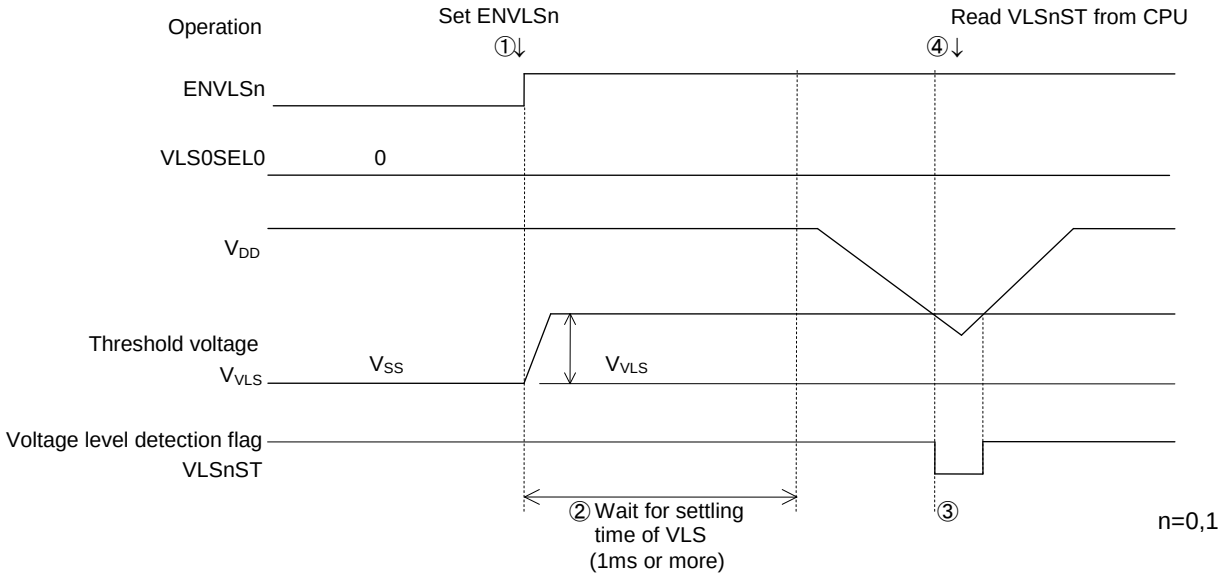


Figure 16-3 Example of Operation Timing Diagram with voltage level detection flag (VLSnST)

The operations in Figure 16-3 are described below.

1) Set ENVLSn to "1" to turned on the voltage level supervisor.
2) Wait the settling time (min. 1 ms) of the voltage level supervisor.
3) When V_{DD} drops, the voltage level detection flag (VLSnST) becomes "0".
4) Read VLSnST from CPU.

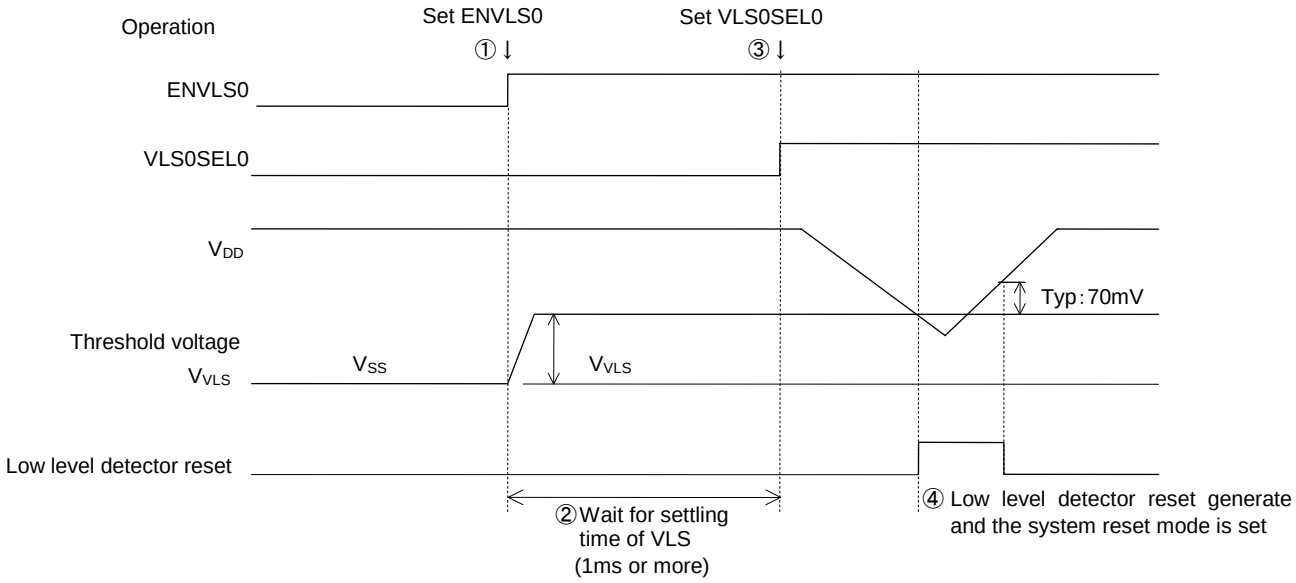


Figure 16-4 Example of Operation Timing Diagram with low level detector reset function enabled(VLS0)

The operations in Figure 16-4 are described below.

① Set ENVLS0 to "1" to turned on the voltage level supervisor.
② Wait the settling time (min. 1 ms) of the voltage level supervisor
③ Set VLS0SEL0 to "1" to enabled level detector reset function.
④ V_{DD} drops and low voltage low voltage level detector reset, and then the system reset mode is set.

Chapter 17

Analog Comparator

17 Analog Comparator

17.1 Overview

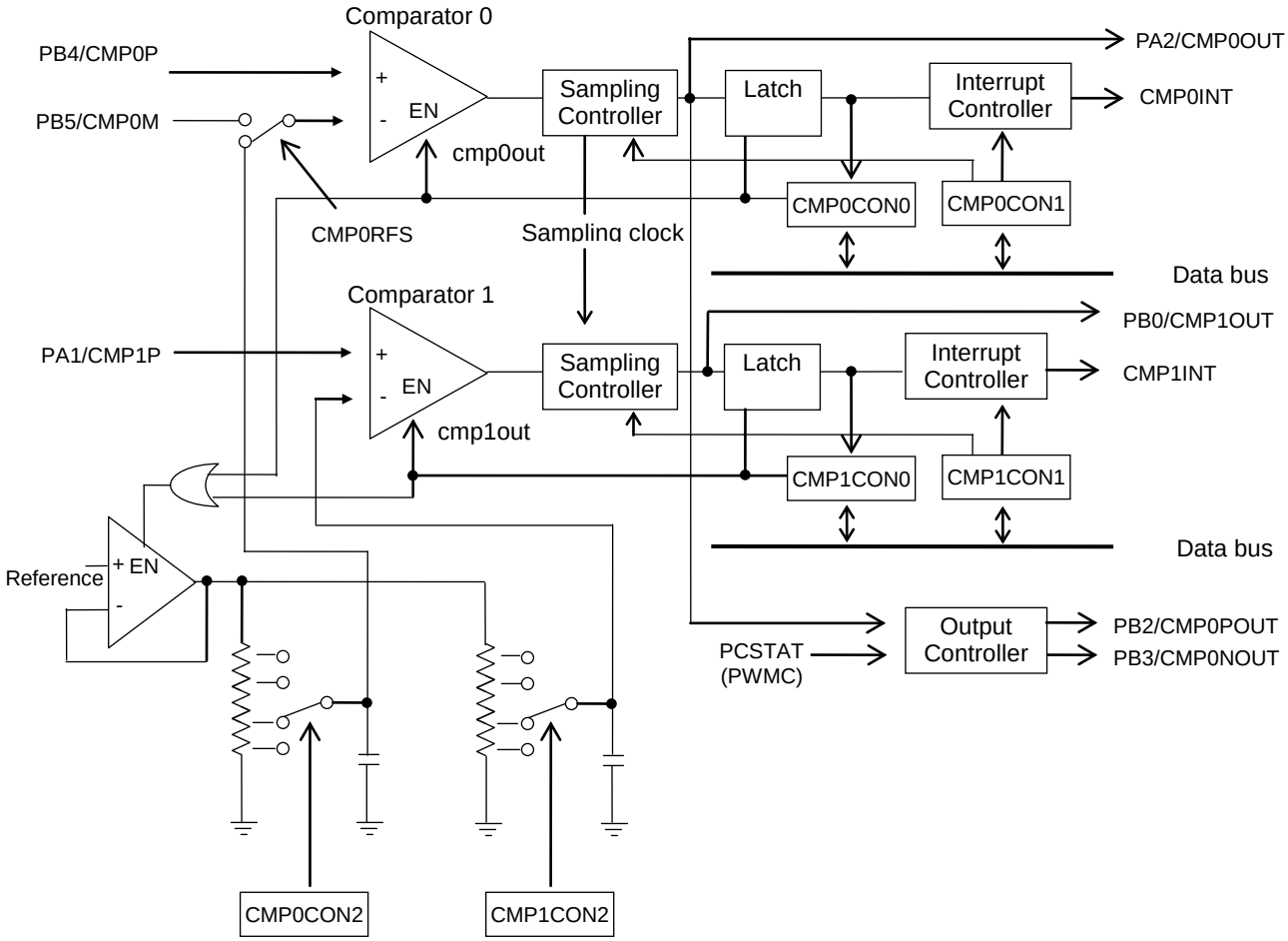
This LSI includes 2 channels of analogue comparator.
Voltage comparison (differential input) between two pins (CMP0P, CMP0M) that are input to the comparator is available.

17.1.1 Features

- The comparator output can generate an interrupt.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ, T128KHZ, T256KHZ)
- The last status of comparator output (CMPnD) remains after the comparator is deactivated.
- The comparator 0 includes 20mV hysteresis at typ.

17.1.2 Configuration

Figure 17-1 shows the configuration of the Comparator.



CMP0/1CON0: Comparator 0/1 control register 0
CMP0/1CON1: Comparator 0/1 control register 1
CMP0/1CON2: Comparator 0/1 control register 2

Figure 17-1 Configuration of Analog Comparator

17.1.3 List of Pins

Pin name	I/O	Description
PB4/CMP0P	I	Analog comparator 0 non-inverted input pin
PB5/CMP0M	I	Analog comparator 0 inverted input pin
PA2/CMP0OUT	O	Analog comparator 0 output pin
PB2/CMP0POUT	O	Analog comparator 0 output pin
PB3/CMP0NOUT	O	Analog comparator 0 output pin
PA1/CMP1P	I	Analog comparator 1 non-inverted input pin
PB0/CMP1OUT	O	Analog comparator 1 output pin

17.2 Description of Registers

17.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F950H	Comparator 0 control register 0	CMP0CON0	—	R/W	8	00H
0F951H	Comparator 0 control register 1	CMP0CON1	—	R/W	8	00H
0F952H	Comparator 0 control register 2	CMP0CON2	—	R/W	8	08H
0F954H	Comparator 1 control register 0	CMP1CON0	—	R/W	8	00H
0F955H	Comparator 1 control register 1	CMP1CON1	—	R/W	8	00H
0F956H	Comparator 1 control register 2	CMP1CON2	—	R/W	8	08H

17.2.2 Comparator 0 control register 0 (CMP0CON0)

Address: 0F950H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP0CON	—	—	—	—	—	—	CMP0D	CMP0EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

CMP0CON0 is a special function register (SFR) to control the comparator.

Description of Bits

- **CMP0EN** (bit 0)
  The CMP0EN bit is used to control ON/OFF of the comparator 0.When CMP0EN is set to "1", the comparator 0 is turned on. When it is set to "0", the comparator 0 is turned off.

CMP0EN	Description
0	Comparator 0 OFF (initial value)
1	Comparator 0 ON

- **CMP0D** (bit 1)
  CMP0D indicates the status of the comparator 0 output (CMP0OUT in Figure 17-1).It is set to "1" when the PB4 pin voltage is higher than the PB5 pin voltage (PB4>PB5). It is set to "0" when the PB4 pin voltage is lower than the PB5 pin voltage (PB4<PB5).It holds the last status even after the comparator 0 is turned off (CMP0EN is set to "0").

CMP0D	Description
0	PB4 < PB5 (initial value)
1	PB4 > PB5

17.2.3 Comparator 0 control register 1 (CMP0CON1)

Address: 0F951H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP0CON1	—	—	—	CMP0 RFS	CMP0 SM1	CMP0 SM0	CMP0E1	CMP0E0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CMP0CON1 is a special function register (SFR) to control the comparator 0 interrupt.

Description of Bits

- **CMP0E0, CMP0E1** (bit 0, bit 1)
  The CMP0E0 and CMP0E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.

CMP0E1	CMP0E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

Description of Bits

- **CMP0SM0, CMP0SM1** (bit 2, bit 3)
  The CMP0SM0 and CMP0SM1 bits are used to select with/without sampling for the comparator 0 comparison.

CMP0SM1	CMP0SM0	Description
0	0	Detects without sampling (initial value)
0	1	Detects with sampling (T16KHZ)
1	0	Detects with sampling (T128KHZ)
1	1	Detects with sampling (T256KHZ)

Description of Bits

- **CMP0RFS** (bit 4)
  The CMP0RFS bit is used to select the reference voltage (Vref) of the comparator 0.

CMP0RFS	Description
0	Vref= (initial value): Internal reference input
1	Vref=PB5: Differential external input

Note:

- In STOP mode, since the sampling clock stops, no sampling is performed regardless of the values set in CMP0SM1/0.
- When the sampling (T256KHZ, T128KHZ) is selected, PLL must be operated.
- If VSL0 or VLS1(Voltage Level Supervisor0 or 1) is stopped in STOP mode, the internal reference voltage source in the comparator is also stopped. Set SFRs(Specific Function

Registers) so that the VSL0 or VSL1 can work in STOP mode when using the CMP0(Comparator 0) in the STOP mode. Set ENVLS0 bit or ENVLS1 bit of VLSCON1 register to "1" and set DVLSSP bit of VLSCON0 register. For more details about VLS, see Chapter 16, "Voltage Level Supervisor".

17.2.4 Comparator 0 control register 2 (CMP0CON2)

Address: 0F952H
Access: R/W
Access size: 8 bits
Initial value: 08H

	7	6	5	4	3	2	1	0
CMP0CON2	—	—	—	—	CMP0RF3	CMP0RF2	CMP0RF1	CMP0RF0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0

CMP0CON2 is a special function register (SFR) to select the reference voltage of the comparator 0.

Description of Bits

- **CMP0RF0, CMP0RF1, CMP0RF2, CMP0RF3** (bit 0, bit 1, bit 2, bit 3)
  The CMP0REF0, CMP0REF1, CMP0REF2, and CMP0REF3 bits are used to select the reference voltage of the comparator 0.
  This setting is valid when the reference voltage (Vref) of the comparator 0 is set to the internal reference input (CMP0RFS=0). A setting of 0h (0.05V) is possible without a guaranteed accuracy.

CMP0RF3	**CMP0RF2**	**CMP0RF1**	**CMP0RF0**	Comparator 0 Reference voltage
0	0	0	0	0.05V (no guaranteed accuracy)
0	0	0	1	0.10V
0	0	1	0	0.15V
0	0	1	1	0.20V
0	1	0	0	0.25V
0	1	0	1	0.30V
0	1	1	0	0.35V
0	1	1	1	0.40V
1	0	0	0	0.45V (initial value)
1	0	0	1	0.50V
1	0	1	0	0.55V
1	0	1	1	0.60V
1	1	0	0	0.65V
1	1	0	1	0.70V
1	1	1	0	0.75V
1	1	1	1	0.80V

17.2.5 Comparator 1 control register 0 (CMP1CON0)

Address: 0F954H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP1CON0	—	—	—	—	—	—	CMP1D	CMP1EN
R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

CMP1CON0 is a special function register (SFR) to control the comparator.

Description of Bits

- **CMP1EN** (bit 0)
  The CMP1EN bit is used to control ON/OFF of the Comparator 1.
  When CMP1EN is set to "1", the Comparator 1 is turned on. When it is set to "0", the Comparator 1 is turned off.

CMP1EN	Description
0	Comparator 1 OFF (initial value)
1	Comparator 1 ON

- **CMP1D** (bit 1)
  CMP1D indicates the status of the Comparator 1 output (CMP1OUT in Figure 17-1).
  It is set to "1" when the PA1 pin voltage is higher than the internal reference voltage (PA1>Internal reference voltage). It is set to "0" when the PA1 pin voltage is lower than the internal reference voltage (PA1<Internal reference voltage).
  It holds the last status even after the Comparator 1 is turned off (CMP1EN is set to "0").

CMP1D	Description
0	PA1 < Internal reference voltage (initial value)
1	PA1 > Internal reference voltage

17.2.6 Comparator 1 control register 1 (CMP1CON1)

Address: 0F955H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMP1CON1	—	—	—	—	CMP1SM1	CMP1SM0	CMP1E1	CMP1E0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CMP1CON1 is a special function register (SFR) to control the Comparator 1 interrupt.

Description of Bits

- **CMP1E0, CMP1E1** (bit 0, bit 1)
  The CMP1E0 and CMP1E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.

CMP1E1	CMP1E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

Description of Bits

- **CMP1SM0, CMP1SM1** (bit 2, bit 3)
  The CMP1SM0 and CMP1SM1 bits are used to select with/without sampling for the Comparator 1 comparison.

CMP1SM1	CMP1SM0	Description
0	0	Detects without sampling (initial value)
0	1	Detects with sampling (T16KHZ)
1	0	Detects with sampling (T128KHZ)
1	1	Detects with sampling (T256KHZ)

Note:

- In STOP mode, since the sampling clock stops, no sampling is performed regardless of the values set in CMP1SM1/0.
- When the sampling (T256KHZ, T128KHZ) is selected, PLL must be operated.
- If VSL0 or VLS1(Voltage Level Supervisor0 or 1) is stopped in STOP mode, the internal reference voltage source in the comparator is also stopped. Set SFRs(Specific Function Registers) so that the VSL0 or VSL1 can work in STOP mode when using the CMP1(Comparator 1) in the STOP mode. Set ENVLS0 bit or ENVLS1 bit of VLSCON1 register to "1" and set DVLSSP bit of VLSCON0 register. For more details about VLS, see Chapter 16, "Voltage Level Supervisor".

17.2.7 Comparator 1 control register 2 (CMP1CON2)

Address: 0F956H
Access: R/W
Access size: 8 bits
Initial value: 08H

	7	6	5	4	3	2	1	0
CMP1CON2	—	—	—	—	CMP1RF3	CMP1RF2	CMP1RF1	CMP1RF0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0

CMP1CON2 is a special function register (SFR) to select the reference voltage of the Comparator 1.

Description of Bits

- **CMP1RF0, CMP1RF1, CMP1RF2, CMP1RF3** (bit 0, bit 1, bit 2, bit 3)
  The CMP1REF0, CMP1REF1, CMP1REF2, and CMP1REF3 bits are used to select the reference voltage of the Comparator 1.
  This setting is valid when the reference voltage (Vref) of the Comparator 1 is set to the internal reference input (CMP1RFS=0). A setting of 0h (0.05V) is possible without a guaranteed accuracy.

CMP1RF3	**CMP1RF2**	**CMP1RF1**	**CMP1RF0**	Comparator 1 Reference voltage
0	0	0	0	0.05V (no guaranteed accuracy)
0	0	0	1	0.10V
0	0	1	0	0.15V
0	0	1	1	0.20V
0	1	0	0	0.25V
0	1	0	1	0.30V
0	1	1	0	0.35V
0	1	1	1	0.40V
1	0	0	0	0.45V (initial value)
1	0	0	1	0.50V
1	0	1	0	0.55V
1	0	1	1	0.60V
1	1	0	0	0.65V
1	1	0	1	0.70V
1	1	1	0	0.75V
1	1	1	1	0.80V

17.3 Description of Operation

17.3.1 Comparator Functions

The comparator compares the input voltages of the CMPnP and CMPnM pins to output the result to the CMPnD bit of the comparator control register 0 (CMPnCON0).
CMPnEN of CMPnCON0 is controlled by the comparator enable. When CMPnEN is set to "1", the comparator is activated (ON). When CMPnEN is set to "0", the comparator is deactivated (OFF) and has no supply current.
The comparison result is read from the CMPnD bit. When CMPnD is "1", it indicates that the input voltage of the CMPnP pin is higher than that of the CMPnM pin. When CMPnD is "0", it indicates that the input voltage of the CMPnP pin is lower than that of the CMPnM pin.
The comparator requires a settling time. Read CMPnD bit 3ms or more after CMPnEN bit is set to "1".
Figure 17-2 shows an example of the operation timing diagram.

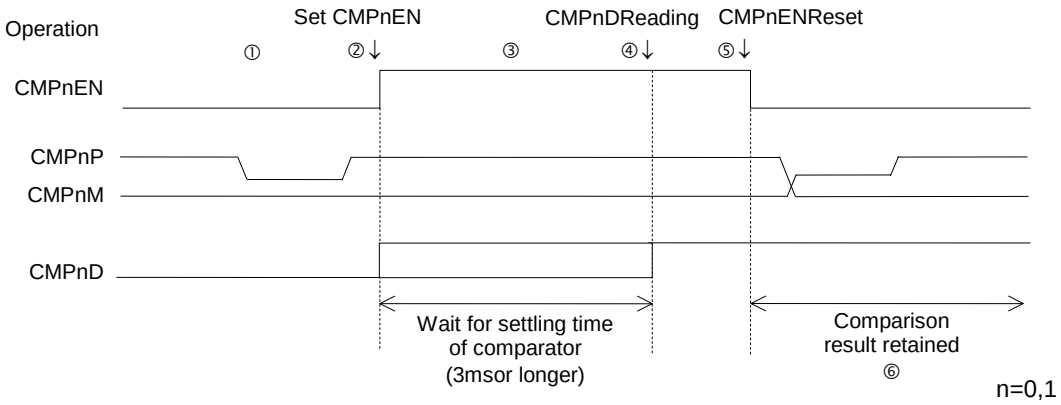


Figure 17-2 Example of Operation Timing Diagram (n=0,1)

The operations in Figure 17-2 are described below.

① Select the interrupt mode by CMPnCON1.
② Set CMPnEN to "1" to turn on the comparator.
③ Wait the settling time (min. 3 ms) of the comparator.
④ Read the comparison result (CMPnD).
⑤ Set CMPnEN to "0" to turn off the comparator. At the same time, the result is retained.

CMPnD can be read after CMPnEN is set to "0" because CMPnD holds the comparison result at the time when CMPnEN is set to "0".

17.3.2 Analog Comparator Output Function

The comparator 0 outputs CMP0POUT, CMP0NOUT by the PCSTAT bit (the bit 7 of the PWCCON1) which indicate PMMC is counting.
Figure 17-3 shows the operation timing diagram of CMP0POUT, CMP0NOUT in the count start by software and in the count stop by external trigger of CMP0.

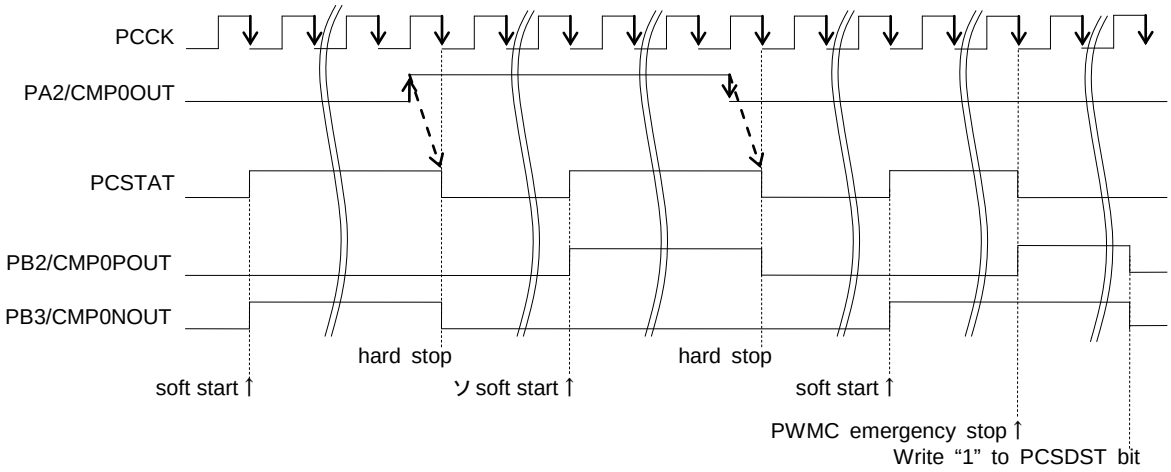
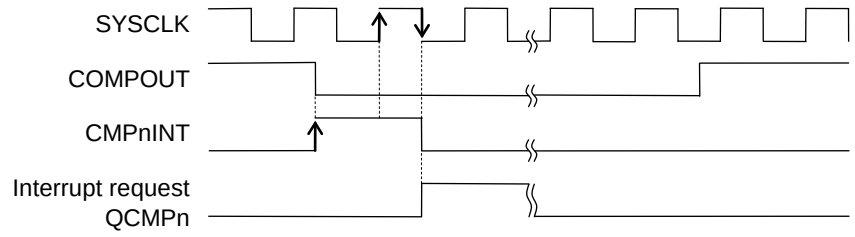


Figure 17-3 Operation Timing Diagram of CMP0POUT, CMP0NOUT

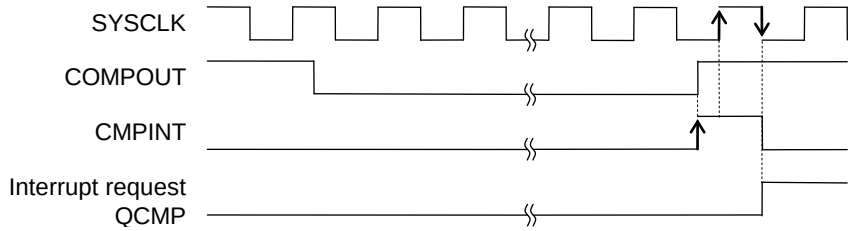
【Note】
When PWMC stops urgently, both CMP0POUT and CMP0NOUT are set to "H" levels.
When "1" is written in the PCSDST bit of PWMC control register 1 (PWMCON1) of PWMC, the PCSDST bit is set to "0" and both CMP0POUT and CMP0NOUT are set to "L" levels at the same time.
For PWM, see Chapter 10, "PWM ".

17.3.3 Interrupt Request

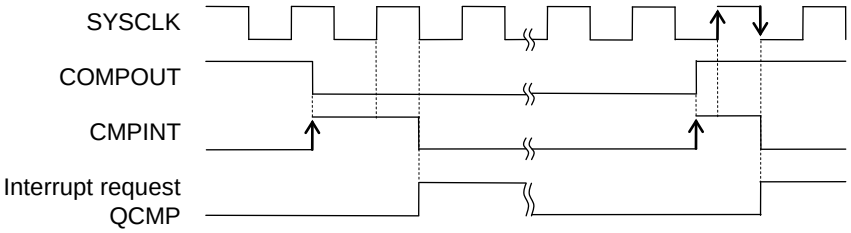
When an interrupt edge selected by the comparator control register 1 (CMPnCON1) occurs on the comparison result of the comparator, a comparator interrupt (CMPnINT) is generated. For the comparator interrupt, the edge can be selected.
Figure 17-4 shows the interrupt generation timing in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling, and in rising-edge interrupt mode with sampling.



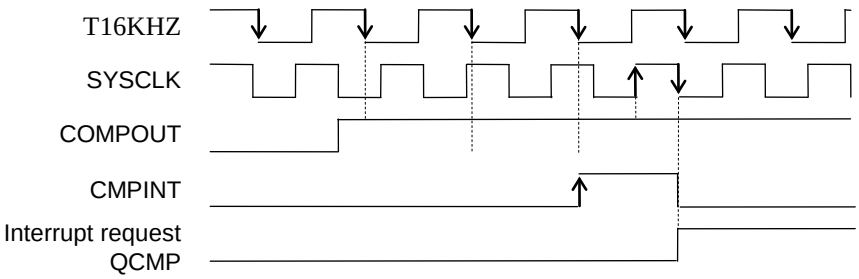
(a) When Falling-Edge Interrupt Mode without Sampling is Selected



(b) When Rising-Edge Interrupt Mode without Sampling is Selected



(c) When Both-Edge Interrupt Mode without Sampling is Selected



(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 17-4 Comparator Interrupt Generation Timing

Chapter 18

On-chip Debug

18 On-Chip Debug Function

18.1 Overview

This LSI has an on-chip debug function allowing Flash memory rewriting.
The on-chip debug emulator (uEASE) is connected to this LSI to perform the on-chip debug function.

18.2 Method of Connecting to On-Chip Debug Emulator

Figure 18-1 shows the connection to the on-chip debug emulator (uEASE).
For the on-chip debug emulator, refer to the "uEASE User's Manual."

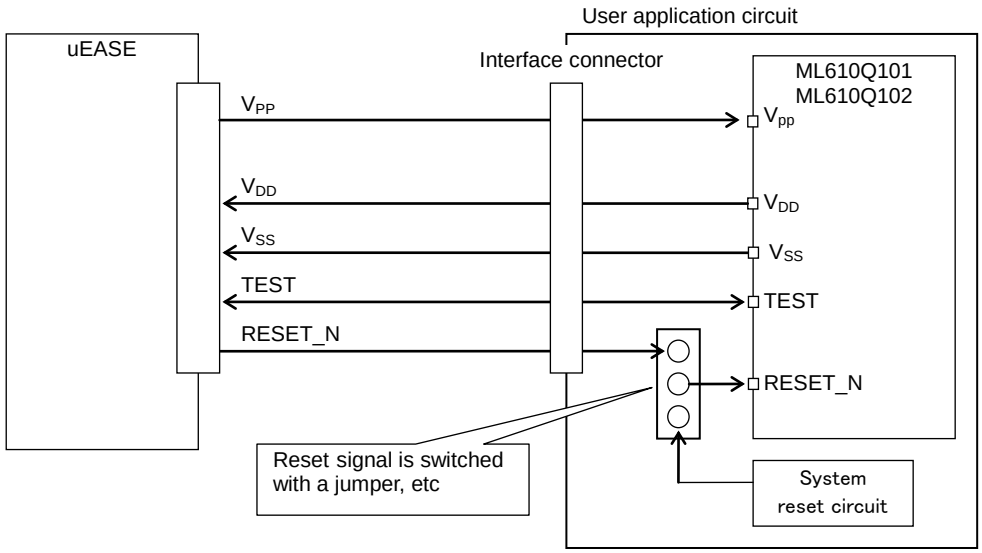


Figure 18-1 Connection to On-chip Debug Emulator (uEASE)

Note:

•Please do not apply LSIs being used for debugging to mass production.

•When using the on-chip debug function or the flash rewrite function after mounting of the board, design the board so that the 5 pins (VPP, V_{DD}, V_{SS}, RESET_N, TEST) required for connection to the on-chip debug emulator can be connected.

•"4.5V to 5.5V" has to be supplied to V_{DD} while debugging and writing flash.

• When μEASE connecting, please do not connect the capacity of more than 100 pF of parasitic capacitance inclusion between the RESET_N pin and the VSS pin. A communication error can't bring and normally debug a program any more.

When the system reset circuit is included in the user application circuit, enable switching of the connection in the user application circuit, as shown above. When the system reset circuit is not included in the user application circuit, the RESET_N pin can be connected directy to the RESET_N pin of this LSI.

•Please start a debugger after canceling stop mode.

For details, see "uEASE User's Manual" and "uEASE Target Connection Manual".

Appendixes

Appendix A Registers

Contents of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H
0F001H	Reset status register	RSTAT	—	R/W	8	Undefined
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	3BH
0F003H	Frequency control register 1	FCON1		R/W	8	00H
0F008H	Stop code acceptor	STPACP	—	W	8	Undefined
0F009H	Standby control register	SBYCON	—	W	8	00H
0F00AH	Low-speed time base counter divide register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter divide register	HTBDR	—	R/W	8	00H
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H
0F010H	Interrupt enable register 0	IE0	—	R/W	8	00H
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H
0F024H	Port AB interrupt control register 0	PABICON0	—	R/W	8	00H
0F025H	Port AB interrupt control register 1	PABICON1	—	R/W	8	00H
0F026H	Port AB interrupt control register 2	PABICON2	—	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H
0F02EH	Block control register 6	BLKCON6	—	R/W	8	00H
0F02FH	Block control register 7	BLKCON7	—	R/W	8	00H
0F0D8H	Voltage Level Supervisor control register 0	VLSCON0	VLSCON	R/W	8/16	00H
0F0D9H	Voltage Level Supervisor control register 1	VLSCON1		R/W	8	Undefined
0F0DAH	Voltage Level Supervisor mode register	VLSMOD	−	R/W	8	00H
0F250H	Port A data register	PAD	—	R/W	8	00H
0F251H	Port A direction register	PADIR	—	R/W	8	00H
0F252H	Port A control register 0	PACON0	PACON	R/W	8/16	00H
0F253H	Port A control register 1	PACON1		R/W	8	00H
0F254H	Port A mode register 0	PAMOD0	PAMOD	R/W	8/16	00H
0F255H	Port A mode register 1	PAMOD1		R/W	8	00H
0F258H	Port B data register	PBD	—	R/W	8	00H
0F259H	Port B direction register	PBDIR	—	R/W	8	00H
0F25AH	Port B control register 0	PBCON0	PBCON	R/W	8/16	00H
0F25BH	Port B control register 1	PBCON1		R/W	8	00H
0F25CH	Port B mode register 0	PBMOD0	PBMOD	R/W	8/16	00H
0F25DH	Port B mode register 1	PBMOD1		R/W	8	00H

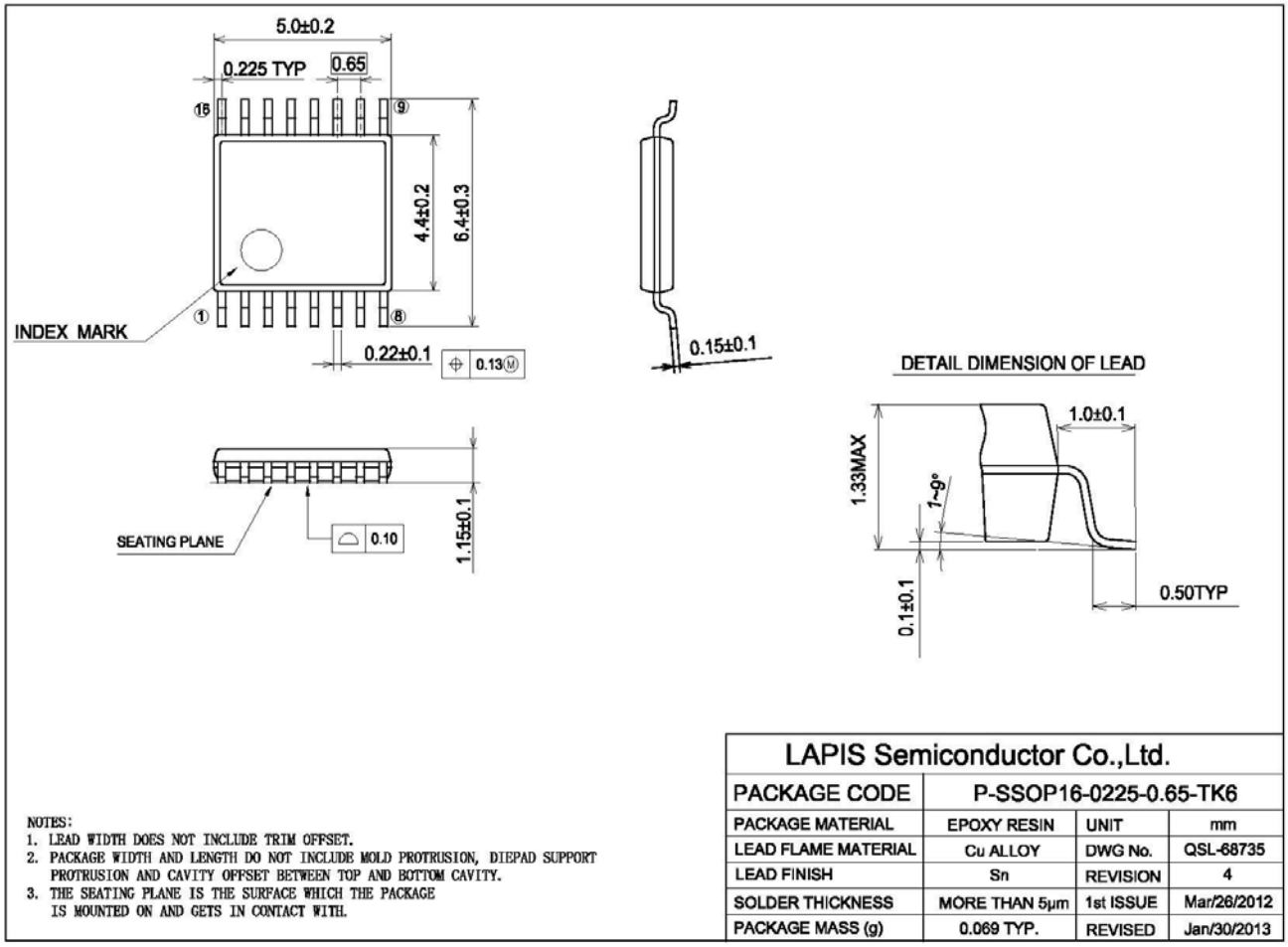
Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2F1H	SA-ADC control register 1	SADCON1	—	R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	—	R/W	8	00H
0F360H	Timer E data register	TMED	TMEDC	R/W	8/16	0FFH
0F361H	Timer E counter register	TMEC		R/W	8	00H
0F362H	Timer E control register 0	TMECON0	TMECON	R/W	8/16	00H
0F363H	Timer E control register 1	TMECON1		R/W	8	00H
0F364H	Timer E control register 2	TMECON2	TMECON23	R/W	8/16	00H
0F365H	Timer E control register 3	TMECON3		R/W	8	00H
0F368H	Timer F data register	TMFD	TMFDC	R/W	8/16	0FFH
0F369H	Timer F counter register	TMFC		R/W	8	00H
0F36AH	Timer F control register 0	TMFCON0	TMFCON	R/W	8/16	00H
0F36BH	Timer F control register 1	TMFCON1		R/W	8	00H
0F36CH	Timer F control register 2	TMFCON2	TMFCON23	R/W	8/16	00H
0F36DH	Timer F control register 3	TMFCON3		R/W	8	00H
0F8E0H	Timer 8 data register	TM8D	TM8DC	R/W	8/16	0FFH
0F8E1H	Timer 8 counter register	TM8C		R/W	8	00H
0F8E2H	Timer 8 control register 0	TM8CON0	TM8CON	R/W	8/16	00H
0F8E3H	Timer 8 control register 1	TM8CON1		R/W	8	00H
0F8E4H	Timer 9 data register	TM9D	TM9DC	R/W	8/16	0FFH
0F8E5H	Timer 9 counter register	TM9C		R/W	8	00H
0F8E6H	Timer 9 control register 0	TM9CON0	TM9CON	R/W	8/16	00H
0F8E7H	Timer 9 control register 1	TM9CON1		R/W	8	00H
0F8E8H	Timer A data register	TMAD	TMADC	R/W	8/16	0FFH
0F8E9H	Timer A counter register	TMAC		R/W	8	00H
0F8EAH	Timer A control register 0	TMACON0	TMACON	R/W	8/16	0A0H
0F8EBH	Timer A control register 1	TMACON1		R/W	8	00H
0F8ECH	Timer B data register	TMBD	TMBDC	R/W	8/16	0FFH
0F8EDH	Timer B counter register	TMBC		R/W	8	00H
0F8EEH	Timer B control register 0	TMBCON0	TMBCON	R/W	8/16	00H
0F8EFH	Timer B control register 1	TMBCON1		R/W	8	00H
0F910H	PWMC period register L	PWCPL	PWCP	R/W	8/16	0FFH
0F911H	PWMC period register H	PWCPH		R/W	8	0FFH
0F912H	PWMC duty register L	PWCDL	PWCD	R/W	8/16	00H
0F913H	PWMC duty register H	PWCDH		R/W	8	00H
0F914H	PWMC counter register L	PWCCL	PWCC	R/W	8/16	00H
0F915H	PWMC counter register H	PWCCH		R/W	8	00H
0F916H	PWMC control register 0	PWCCON0	PWCCON	R/W	8/16	00H
0F917H	PWMC control register 1	PWCCON1		R/W	8	00H
0F918H	PWMC control register 2	PWCCON2	PWCCON23	R/W	8/16	00H
0F919H	PWMC control register 3	PWCCON3		R/W	8	00H
0F91AH	PWMC wait register	PWCWAIT	—	R/W	8	00H
0F950H	Comparator 0 control register 0	CMP0CON0	—	R/W	8	00H
0F951H	Comparator 0 control register 1	CMP0CON1	—	R/W	8	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F952H	Comparator 0 control register 2	CMP0CON2	—	R/W	8	08H
0F954H	Comparator 1 control register 0	CMP1CON0	—	R/W	8	00H
0F955H	Comparator 1 control register 1	CMP1CON1	—	R/W	8	00H
0F956H	Comparator 1 control register 2	CMP1CON2	—	R/W	8	08H

Appendix B Package Dimensions

ML610Q101/ML610Q102 Package Dimensions(SSOP16)

(Unit: mm)



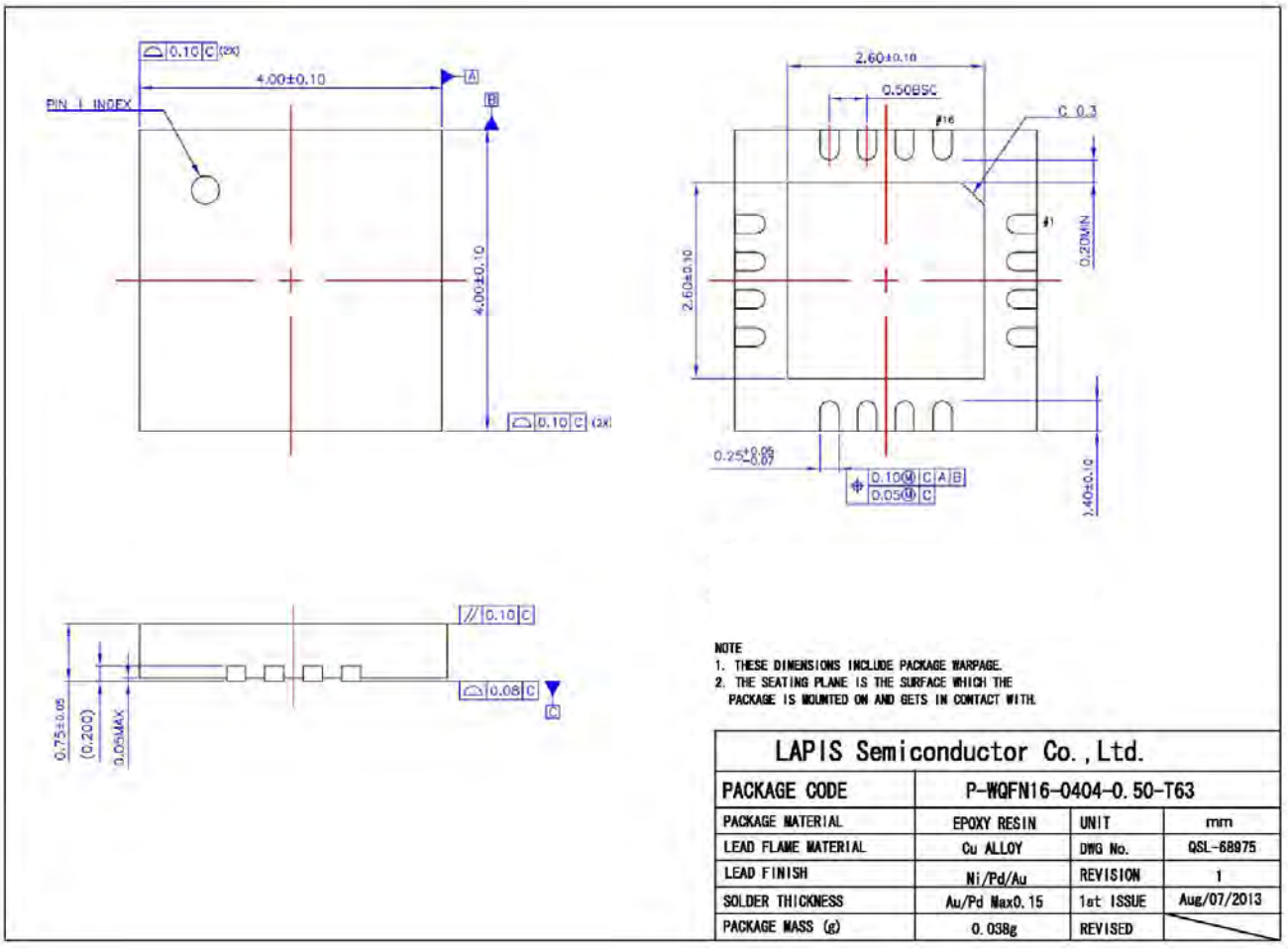
FigureB-1 P-SSOP16

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML610Q101/ML610Q102 Package Dimensions(WQFN16)

(Unit: mm)



FigureB-2 WQFN16

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Appendix C Electrical Characteristics

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Power supply voltage 2	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Ta = 25°C	–12 to +11	mA
Power dissipation	PD	Ta = 25°C	0.5	W
Storage temperature	T_{STG}	—	–55 to +150	°C

● Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–40 to +85	°C
Operating voltage	V_{DD}	—	2.7 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 2.7V to 5.5V	30k to 8.4M	Hz

● Operating Conditions of Flash Memory

(V_{SS}=0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Operating temperature	T_{OP}	At write/erase	0	—	+40	°C
Operating voltage	V_{DD}	At write/erase	4.5	—	5.5	V
	V_{PP}	At write/erase	7.7	—	8.3	
Rewrite counts	C_{EP}	—	—	—	80	cycles
Data retention*[1]	Y_{DR}	—	10	—	—	years

*[1] : However, please keep active time of the flash memory from exceeding ten years.

Vpp pin has internal pull-down resistor.

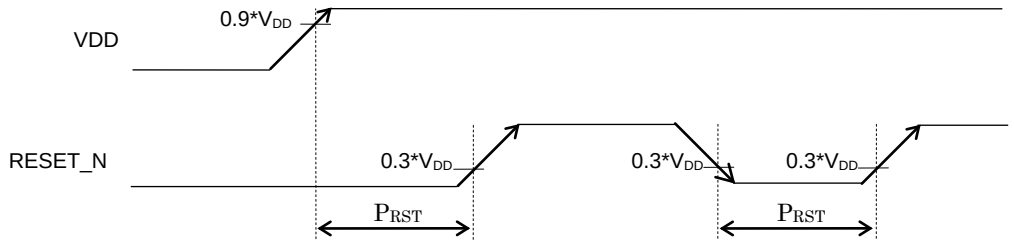
● DC Characteristics (1/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Low-speed RC oscillation frequency	f_{RCL}	Ta = 25°C	31	32.768	34	kHz	1
PLL oscillation frequency*1	f_{PLL}	Ta = 25°C	Typ. −1%	16.384	Typ. +1%	MHz	
		Ta = -10 to +85°C	Typ. -2%	16.384	Typ. +2%		
		Ta = −40 to +85°C	Typ. −2.5%	16.384	Typ. +2.5%		
Reset pulse width	T_{RST}	—	100	—	—	µs	
Reset noise elimination pulse width	T_{NRST}	—	—	—	0.4		
Power-on reset activation power rise slope	ΔV/ ΔT	0V to 2.0V	0.10	—	10	V/ms	

*1 : 1024 clock average. CPU clk is f_{PLL} /2 max.

● RESET



RESET_N pin reset

Power on reset

● DC Characteristics (2/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
VLS Judgment voltage	V_{VLS0F}	Ta=25°C , V_{DD}=fall		Typ −3.0 %	2.85	Typ +3.0 %	V	1
		V_{DD}=fall		Typ. −5.0 %	2.85	Typ. +5.0 %		
	V_{VLS0R}	Ta=25°C , V_{DD}=rise		Typ. −3.0 %	2.92	Typ. +3.0 %		
		V_{DD}=rise		Typ. −5.0 %	2.92	Typ. +5.0 %		
	V_{VLS1}	Ta=25°C	VLS0=0	Typ −3.0 %	3.295	Typ +3.0 %		
			VLS0=1		3.625			
		—	VLS0=0	Typ −5.0 %	3.295	Typ +5.0 %		
			VLS0=1		3.625			
Comparator0 In-phase input voltage range	V_{CMR}	—		0.1	—	V_{DD} -1.5	V	4
Comparator0 hysteresis	V_{HYSP}	Ta=25°C , V_{DD} = 5.0V		10	20	30	mV	
		V_{DD} = 5.0V		5	20	35		
Comparator0 Input offset voltage	V_{CMOF}	Ta=25°C , V_{DD} = 5.0V		—	—	7		
Comparator Reference-voltage error*3	V_{CMREF}	Ta=25°C		-25	—	25		
		—		-50	—	50		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta=-40 to +85°C	—	1	30	μA	1
Supply current 2	IDD2	CPU: In 32.768kHz operating state.*1 High-speed oscillation: Stopped.	Ta=-40 to +85°C	—	3.7	6	mA	

*1 : LTBC and WDT are operating ,and significant bits of BLKCON0 to BLKCON4 registers are all "1".

*2 : When the CPU operating rate is 100%. Minimum instruction execution time: Approx 0.122 μs (at 8.192MHz system clock)

*3 :Comparator input offset voltage is included.

● DC Characteristics (3/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage	VOH	IOH1 = −3.0mA, V_{DD} = 4.5V *1	V_{DD} −0.7	—	—	V	2
	VOL	IOL1 = +8.5mA, V_{DD} = 4.5V *1	—	—	0.6		
Output leakage	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	+1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	−1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}	—	—	1	μA	4
	IIL1	VIL1 = V_{SS}, V_{DD} = 5.0V	−650	−500	−350		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD} = 5.0V	20	115	200		
	IIL1	VIL1 = V_{SS}	−1	—	—		
Input current 2 (PA0-PA2) (PB0-PB7)	IIH2	VIH2 = V_{DD} = 5.0V (when pulled-down)	20	115	200		
	IIL2	VIL2 = V_{SS}, V_{DD}=5.0V (when pulled-up)	−200	−100	−20		

*1 : When the one terminal output state.

● DC Characteristics (4/4)

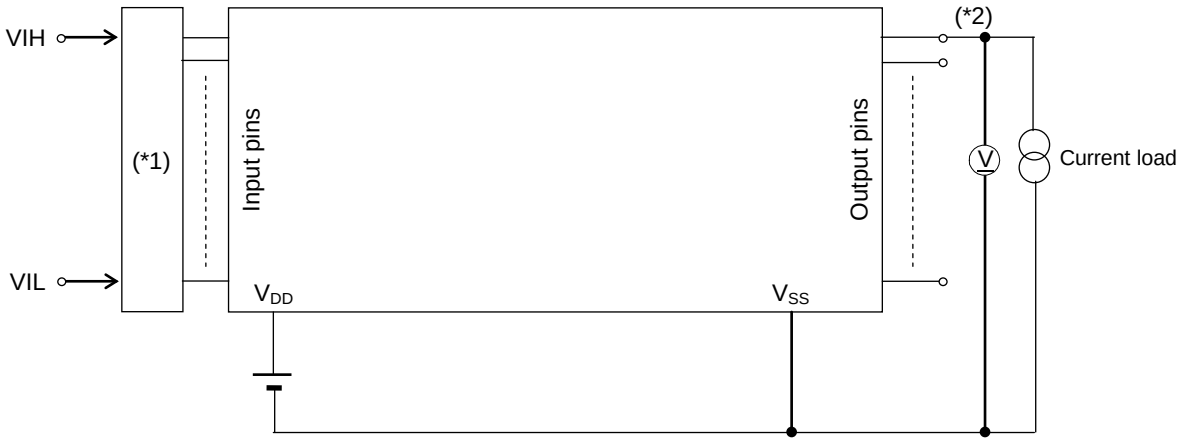
(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (PA0 to PA2) (PB0,to PB7)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	2
	VIL1	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (PA0 to PA2) (PB0 to PB7)	CIN	f = 10kHz Ta = 25°C	—	—	20	pF	—

● Measuring circuit

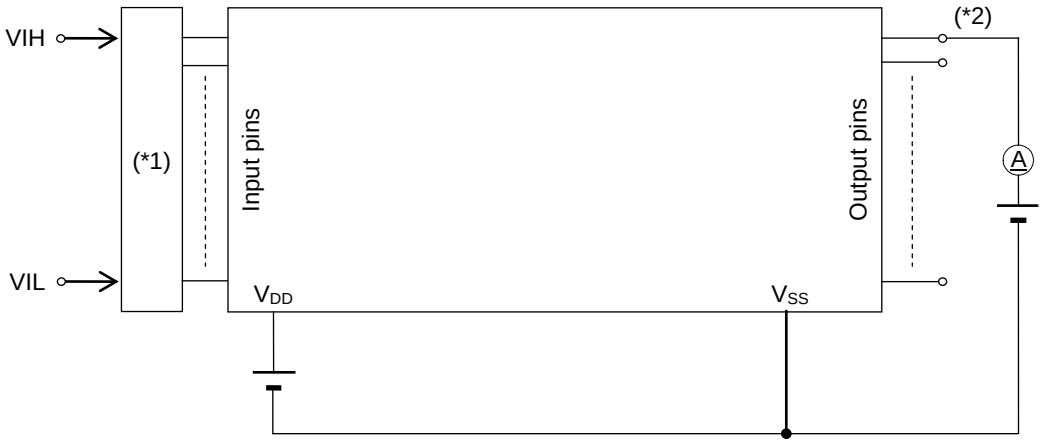
Measuring circuit 1

Measuring circuit 2



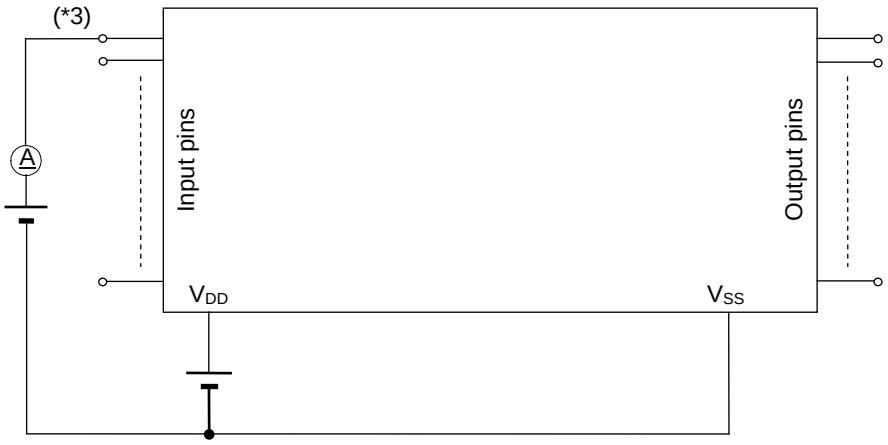
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 3



*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 4

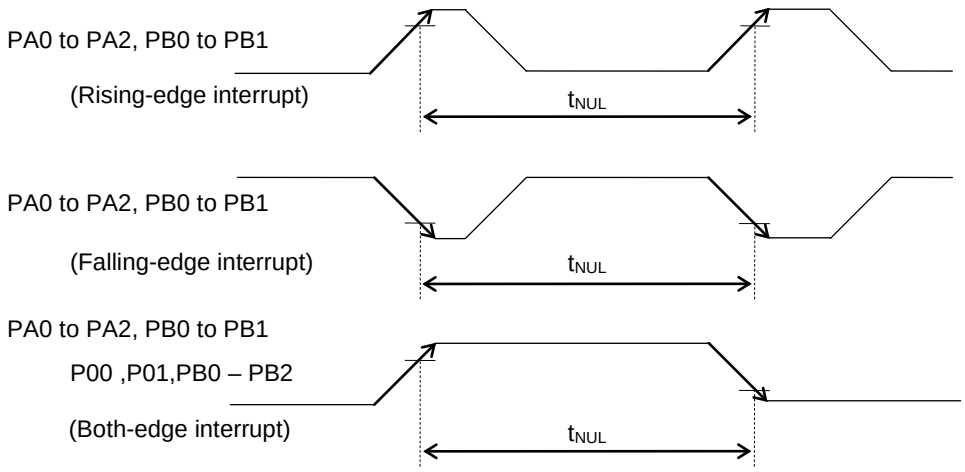


*3: Measured at the specified output pins.

● AC Characteristics (External Interrupt)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	2.5 x sysclk	—	3.5 x sysclk	µs

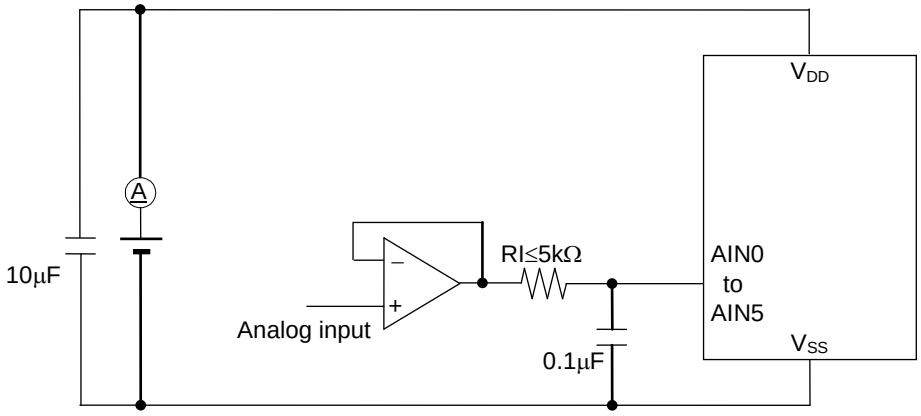


● Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	10	bit
Integral non-linearity error	INL	R_I≦5kΩ, HSCLK=8.192MHz	–4	—	+4	LSB
Differential non-linearity error	DNL	R_I≦5kΩ, HSCLK=8.192MHz	–3	—	+3	
Zero-scale error	V_{OFF}	R_I≦5kΩ, HSCLK=8.192MHz	–4	—	+4	
Full-scale error	FSE	R_I≦5kΩ, HSCLK=8.192MHz	–4	—	+4	
Allowable signal source impedance	R_I	—	—	—	5k	Ω
Conversion time	t_{CONV}	—	—	102	—	ϕ/CH

ϕ: f_{PLL}/2



Appendix D Check List

This Check List has notes to prevent commonly-made programming mistakes and frequently overlooked or misunderstood hardware features of the MCU. Check each note listed up chapter by chapter while coding the program or evaluating it using the MCU.

Chapter 1 Overview

•About unused pins

[ ] Please confirm how to handle the unused pins(Refer to Section 1.3.4 in the user's manual).

Chapter 2 CPU and Memory Space

(ML610Q101)

• Program Memory size

[ ] 4,064 Byte (0:0000H to 0:0FDFH)

• Data Memory size

[ ] 4,096 Byte (0:0000H to 0:0FFFH)

• Data RAM size

[ ] 256 Byte (0:E000H to 0:E0FFH)

(ML610Q102)

• Program Memory size

[ ] 6,112 Byte (0:0000H to 0:17DFH)

• Data Memory size

[ ] 6,144Byte (0:0000H to 0:17FFH)

• Data RAM size

[ ] 256 Byte (0:E000H to 0:E0FFH)

• Unused area

(ML610Q101)

[ ] Please fill test area 0:0FE0H to 0:0FFFH with BRK instruction code "0FFH" (Refer to a startup file "ML610101.asm" for programming in the source code).

[ ] For fail safe in your system, please fill unused program memory area (your program code does not use) with BRK instruction code "0FFH". Please fill the area with the code "0FFH" when you release a code for LAPIS Semiconductor's factory programming.

(ML610Q102)

[ ] Please fill test area 0:17E0H to 0:17FFH with BRK instruction code "0FFH" (Refer to a startup file "ML610102.asm" for programming in the source code).

[ ] For fail safe in your system, please fill unused program memory area (your program code does not use) with BRK instruction code "0FFH". Please fill the area with the code "0FFH" when you release a code for LAPIS Semiconductor's factory programming.

• Initializing RAM

[ ] The hardware reset does not initialize RAM. Please initialize RAM by the software.

Chapter 3 Reset Function

• Reset activation pulse width

[ ] Minimum 100us (Refer to Appendix C-2 in the user's manual)

[ ] There is no flag which shows that the reset by RESET_N pin occurred (Refer to 3.2.2 in the user's manual).

• BRK instruction reset

[ ] In system reset by the BRK instruction, no special function register (SFR) is initialized either. Therefore initialize the SFRs by your software (Refer to 3.3.1 in the user's manual).

Chapter 4 MCU Control Function

•STOP mode

[ ] Please note the STPACP is not enabled when both interrupt enable flags and the interrupt request flags are "1" & MIE flag is "0" (Refer to Section 4.2.2 - 4.2.3. in the user's manual).

[ ] Place two NOP instructions next to the instruction that sets the STP bit to "1" (Refer to Section 4.3.3. in the user's manual).

•HALT mode

[ ] Place two NOP instructions next to the instruction that sets the HLT bit to "1" (Refer to Section 4.3.2. in the user's manual).

•BLKCON register

[ ] BLKCON registers enable or disable corresponsive each peripheral (Refer to Section 4.2.4 - 4.2.7. in the user's manual).

[ ] When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop.

Chapter 5 Interrupts(INTs)

•Unused interrupt vector table

[ ] Please define all unused interrupt vector tables for fail safe.

•Non-maskable interrupt

[ ] The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that does not depend on MIE flag (Refer to Sections 5.2.10. and 5.3 in the User's Manual).

Chapter 6 Clock Generation Circuit

• Initial System clock

[ ] At power up or system reset, the RC32.768kHz oscillation clock oscillates and 32.768kHz clock is supplied to CPU as the system clock.

• Switching from high-speed clock to low-speed clock

[ ] When switching from high-speed clock to low-speed clock after return from the STOP mode, check that the time-base counter interrupt request bit (Q128H) is "1" and confirm that the LSCLK is oscillating.

• Port secondary function setting

[ ] Specify the secondary function for the port 2 when driving a clock to the pin (Refer to Section 6.4 in the user's manual).

Chapter 7 Time Base Counter

• HTBCLK

[ ] When using the HTBCLK for a timer, set an arbitrary dividing ratio in the high-speed side time base counter frequency divide register (HTBDR register) (see Section 7.2.3. in the User's Manual).

• How to read LTBC

[ ] Read consecutively LTBC(Low-speed Time Base Counter) twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock (Refer to Section 7.3.1 in the user's manual).

Chapter 8 Timer

• How to read the timer counter registers

[ ] Check notes for reading the timer counter registers while counting up (Refer to Sections 8.2.8 to 8.2.13 in the user's manual).

Chapter 9 Watchdog Timer

• Overflow period

Clear WDT during the selected overflow period:

[ ] 125ms, [ ] 500ms, [ ] 2s, [ ] 8s

• WDP

[ ] Check the WDP content before writing to the WDTCON register, then determine writing whether "5AH" or "0A5H" (Refer to Section 9.2.2. in the user's manual).

Chapter 10 PWM

• Output pins used

[ ] PA0 pin, PB0 pin or PB7 pin is used.

• Input pins used

[ ] PA0 pin, PA1 pin, PA2 pin, PB0 pin, PB1 pin, PB2 pin, PB3 pin, PB4 pin, PB5 pin, PB6 pin, PB7 pin, TM9INT,TMBINT or TMFINT is used.

• How to read the registers

[ ] Check notes for reading the timer counter registers while counting up (Refer to Sections 10.2.4 in the user's manual).

• Port secondary and fourthly function setting

[ ] Specify the secondary or fourthly function for the port (Refer to Section 10.4 in the user's manual).

Chapter 11 UART

• Pins used

[ ] PB0(RXD0) or PB5(RXD0) is used.

[ ] PB1(TXD0) or PB4(TXD0) is used.

[ ] Select PB0 or PB5 with the U0RSEL bit (UA0MOD0 register).

• Port secondary and tertiary function setting

[ ] Specify the secondary or tertiary function for the port (Refer to Section 12.4 in the user's manual).

Chapters 12 to 13 Port

• Handling pins

[ ] Don't leave Hi-impedance Input ports and Input/Output ports in floating state.

• Port secondary function setting

[ ] Specify properly PnCON0/1 and PnMOD0/1 registers for each port.

Chapters 14 Port AB interrupt control circuit

[ ] In STOP mode, the sampling option is not available regardless the setting of PB1SM ~ PA0SM as the 16kHz sampling clock stops.

Chapter 15 Successive Approximation Type A/D Converter

• Operating Conditions

[ ] Please confirm voltage of operation and a clock frequency.
VDD=2.7V-5.5V

[ ] Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).

[ ] Do not start A/D conversion with all of bits SACHB to SACH0 of the SA-ADC mode register 0 (SADMOD0) and the SA-ADC mode register 1 (SADMOD1) set to "0" (Please refer to clause 28.2.35 to 28.2.37 in the user's manual).

Chapter 16 Voltage Level detect Supervisor (VLS)

[ ] Set the VLSMOD register 1ms or more after the ENVLS1/ENVLS0 bit is set to "1".

Chapter 17 Analog Comparator

[ ] In STOP mode, since the sampling clock stops, no sampling is performed regardless of the values set in CMP0SM1/0.

[ ] When the sampling (T256KHZ, T128KHZ) is selected, PLL must be operated..

Chapter 18 On-Chip Debug Function

[ ] Supply a voltage from 4.5V to 5.5V to the VDD pin when programming (erasing and writing) the Flash ROM with μEASE.

[ ] Please do not apply LSI being used for debugging to mass production.

[ ] Please validate the ROM code on your production board without μEASE.

[ ] When using the on-chip debug function or the flash rewrite function after mounting of the board, design the board so that the 5 pins (VPP, VDD, VSS, RESET_N, TEST) required for connection to the on-chip debug emulator can be connected.

[ ] When the system reset circuit is included in the user application circuit, enable switching of the connection in the user application circuit. When the system reset circuit is not included in the user application circuit, the RESET_N pin can be connected directly to the RESET_N pin of this LSI.

[ ] Make capacitance between RSET_N pin and Vss pin 100pF or lower including parasitic capacitance, otherwise the on-chip debug communication may have errors.

[ ] Please start a debugger after canceling stop mode.

Appendix A SFR (Specific Function Registers)

• Initial value

[ ] Please confirm there are some SFRs have undefined initial value at reset (Refer to Appendix A in the user's manual).

Appendix C Electrical Characteristics

• External capacitors for Power circuits

[ ] Cv = 1uF (for VDD pin)

• Operating voltage

[ ] 2.7V to 5.5V

• Operating temperature

[ ] -40'C to +85'C

Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL610Q101-01	Dec. 3, 2012	–	–	Formal edition 1.0
FEUL610Q101-02	Jul. 1 2015	-	-	Change template
		-	1-3	Add 16 pin WQFN
		-	1-7	Add the WQFN16 pin layout
		1-8	1-8	Add list of pins of the WQFN.
		1-8	1-8	Correct erroneous description about PA0,PA1. "I" to "I/O"
		15-9	15-9	Remove the description of conversion time
		-	18-1	Add the following description. "When μEASE connecting, please do not connect the capacity of more than 100 pF of parasitic capacitance inclusion between the RESET_N pin and the VSS pin. A communication error can't bring and normally debug a program anymore."
		C-8	C-8	Correct erroneous description. "ϕ: f_{PLL}/4" to "ϕ: f_{PLL}/2"
		16-4	16-4	Correct erroneous description about VLS0ST. "When ENVLS0 is "0", VLS0ST is fixed to"1"." to "When ENVLS0 is "0", VLS0ST is fixed to"0"."
		16-4	16-4	Correct erroneous description about VLS0ST. 1: Higher than the threshold voltage 0: Lower than the threshold voltage to 0: Higher than the threshold voltage 1: Lower than the threshold voltage
		16-4	16-4	Correct erroneous description about VLS1ST. "When ENVLS0 is "0", VLS1ST is fixed to"1"." to "When ENVLS0 is "0", VLS1ST is fixed to"0"."
		16-4	16-4	Correct erroneous description about VLS1ST. 1: Higher than the threshold voltage 0: Lower than the threshold voltage to 0: Higher than the threshold voltage 1: Lower than the threshold voltage
		-	17-4	Add the following description. If VSL0 or VLS1(Voltage Level Supervisor0 or 1) is stopped in STOP mode, the internal reference voltage source in the comparator is also stopped. Set SFRs(Specific Function Registers) so that the VSL0 or VSL1 can work in STOP mode when using the CMP0(Comparator 0) in the STOP mode. Set ENVLS0 bit or ENVLS1 bit of VLSCON1 register to "1" and set DVLSSP bit of VLSCON0 register. For more details about VLS, see Chapter 16, "Voltage Level Supervisor".

		-	17-8	Add the following description. If VSL0 or VLS1(Voltage Level Supervisor0 or 1) is stopped in STOP mode, the internal reference voltage source in the comparator is also stopped. Set SFRs(Specific Function Registers) so that the VSL0 or VSL1 can work in STOP mode when using the CMP1(Comparator 1) in the STOP mode. Set ENVLS0 bit or ENVLS1 bit of VLSCON1 register to "1" and set DVLSSP bit of VLSCON0 register. For more details about VLS, see Chapter 16, "Voltage Level Supervisor".
		-	C-2	Add the following items. “Power-on reset activation power rise slope”
		-	C-8	Add the following items. “Allowable signal source impedance”
			D-1,2,3	Add CheckList