



# MICROCHIP PIC12(L)F1501/PIC16(L)F150X

## 8/14/20-Pin, 8-Bit Flash Microcontrollers Product Brief

### High-Performance RISC CPU:

- C Compiler Optimized Architecture
- Only 49 Instructions
- Up to 14 Kbytes Linear Program Memory Addressing
- Up to 512 bytes Linear Data Memory Addressing
- Operating Speed:
  - DC – 20 MHz clock input
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

### Flexible Oscillator Structure:

- 16 MHz Internal Oscillator Block:
  - Factory calibrated to  $\pm 1\%$ , typical
  - Software selectable frequency range from 16 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- Three External Clock modes up to 20 MHz

### Special Microcontroller Features:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC12LF1501/PIC16LF150X)
  - 2.3V to 5.5V (PIC12F1501/PIC16F150X)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Programmable Low-Power Brown-Out Reset (LPBOR)
- Extended Watchdog Timer (WDT):
  - Programmable period from 1 ms to 256s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Power-Saving Sleep mode:
  - Low-Power Sleep mode
  - Low-Power BOR (LPBOR)
- Integrated Temperature Indicator

### Low-Power Features

#### (PIC12LF1501/PIC16LF150X):

- Standby Current:
  - 20 nA @ 1.8V, typical
- Watchdog Timer Current:
  - 300 nA @ 1.8V, typical
- Operating Current:
  - 30  $\mu$ A/MHz @ 1.8V, typical
- Timer1 Oscillator:
  - 600 nA @ 32 kHz, 1.8V, typical (PIC16LF1508/09 devices only)

### Peripheral Features:

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 12 external channels
  - 2 internal channels:
    - Fixed Voltage Reference channel
    - Temperature Indicator channel
  - Auto acquisition capability
  - Conversion available during Sleep
- Up to 2 Comparators:
  - Rail-to-rail inputs
  - Power mode control
  - Software controllable hysteresis
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - Up to 1 rail-to-rail resistive 5-bit DAC with positive and negative reference selection
- Up to 17 I/O Pins and 1 Input-only Pin:
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-change (IOC) pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Four 10-bit PWM modules
- Up to 1 Master Synchronous Serial Port (MSSP) with SPI and I<sup>2</sup>C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Up to 1 Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible

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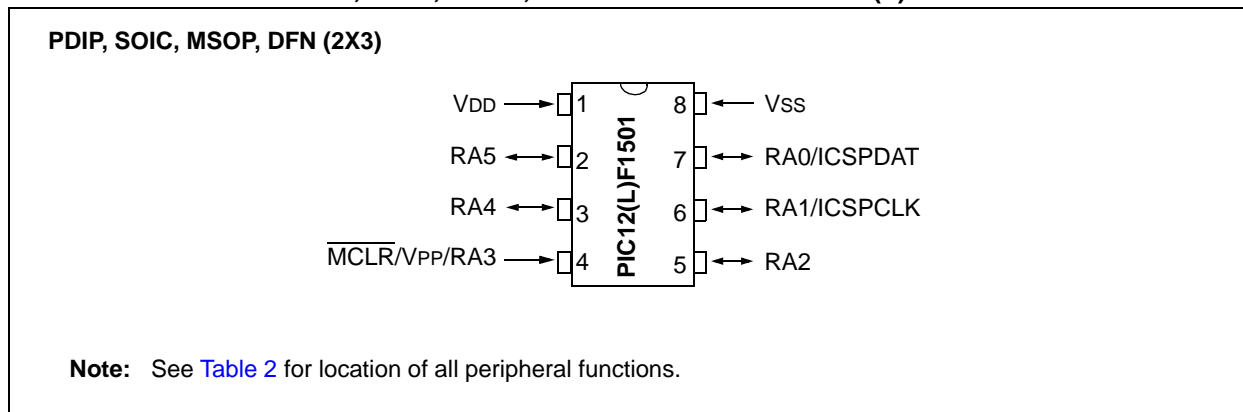
- Auto-baud detect
- Auto-wake-up on Start
- Up to 4 Configurable Logic Cell (CLC) modules:
  - Up to 16 selectable input source signals
  - Four inputs per module
  - Software control of combinational/sequential logic/state/clock functions
  - AND/OR/XOR/D Flop/D Latch/SR/JK
  - External or internal inputs/outputs
  - Operation while in Sleep
- Numerically Controlled Oscillator (NCO):
  - 20-bit accumulator
  - 16-bit increment
  - True linear frequency control
  - High-speed clock input
  - Selectable Output modes
    - Fixed Duty Cycle (FDC)
    - Pulse Frequency Modulation (PFM)
- Complementary Waveform Generator (CWG):
  - Up to 8 selectable signal sources
  - Selectable falling and rising edge dead-band control
  - Polarity control
  - Up to 4 auto-shutdown sources
  - Multiple input sources: PWM, CLC, NCO

**TABLE 1: PIC12(L)F1501/PIC16(L)F150X FAMILY TYPES**

Device	Program Memory Flash (words)	SRAM (bytes)	I/Os	10-bit A/D (ch)	Comparators	DAC	Timers 8/16-bit	PWM	EUSART	MSSP	CWG	CLC	NCO	ICD	XLP
PIC12F1501 PIC12LF1501	1024	64	6	4	1	1	2/1	4	—	—	1	2	1	—	—
PIC16F1503 PIC16LF1503	2048	128	12	8	2	1	2/1	4	—	1	1	2	1	—	—
PIC16F1507 PIC16LF1507	2048	128	18	12	—	—	2/1	4	—	—	1	2	1	—	—
PIC16F1508 PIC16LF1508	4096	256	18	12	2	1	2/1	4	1	1	1	4	1	V3	X
PIC16F1509 PIC16LF1509	8192	512	18	12	2	1	2/1	4	1	1	1	4	1	V3	X

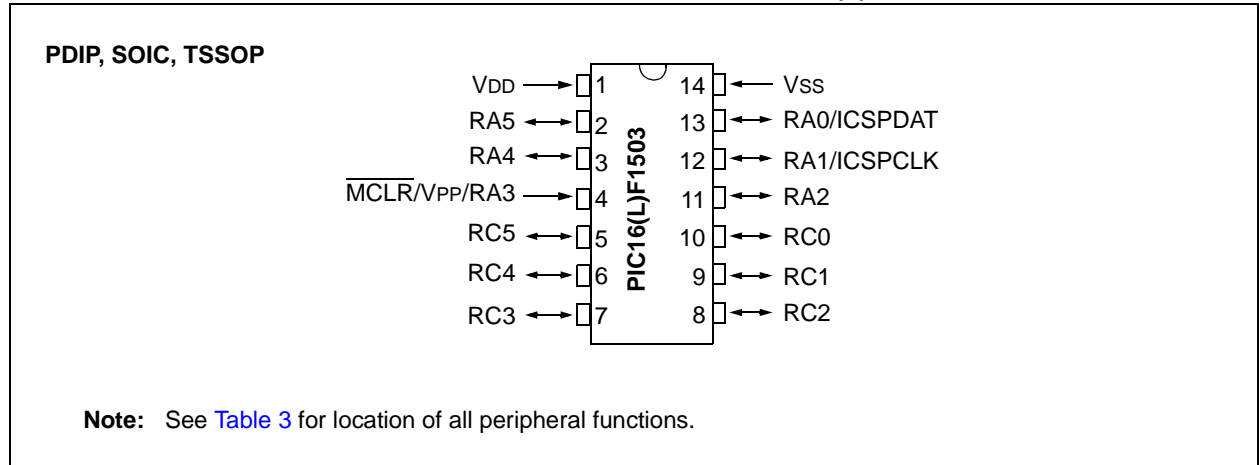
**Note:** Pin details are subject to change.

**FIGURE 1: 8-PIN PDIP, SOIC, MSOP, DFN DIAGRAM FOR PIC12(L)F1501**

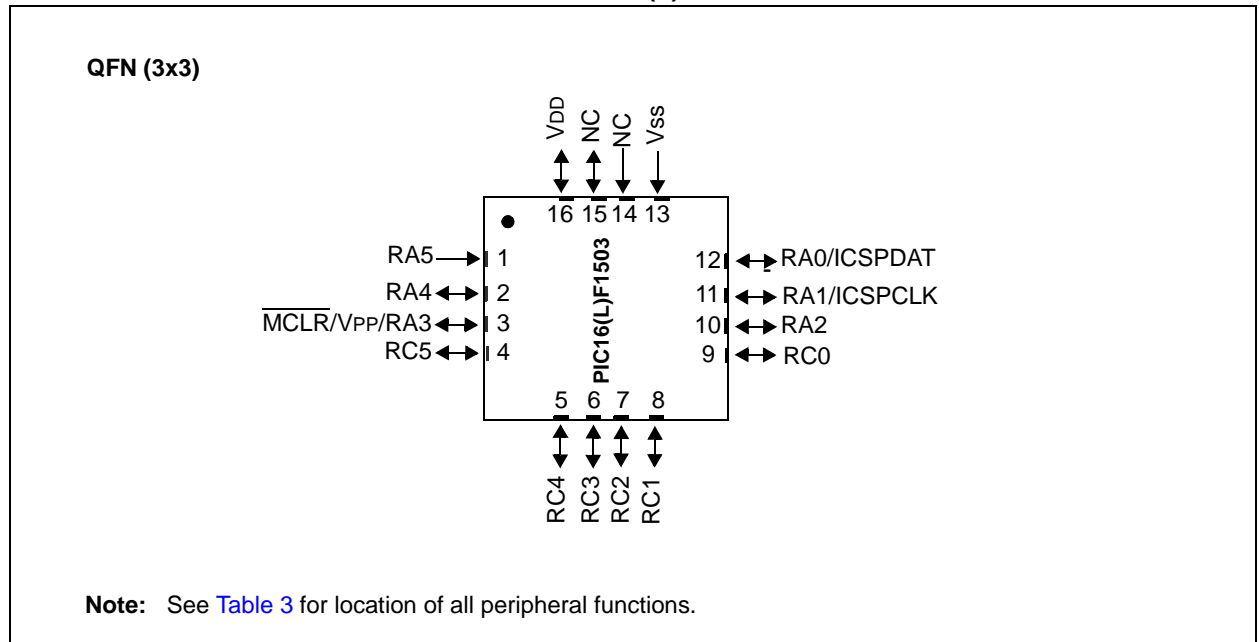


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**FIGURE 2: 14-PIN PDIP, SOIC, TSSOP DIAGRAM FOR PIC16(L)F1503**

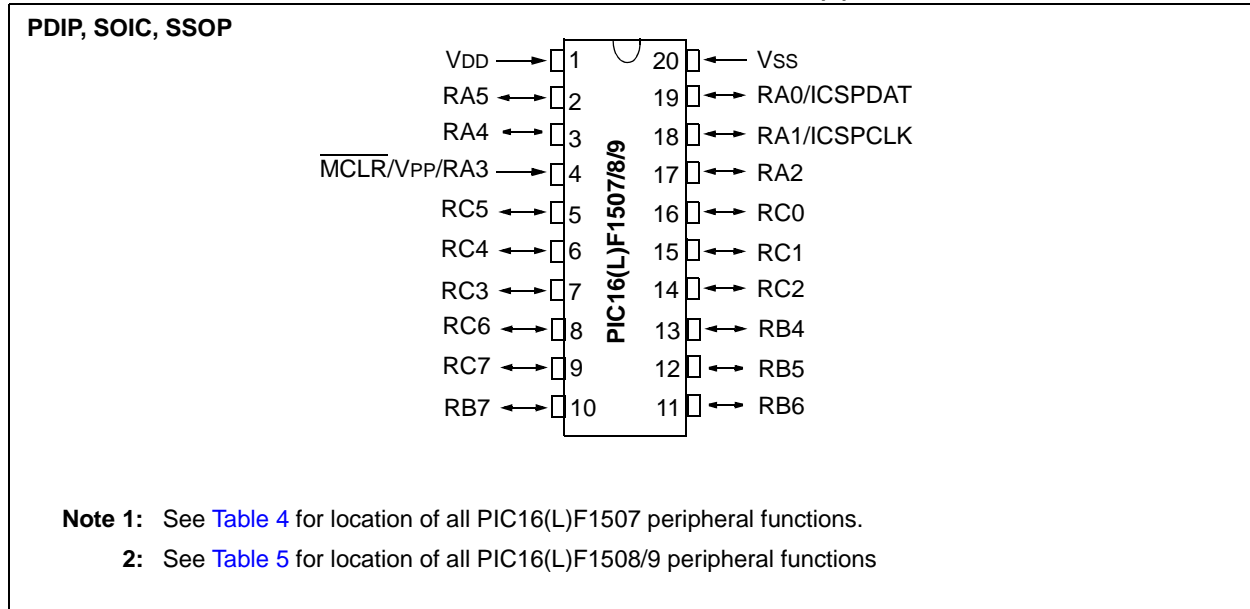


**FIGURE 3: 16-PIN QFN DIAGRAM FOR PIC16(L)F1503**

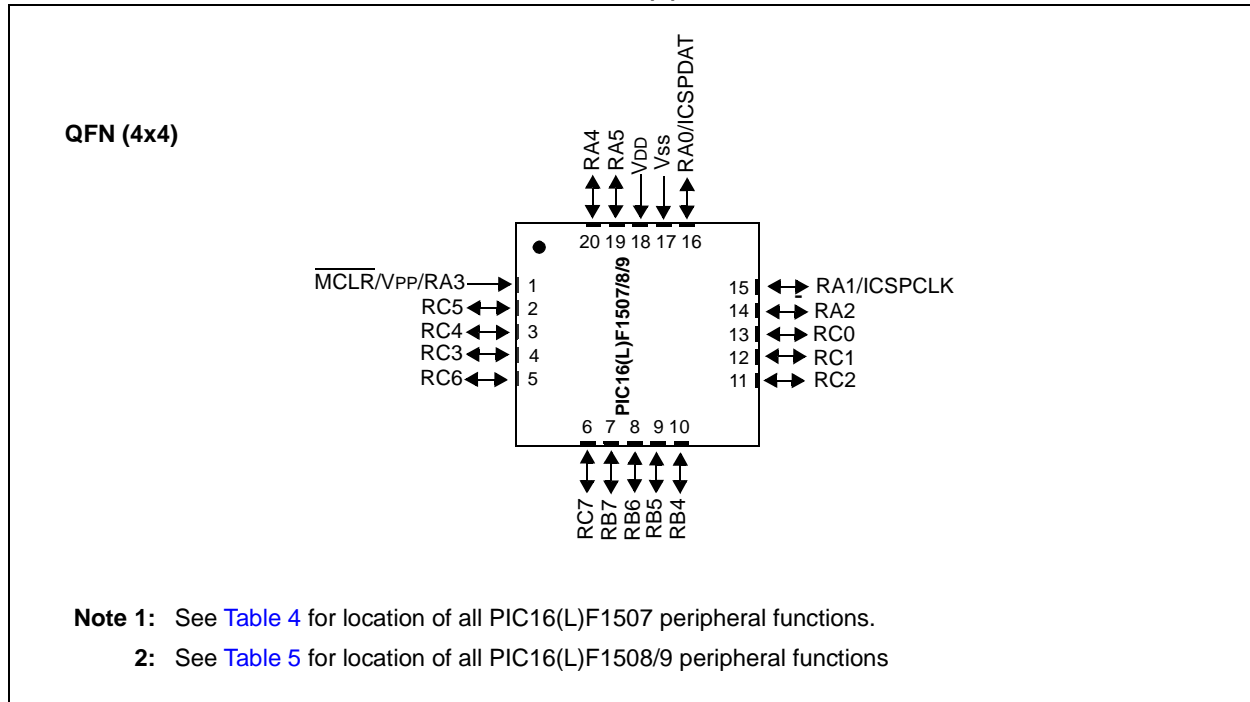


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**FIGURE 4: 20-PIN PDIP, SOIC, SSOP DIAGRAM FOR PIC16(L)F1507/8/9**



**FIGURE 5: 20-PIN QFN DIAGRAM FOR PIC16(L)F1507/8/9**



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**TABLE 2: 8-PIN ALLOCATION TABLE (PIC12(L)F1501)**

I/O	8-Pin PDIP/SOIC/MSOP/DFN	ADC	Reference	Comparator	Timer	CWG	NCO	CLC	PWM	Interrupt	Basic
RA0	7	AN0	DACOUT1	C1IN+	—	CWGB <sup>(1)</sup>	—	CLC2IN1	PWM2	IOC	ICSPDAT
RA1	6	AN1	VREF+	C1IN0-	—	—	NCOOUT <sup>(1)</sup>	CLC2IN0	—	IOC	ICSPCLK
RA2	5	AN2	DACOUT2	C1OUT	T0CKI	CWGA <sup>(1)</sup> CWGFLT	—	CLC1OUT <sup>(1)</sup>	PWM1	INT IOC	—
RA3	4	—	—	—	T1G <sup>(2)</sup>	—	—	CLC1IN0	—	IOC	$\overline{\text{MCLR}}$ V <sub>PP</sub>
RA4	3	AN3	—	C1IN1-	T1G <sup>(1)</sup>	CWGB <sup>(2)</sup>	—	CLC1OUT <sup>(2)</sup>	PWM3	IOC	CLKOUT
RA5	2	—	—	—	T1CKI	CWGA <sup>(2)</sup>	NCOCLK NCOOUT <sup>(2)</sup>	CLC2OUT CLC1IN1	PWM4	IOC	CLKIN
VDD	1	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	VSS

**Note 1:** Default location for peripheral pin function. Alternate location can be selected using the APFCON register.

**Note 2:** Alternate location for peripheral pin function selected by the APFCON register.

**TABLE 3: 14-PIN ALLOCATION TABLE (PIC16(L)F1503)**

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	ADC	Reference	Comparator	Timer	CWG	NCO	CLC	PWM	MSSP	Interrupt	Basic
RA0	13	12	AN0	DACOUT1	C1IN+	—	—	—	—	—	—	IOC	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	IOC	ICSPCLK
RA2	11	10	AN2	DACOUT2	C1OUT	T0CKI	$\overline{\text{CWGFLT}}$	—	CLC1OUT <sup>(1)</sup>	PWM3	—	INT IOC	—
RA3	4	3	—	—	—	T1G <sup>(2)</sup>	—	—	CLC1IN0	—	$\overline{\text{SS}}$ <sup>(2)</sup>	IOC	$\overline{\text{MCLR}}$ V <sub>PP</sub>
RA4	3	2	AN3	—	—	T1G <sup>(1)</sup>	—	NCOOUT <sup>(2)</sup>	—	—	SDO <sup>(2)</sup>	IOC	CLKOUT
RA5	2	1	—	—	—	T1CKI	—	NCOCLK	CLC1IN1	—	—	IOC	CLKIN
RC0	10	9	AN4	—	C2IN+	—	—	—	CLC2OUT	—	SCL SCK	—	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	—	—	NCOOUT <sup>(1)</sup>	—	PWM4	SDA SDI	—	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	—	—	—	—	—	SDO <sup>(1)</sup>	—	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	—	—	—	CLC2IN0	PWM2	$\overline{\text{SS}}$ <sup>(1)</sup>	—	—
RC4	6	5	—	—	C2OUT	—	CWGB	—	CLC2IN1	—	—	—	—
RC5	5	4	—	—	—	—	CWGA	—	CLC1OUT <sup>(2)</sup>	PWM1	—	—	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	VSS

**Note 1:** Default location for peripheral pin function. Alternate location can be selected using the APFCON register.

**Note 2:** Alternate location for peripheral pin function selected by the APFCON register.

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TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1507)

I/O	20-Pin PDIP/SSOP	20-Pin QFN	ADC	Reference	Timer	CWG	NCO	CLC	PWM	Interrupt	Basic
RA0	19	16	AN0	—	—	—	—	—	—	IOC	ICSPDAT
RA1	18	15	AN1	VREF+	—	—	—	—	—	IOC	ICSPCLK
RA2	17	14	AN2	—	T0CKI	CWGFLT	—	CLC1OUT <sup>(1)</sup>	PWM3	INT IOC	—
RA3	4	1	—	—	—	—	—	CLC1IN0	—	IOC	MCLR V <sub>PP</sub>
RA4	3	20	AN3	—	T1G	—	—	—	—	IOC	CLKOUT
RA5	2	19	—	—	T1CKI	—	NCOCLK	—	—	IOC	CLKIN
RB4	13	10	AN10	—	—	—	—	—	—	IOC	—
RB5	12	9	AN11	—	—	—	—	—	—	IOC	—
RB6	11	8	—	—	—	—	—	—	—	IOC	—
RB7	10	7	—	—	—	—	—	—	—	IOC	—
RC0	16	13	AN4	—	—	—	—	CLC2OUT	—	—	—
RC1	15	12	AN5	—	—	—	NCOOUT <sup>(1)</sup>	—	PWM4	—	—
RC2	14	11	AN6	—	—	—	—	—	—	—	—
RC3	7	4	AN7	—	—	—	—	CLC2IN0	PWM2	—	—
RC4	6	3	—	—	—	CWGB	—	CLC2IN1	—	—	—
RC5	5	2	—	—	—	CWGA	—	CLC1OUT <sup>(2)</sup>	PWM1	—	—
RC6	8	5	AN8	—	—	—	NCOOUT <sup>(2)</sup>	—	—	—	—
RC7	9	6	AN9	—	—	—	—	CLC1IN1	—	—	—
VDD	1	18	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	VSS

**Note 1:** Default location for peripheral pin function. Alternate location can be selected using the APFCON register.

**2:** Alternate location for peripheral pin function selected by the APFCON register.

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**TABLE 5: 20-PIN ALLOCATION TABLE (PIC16(L)F1508/9)**

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	Comparator	Timer	CWG	NCO	CLC	PWM	EUSART	MSSP	Interrupt	Basic
RA0	19	16	AN0	DACOUT1	C1IN+	—	—	—	—	—	—	—	IOC	ICSPDAT ICDDAT
RA1	18	15	AN1	VREF+	C1IN0- C2IN0-	—	—	—	CLC4IN1	—	—	—	IOC	ICSPCLK ICDCLK
RA2	17	14	AN2	DACOUT2	C1OUT	T0CKI	CWGFLT	—	CLC1OUT <sup>(1)</sup>	PWM3	—	—	INT IOC	—
RA3	4	1	—	—	—	T1G <sup>(2)</sup>	—	—	CLC1IN0	—	—	SS <sup>(2)</sup>	IOC	MCLR VPP
RA4	3	20	AN3	—	—	T1OSCO T1G <sup>(1)</sup>	—	—	—	—	—	—	IOC	OSC2 CLKOUT
RA5	2	19	—	—	—	T1OSCI T1CKI	—	NCOCLK	—	—	—	—	IOC	OSC1 CLKIN
RB4	13	10	AN10	—	—	—	—	—	CLC3IN0	—	—	SDA SDI	IOC	—
RB5	12	9	AN11	—	—	—	—	—	CLC4IN0	—	RX DX	—	IOC	—
RB6	11	8	—	—	—	—	—	—	—	—	—	SCL SCK	IOC	—
RB7	10	7	—	—	—	—	—	—	CLC3OUT	—	TX CK	—	IOC	—
RC0	16	13	AN4	—	C2IN+	—	—	—	CLC2OUT	—	—	—	—	—
RC1	15	12	AN5	—	C1IN1- C2IN1-	—	—	NCOOUT <sup>(1)</sup>	—	PWM4	—	—	—	—
RC2	14	11	AN6	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—
RC3	7	4	AN7	—	C1IN3- C2IN3-	—	—	—	CLC2IN0	PWM2	—	—	—	—
RC4	6	3	—	—	C2OUT	—	CWGB	—	CLC4OUT CLC2IN1	—	—	—	—	—
RC5	5	2	—	—	—	—	CWGA	—	CLC1OUT <sup>(2)</sup>	PWM1	—	—	—	—
RC6	8	5	AN8	—	—	—	—	NCOOUT <sup>(2)</sup>	CLC3IN1	—	—	SS <sup>(1)</sup>	—	—
RC7	9	6	AN9	—	—	—	—	—	CLC1IN1	—	—	SDO	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	VSS

**Note** 1: Default location for peripheral pin function. Alternate location can be selected using the APFCON register.  
 2: Alternate location for peripheral pin function selected by the APFCON register.

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NOTES:



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