AP133

300mA, LOW QUIESCENT CURRENT, FAST TRANSIENT LOW DROPOUT LINEAR REGULATOR

Features

- 300mA Low Dropout Regulator with EN
- Very low I_Q: 40µA
- Wide input voltage range: 2V – 6V
- Adjustable output: 1V – 5V
- High PSRR: 65dB at 1kHz
- Ultra-fast start-up time: 25µs
- Stable with low ESR, 1µF ceramic output capacitor
- Excellent Load/Line Transient Response
- Low dropout: 350mV at 300mA
- Current limit protection
- Short circuit protection
- Thermal shutdown protection
- Ambient temperature range: -40ºC to 85°C
- SOT25 and DFN2020-6: Available in “Green” Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)

Description

The AP133 is a 300mA, adjustable output voltage, low dropout linear regulator. The device includes pass element, error amplifier, band-gap, current limit and thermal shutdown circuitry. The device is turned on when EN pin is set to logic high level.

The characteristics of low dropout voltage and less quiescent current make it good for low power applications, for example, battery powered devices. The typical quiescent current is approximately 40µA from zero to maximum load.

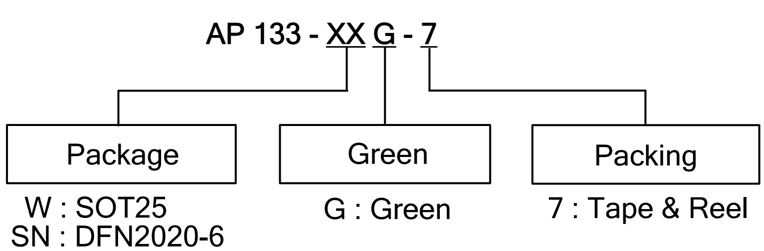
Built-in current-limit and thermal-shutdown functions prevent IC from damage in fault conditions.

The AP133 is available in SOT25 and DFN2020-6 packages.

Applications

- Cellular Phones
- Smart Phones, PDAs
- MP3/MP4
- Bluetooth head set
- Low power application

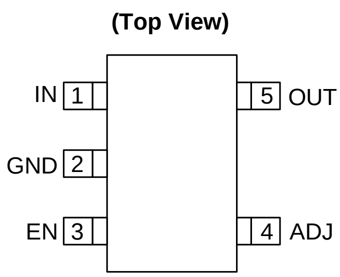
Ordering Information



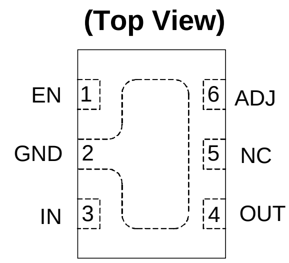
Device	Package Code	Packaging (Note 2)	7” Tape and Reel	
			Quantity	Part Number Suffix
AP133-WG-7	W	SOT25	3000/Tape & Reel	-7
AP133-SNG-7	SN	DFN2020-6	3000/Tape & Reel	-7

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.
2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Pin Assignment



SOT25

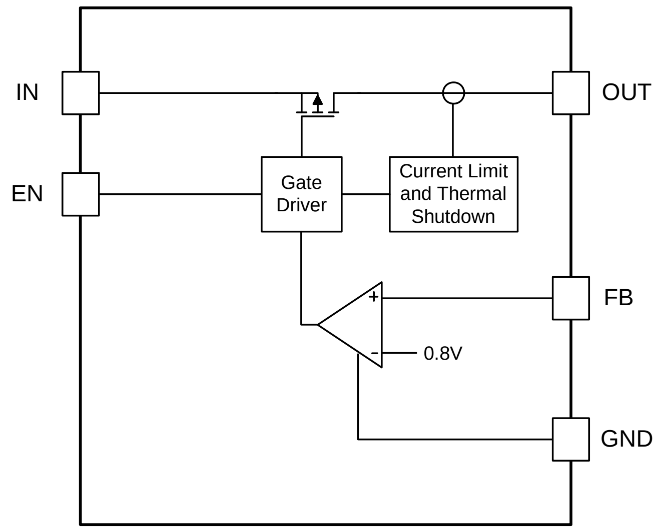


DFN2020-6

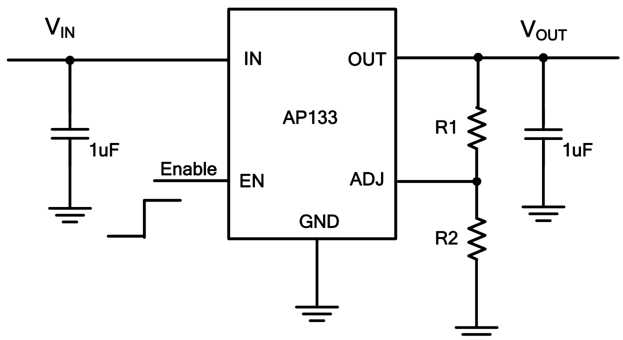
Pin Descriptions

Pin Name	Pin Number		Description
	SOT25	DFN2020-6	
IN	1	3	Voltage input pin. Bypass to ground through at least 0.1µF capacitor
GND	2	2	Ground
EN	3	1	Enable input, active high
ADJ	4	6	Output feedback pin
NC		5	No connection
OUT	5	4	Voltage output pin. Bypass to ground through 1µF ceramic capacitor

Functional Block Diagram



Typical Application Circuit



$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

Absolute Maximum Ratings

Symbol	Parameter		Ratings	Unit
V_{IN}	Input Voltage		7	V
	OUT, ADJ, EN Voltage		V_{IN} + 0.3	V
	Continuous Load Current		Internal Limited	
T_{OP}	Operating Junction Temperature Range		-40 ~ 125	°C
T_{ST}	Storage Temperature Range		-65 ~150	°C
P_D	Power Dissipation (Note 3)	SOT25	740	mW
		DFN2020-6	900	mW
T_J	Maximum Junction Temperature		150	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input voltage (Note 4)	2	6	V
I_{OUT}	Output Current	0	300	mA
T_A	Operating Ambient Temperature	-40	85	°C

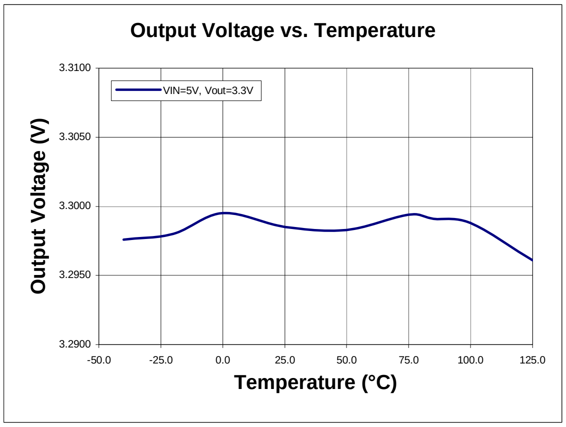
Notes: 3. Ratings apply to ambient temperature at 25°C
4. At V_{IN}< 2.2V and T_A< -20°C, the output current capability may be reduced.

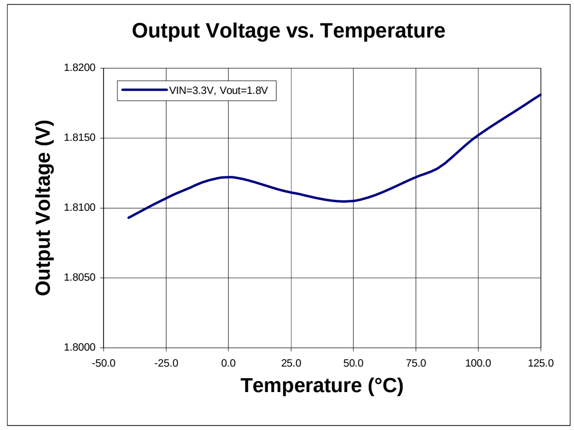
Electrical Characteristics

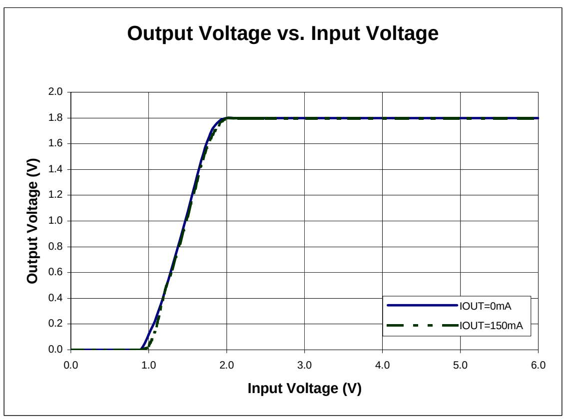
(T_A = 25°C, V_{IN} = V_{OUT} +1V, C_{IN} = 1uF, C_{OUT} = 1uF, V_{EN} = 2V, unless otherwise stated)

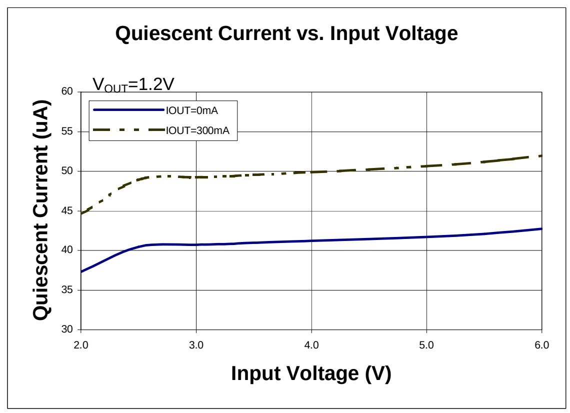
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_Q	Input Quiescent Current	I_{OUT} = 0~300mA	—	40	60	uA
I_{SHDN}	Input Shutdown Current	V_{EN} = 0V, I_{OUT} = 0	—		1	uA
I_{LEAK}	Input Leakage Current	V_{EN} = 0V, OUT grounded	—		1	uA
$V_{Dropout}$	Dropout Voltage	$V_{OUT} \geq$ 1.5V, I_{OUT} = 300mA		350	450	mV
V_{REF}	ADJ reference voltage	I_{OUT}= 0		0.8		V
I_{ADJ}	ADJ leakage		—		1	uA
V_{OUT}	Output Voltage Accuracy		-2		2	%
$\Delta V_{OUT} / \Delta V_{IN}/V$	Line Regulation	V_{IN} = V_{OUT} +1V to 5.5V, I_{OUT} = 1mA		0.05		%/V
$\Delta V_{OUT} / V_{OUT}$	Load Regulation	I_{OUT} from 1mA to 300mA	-1		1	%
t_{ST}	Start-up Time	V_{EN} = 0V to 2.0V, I_{OUT} = 300mA		25		us
PSRR	PSRR	1kHz, I_{OUT} = 0mA		65		dB
I_{SHORT}	Short-circuit Current	V_{IN} = 5.0V, V_{OUT} < 0.2V		120		mA
I_{LIMIT}	Current limit	V_{OUT} = 3V, R_{OUT} = 3Ω	400	600		mA
V_{IL}	EN Input Logic Low Voltage				0.4	V
V_{IH}	EN Input Logic High Voltage		1.4			V
I_{EN}	EN Input leakage	V_{EN} = 0V or 5.5V	-1		1	uA
T_{SHDN}	Thermal shutdown threshold			145		°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
θ_{JA}	Thermal Resistance Junction-to-Ambient — SOT25	Device mounted on FR-4 substrate, 2oz copper, with minimum recommended pad layout.		176		°C/W
	Thermal Resistance Junction-to-Ambient — DFN2020-6			142		
θ_{JC}	Thermal Resistance Junction-to-Case — SOT25			41		°C/W
	Thermal Resistance Junction-to-Case — DFN2020-6			36		

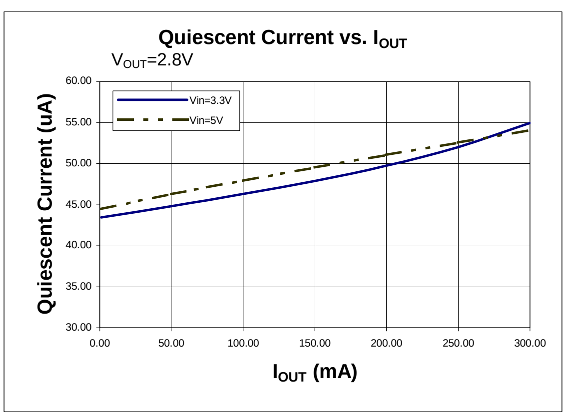
Typical Performance Characteristics

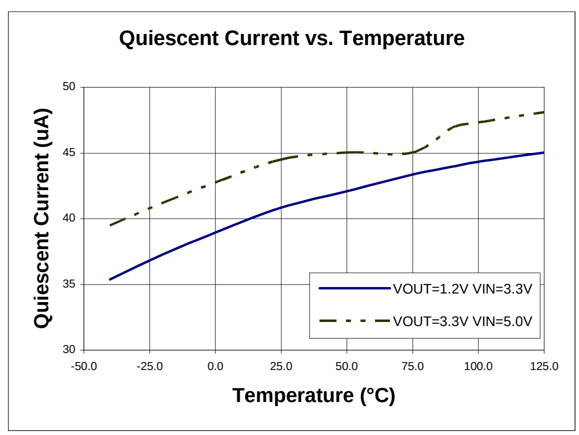




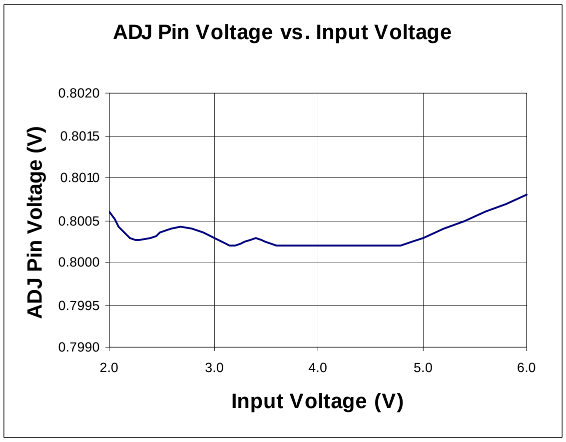


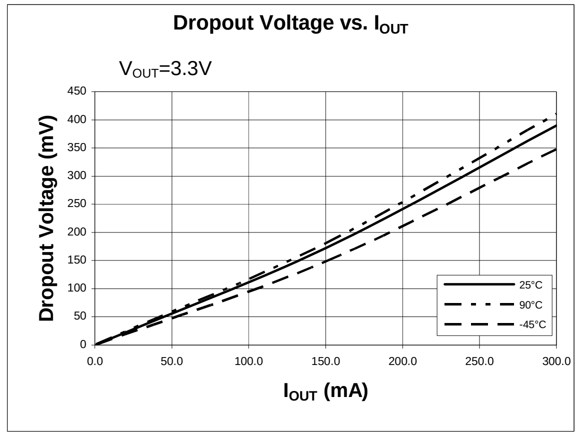




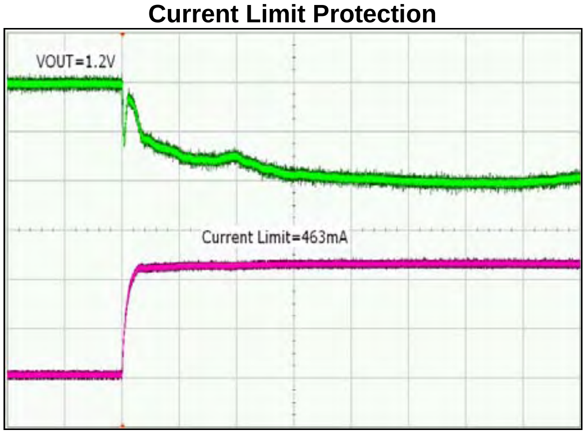


Typical Performance Characteristics (Continued)

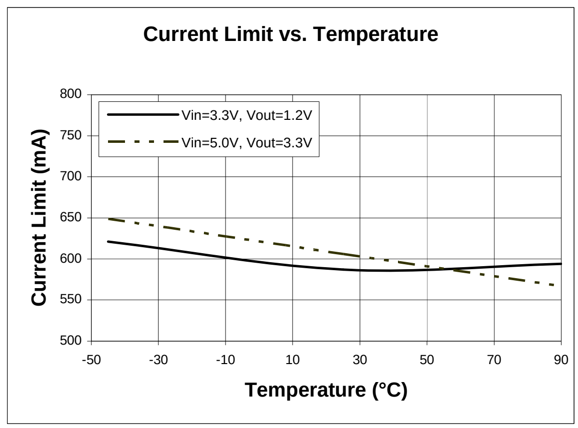




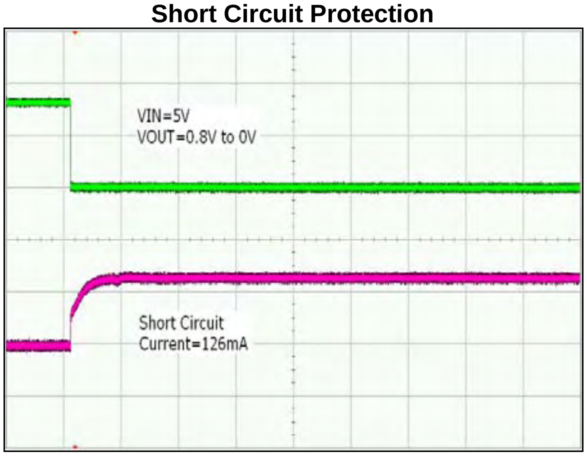
Current Limit Protection



Time (50us/div)

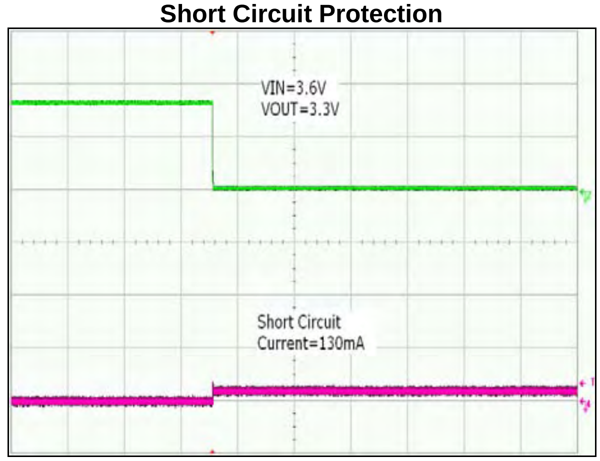


Short Circuit Protection



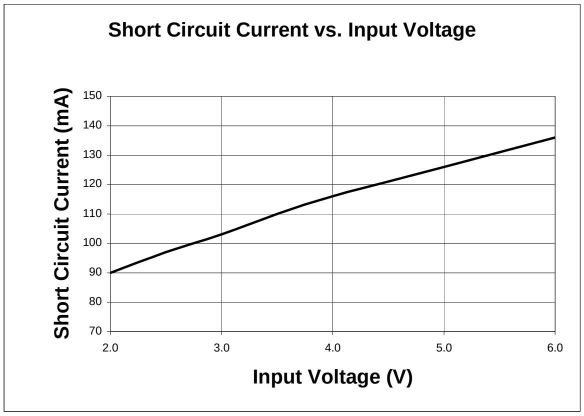
Time (1ms/div)

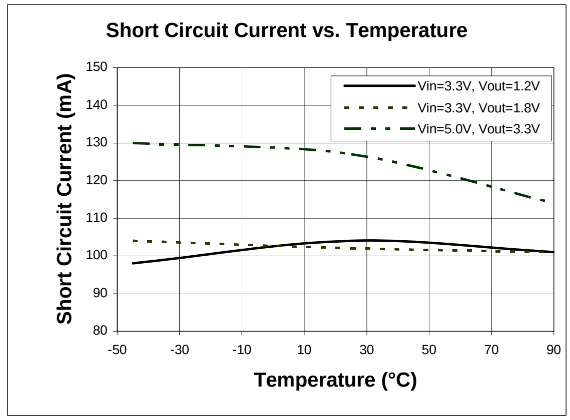
Short Circuit Protection



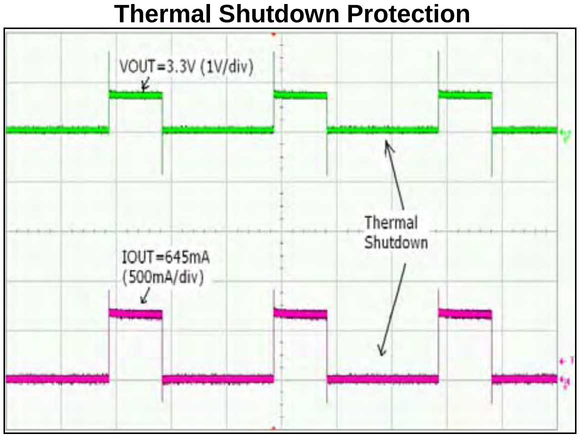
Time (2ms/div)

Typical Performance Characteristics (Continued)

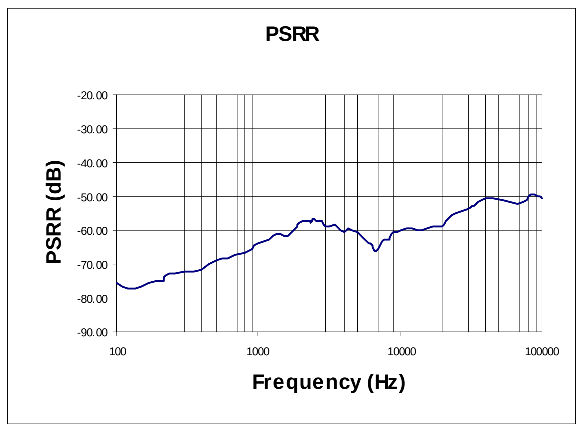




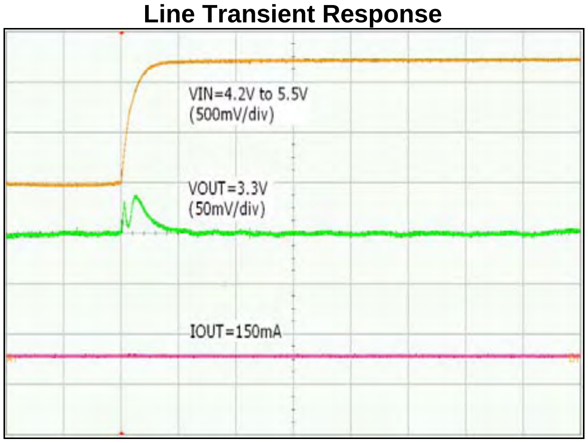
Thermal Shutdown Protection



Time (20ms/div)

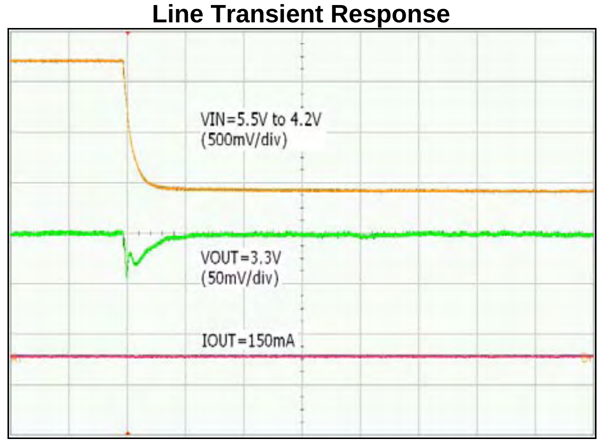


Line Transient Response



Time (20us/div)

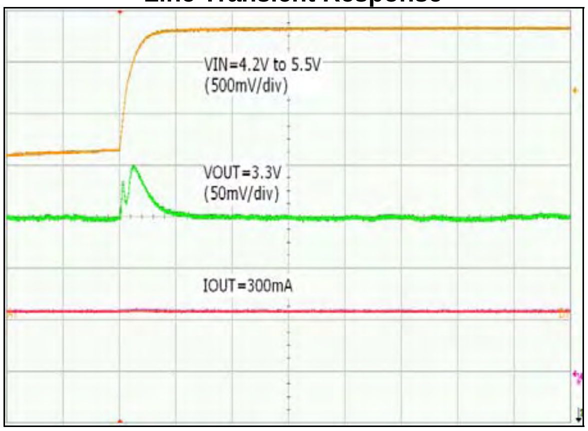
Line Transient Response



Time (20us/div)

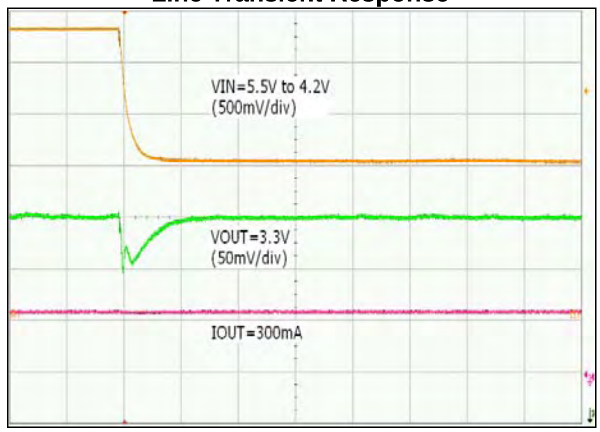
Typical Performance Characteristics (Continued)

Line Transient Response



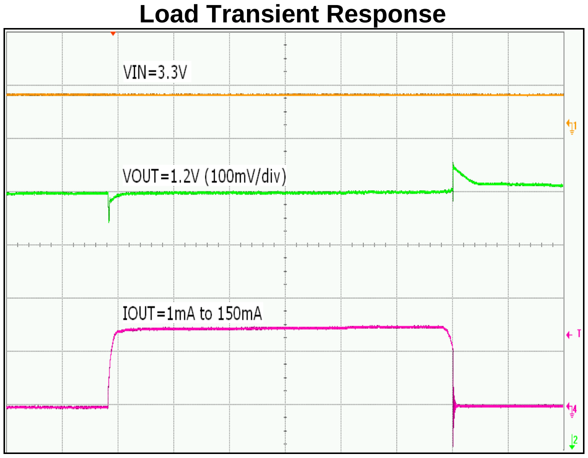
Time (20us/div)

Line Transient Response



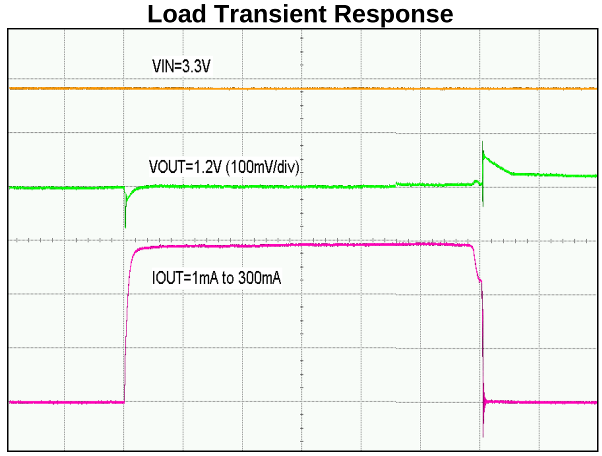
Time (20us/div)

Load Transient Response



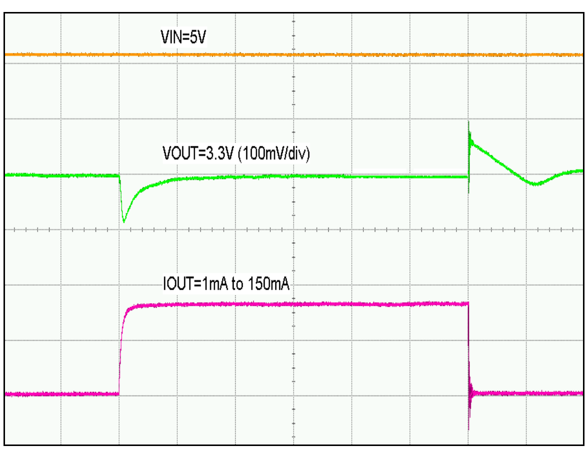
Time (100us/div)

Load Transient Response



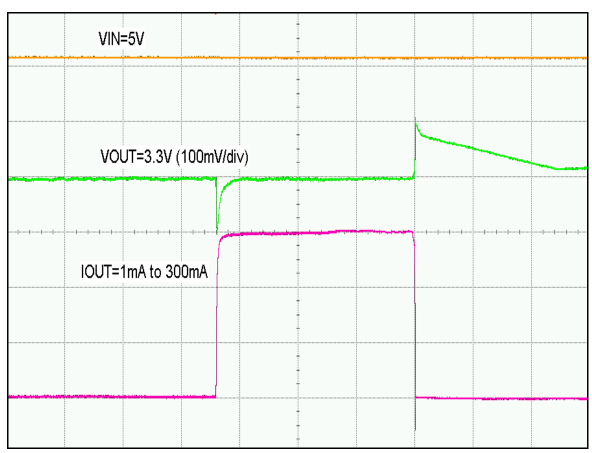
Time (100us/div)

Load Transient Response



Time (20us/div)

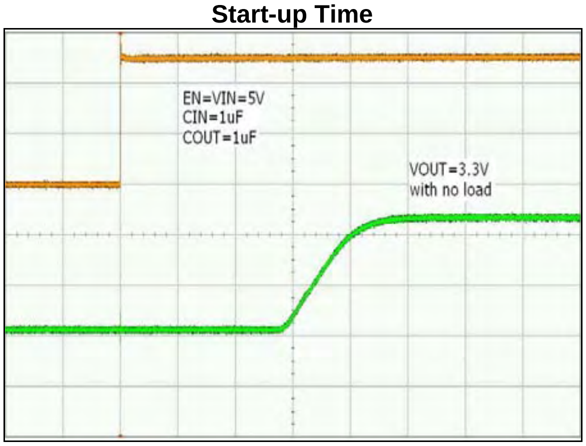
Load Transient Response



Time (100us/div)

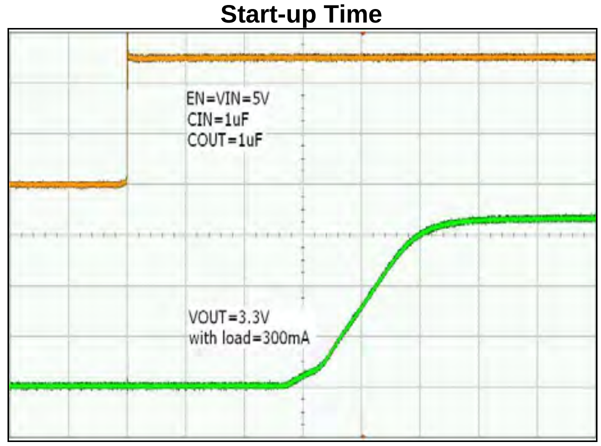
Typical Performance Characteristics (Continued)

Start-up Time



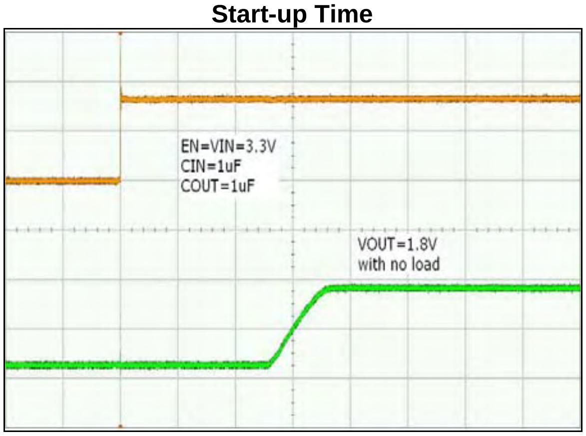
Time (5us/div)

Start-up Time



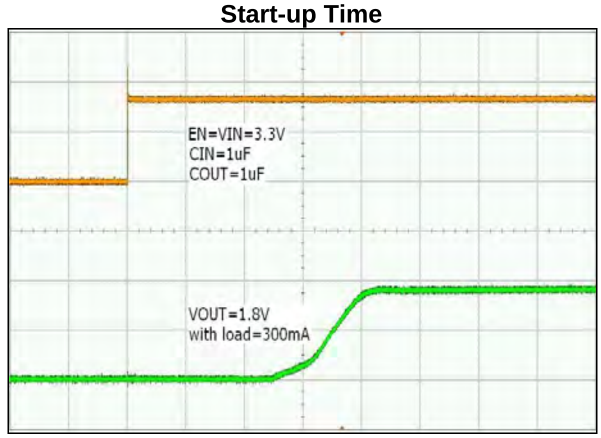
Time (5us/div)

Start-up Time



Time (5us/div)

Start-up Time



Time (5us/div)

Application Note

Input Capacitor

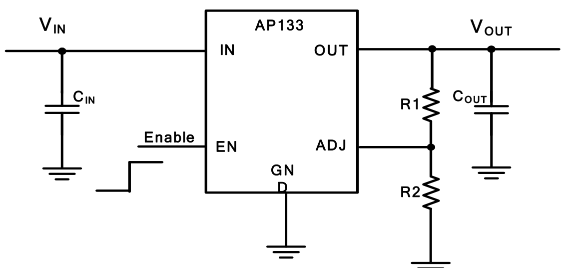
A1µF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND. A lower ESR capacitor allows the use of less capacitance, while higher ESR type require more capacitance.

Output Capacitor

The output capacitor is required to stabilize and help transient response for LDO. The AP133 is stable with very small ceramic output capacitors. The recommended capacitance is from 1µF to 4.7µF, Equivalent Series Resistance (ESR) is from 10mΩ to 100mΩ, and temperature characteristics is X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins, and keep the leads as short as possible.

Adjustable Operation

The AP133 provides output voltage from 1.0V to 5.0V through external resistor divider as shown below.



The output voltage is calculated by:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

Where V_{REF}=0.8V (the internal reference voltage)

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

To maintain the stability of the internal reference voltage, R_2 needs to be kept smaller than 250kΩ.

No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

ON/OFF Input Operation

The AP133 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Current Limit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 600mA to prevent over-current and to protect the regulator from damage due to overheating.

Short Circuit Protection

When OUT pin is short-circuit to GND or OUT pin voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 120mA. This feature protects the regulator from over-current and damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +145°C, allowing the device to cool down. When the junction temperature reduces to approximately +125°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Ultra Fast Start-up

After enabled, the AP133 is able to provide full power in as little as tens of microseconds, typically 25µs, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Fast Transient Response

Fast transient response LDOs can also extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100µA to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs.

The AP133's fast transient response from 0 to 300mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

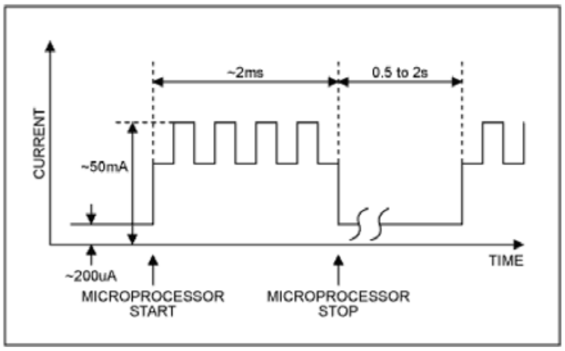
Small Overshoot and Undershoot

The AP133 has small and controlled overshoot and undershoot in load and line transitions. This helps to protect supplied circuit from damage and operation error caused by glitches. This feature also permits the usage of small value output decoupling capacitor with AP133.

Application Note

Low Quiescent Current

Cellular phone baseband internal digital circuits typically operate from 1.8V to 2.6V. When the Li+ battery voltage falls to 3.2-3.3V, most phones shut off, giving at least 500-600mV of headroom for the baseband digital LDO, so dropout is not critical. Output noise and the PSRR are not critical specs for the digital circuits. Nonetheless, this supply requires low quiescent current at light loads because this LDO stays on at all times. Figure below shows how the digital supply current of a representative GSM chipset core varies as a function of time.



In the standby mode, the microprocessor consumes only around 200µA. Since the phone stays in standby for the longest percentage of time, using a 40µA quiescent current LDO, instead of 140µA, saves 100µA and extends the standby time by 340µA/240µA, or 1.417 times.

The baseband internal analog circuit is typically 2.4V-3.0V, and it requires 200-600mV dropout. This LDO is on all the time, so it requires low quiescent current as well. The cellular phone real-time clock LDO needs a very low quiescent current, since this LDO is on all the time even though the handset is powered off.

The AP133, consuming only around 40µA for all input range and output loading, provides great power saving in portable and low power applications.

Wide Output Range

The AP133, with a wide output range of 1.0V to 5.0V, provides a versatile LDO solution for many portable applications.

High PSRR

The RF circuit consists of receive and transmit sections, which typically require 2.6V-3.0V supply voltage. The RF circuits such as LNA (low-noise amplifier), up/down-converter, mixer, PLL, VCO, and IF stage, require low noise and high PSRR LDOs. The temperature-compensated crystal oscillator circuit requires very high PSRR at RF power amplifier burst frequency. For instance, minimum 65dB PSRR at 217Hz is recommended for the GSM handsets.

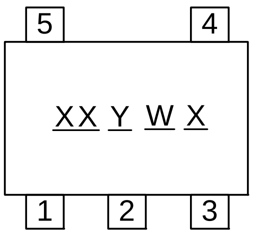
In order to provide good audio quality, the audio power supply for hand-free, game, MP3, and multimedia applications in cellular phones, require low-noise and high PSRR at audio frequency range (20Hz-20kHz).

The AP133, with PSRR of 70dB at 1kHz in best case, is suitable for some of these applications that require high PSRR.

Marking Information

(1) SOT25

(Top View)

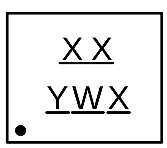


XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Green

Part Number	Package	Identification Code
AP133-W	SOT25	NB

(2) DFN2020-6

(Top View)

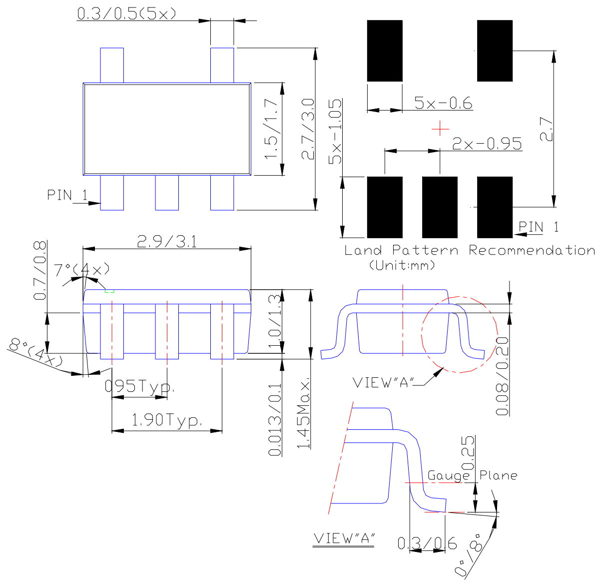


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Green

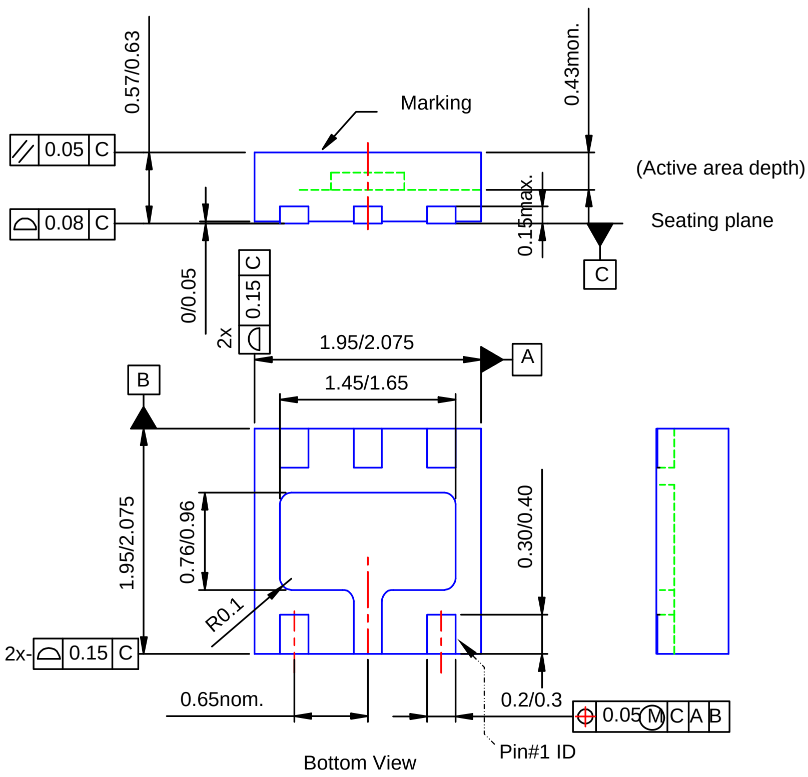
Part Number	Package	Identification Code
AP133-SN	DFN2020-6	NB

Package Information (All Dimensions in mm)

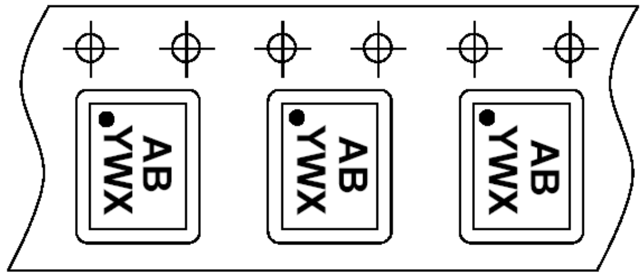
(1) Package Type: SOT25

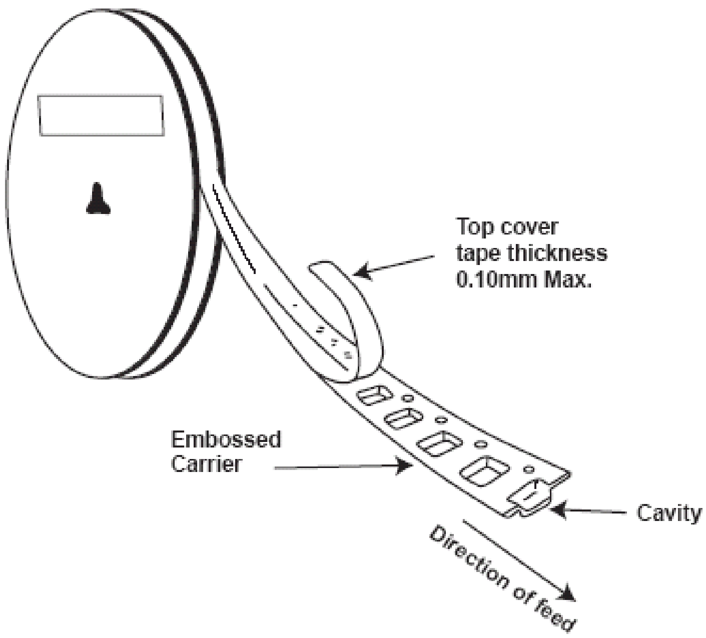


(2) Package Type: DFN2020-6



Taping Orientation





Notes: 5. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf