

July 1997 Revised December 1999

#### FST16232

# Synchronous 16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch

#### **General Description**

The Fairchild Switch FST16232 is a 16-bit to 32-bit highspeed CMOS TTL-compatible synchronous multiplexer/ demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device allows two separate datapaths to be multiplexed onto, or demultiplexed from, a single path. Two control select pins  $(S_1,\ S_0)$  are synchronous and clocked on the rising edge of CLK when  $\overline{\text{CLKEN}}$  is LOW.

#### **Features**

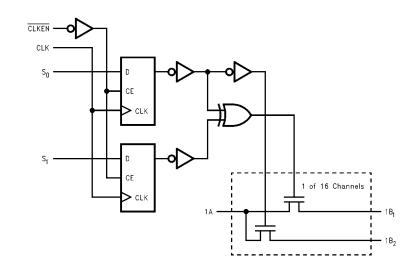
- $\blacksquare$  4 $\Omega$  switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I<sub>CC</sub>.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

#### **Ordering Code:**

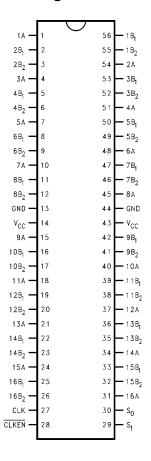
_	Order Number	Package Number	Package Description					
F	ST16232MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide					
F	ST16232MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide					

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### **Logic Diagram**



# **Connection Diagram**



# **Pin Descriptions**

Pin Name	Description					
S <sub>1</sub> , S <sub>0</sub>	Control Pins					
CLK	Clock Input					
CLKEN	Clock Enable Input					
1A, 2A	Bus A					
1B, 2B	Bus B					

### **Truth Table**

		Inputs	Francisco.		
S <sub>1</sub>	S <sub>0</sub>	CLK	CLKEN	Function	
Х	Х	Х	Н	Last State	
L	L	1	L	Disconnect	
L	Н	1	L	$A = B_1$ and $A = B_2$	
Н	L	<b>↑</b>	L	A = B <sub>1</sub>	
Н	Н	1	L	A = B <sub>2</sub>	

#### **Absolute Maximum Ratings**(Note 1)

# Recommended Operating Conditions (Note 3)

 $\begin{array}{ll} \mbox{Power Supply Operating ($V_{CC}$)} & 4.0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Voltage ($V_{IN}$)} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Output Voltage ($V_{OUT}$)} & 0 \mbox{V to } 5.5 \mbox{V} \\ \end{array}$ 

Input Rise and Fall Time (t<sub>r</sub>, t<sub>f</sub>)

Switch Control Input 0nS/V to 5nS/V Switch I/O 0nS/V to DC Free Air Operating Temperature ( $T_A$ ) -40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float

#### **DC Electrical Characteristics**

	Parameter	V <sub>CC</sub> (V)	$T_A = -40  ^{\circ}\text{C} \text{ to } +85  ^{\circ}\text{C}$				
Symbol			Min	Typ (Note 4)	Max	Units	Conditions
V <sub>IK</sub>	Clamp Diode Voltage	4.5			-1.2	V	I <sub>IN</sub> = -18mA
V <sub>IH</sub>	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V <sub>IL</sub>	LOW Level Input Voltage	4.0-5.5			8.0	V	
l <sub>l</sub>	Input Leakage Current	5.5			±1.0	μΑ	0≤ V <sub>IN</sub> ≤5.5V
		0			10	μΑ	V <sub>IN</sub> = 5.5V
l <sub>OFF</sub>	OFF-STATE Leakage Current	5.5			±1.0	μΑ	0 ≤A, B ≤V <sub>CC</sub>
R <sub>ON</sub>	Switch On Resistance	4.5		4	7	Ω	$V_{IN} = 0V$ , $I_{IN} = 64mA$
	(Note 5)	4.5		4	7	Ω	$V_{IN} = 0V$ , $I_{IN} = 30mA$
		4.5		8	12	Ω	V <sub>IN</sub> = 2.4V, I <sub>IN</sub> = 15mA
		4.0		11	20	Ω	$V_{IN} = 2.4V, I_{IN} = 15mA$
I <sub>CC</sub>	Quiescent Supply Current	5.5			3	μΑ	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
Δ I <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	5.5			2.5	mA	One input at 3.4V
							Other inputs at V <sub>CC</sub> or GND

Note 4: Typical values are at  $V_{CC} = 5.0V$  and  $T_A = +25^{\circ}C$ 

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

#### **AC Electrical Characteristics**

		$T_A = -40$ °C to +85 °C, $C_L = 50$ pF, RU = RD = $500\Omega$				Units	Conditions	Figure
Symbol	Parameter							
Symbol		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$		Ullits	Conditions	No.
		Min	Max	Min	Max	1		
f <sub>MAX</sub>	Maximum Clock Frequency	150		150		MHz	V <sub>I</sub> = OPEN	Figure 1 Figure 2
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V <sub>I</sub> = OPEN	Figure 1 Figure 2
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay CLK to B or A	2.0	6.3		6.0	ns	V <sub>I</sub> = OPEN	Figure 1 Figure 2
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	1.7	8.5		9.0	ns	$V_I = 7V$ for $t_{PZL}$ ,	Figure 1 Figure 2
	CLK to $A = B_1 = B_2$	1.7					$V_I = OPEN \text{ for } t_{PZH}$	
	Output Enable Time	2.0	6.5		6.5	ns	$V_I = 7V$ for $t_{PZL}$ ,	Figure 1 Figure 2
	CLK to A or B <sub>1</sub> or B <sub>2</sub>	2.0	0.5		0.5	115	$V_I = OPEN$ for $t_{PZH}$	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	1.0	8.5		9.0	ns	$V_I = 7V$ for $t_{PLZ}$ ,	Figure 1 Figure 2
	CLK to A or B	1.0	0.5		3.0	115	$V_I = OPEN \text{ for } t_{PHZ}$	
t <sub>S</sub>	Setup Time S <sub>1</sub> , S <sub>0</sub> before CLK ↑	2.5		2.8		ns		Figure 1
	Setup Time CLKEN before CLK↑	1.8		2.0				Figure 2
t <sub>H</sub>	Hold Time S <sub>1</sub> , S <sub>0</sub> after CLK ↑	1.0		1.0				Figure 1
	Hold Time CLKEN after CLK ↑	1.5		1.5		ns		Figure 2
t <sub>W</sub>	Pulse Width	3.1		3.1		ns	Clock HIGH or LOW	Figure 1 Figure 2

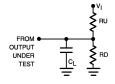
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

#### Capacitance (Note 7)

Symbol	Parameter	Тур	Max	Units	Conditions
C <sub>IN</sub>	Control pin Input Capacitance	4		pF	V <sub>CC</sub> = 5.0V
C <sub>I/O</sub>	Input/Output Capacitance	7		pF	$V_{CC} = 5.0V, S_0, S_1 = 0V$

Note 7: T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

# **AC Loading and Waveforms**



Note: Input driven by 50  $\Omega$  source terminated in 50  $\Omega$ 

Note:  $\mathbf{C}_{\mathsf{L}}$  includes load and stray capacitance

**Note:** Input PRR = 1.0 MHz,  $t_W = 500 \text{ ns}$ 

#### FIGURE 1. AC Test Circuit

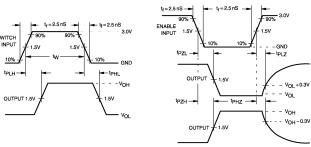
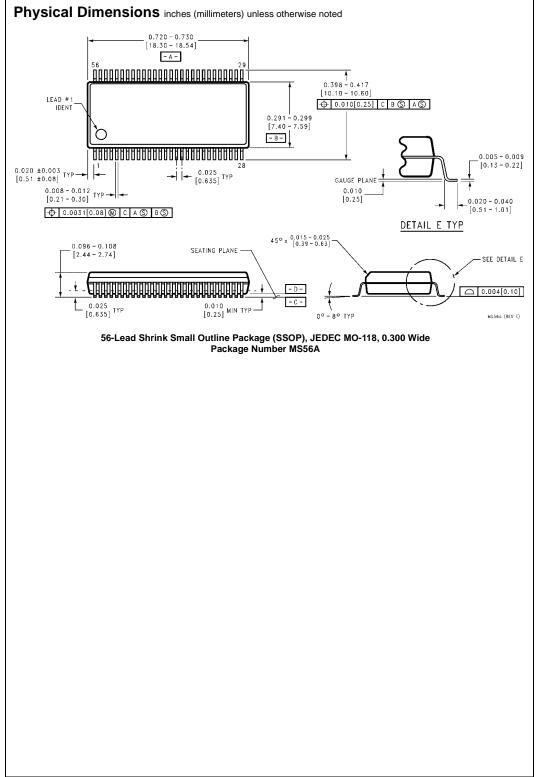
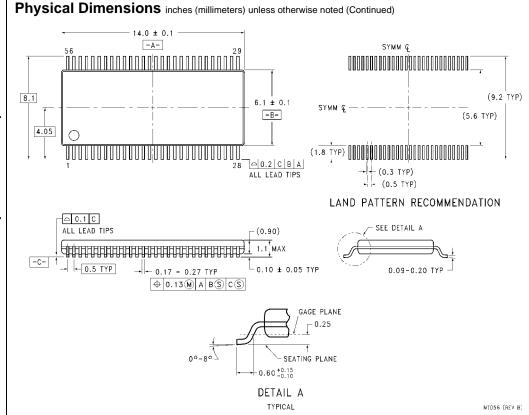


FIGURE 2. AC Waveforms





56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

#### **Technology Description**

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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