

NDF02N60Z, NDD02N60Z

N-Channel Power MOSFET 600 V, 4.8 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode-Protected Gate
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	NDF	NDD	Unit
Drain-to-Source Voltage	V _{DSS}	600		V
Continuous Drain Current R _{θJC} (Note 1)	I _D	2.4	2.2	A
Continuous Drain Current R _{θJC} T _A = 100°C (Note 1)	I _D	1.6	1.4	A
Pulsed Drain Current, V _{GS} @ 10 V	I _{DM}	10	9	A
Power Dissipation R _{θJC}	P _D	24	57	W
Gate-to-Source Voltage	V _{GS}	30		V
Single Pulse Avalanche Energy, I _D = 2.4 A	E _{AS}	120		mJ
ESD (HBM) (JESD 22-A114)	V _{esd}	2500		V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T _A = 25°C) (Figure 17)	V _{ISO}	4500		V
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Continuous Source Current (Body Diode)	I _S	2.4		A
Maximum Temperature for Soldering Leads	T _L	260		°C
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

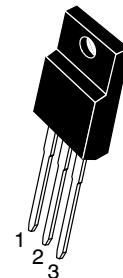
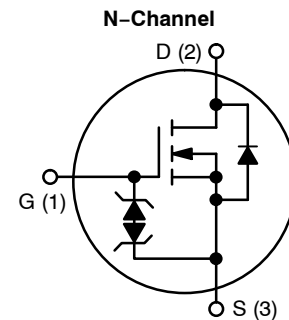
1. Limited by maximum junction temperature
2. I_{SD} = 2.4 A, di/dt ≤ 100 A/μs, V_{DD} ≤ BV_{DSS}, T_J = +150°C



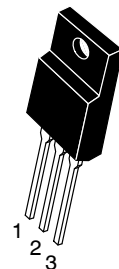
ON Semiconductor®

<http://onsemi.com>

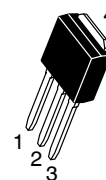
V _{DSS}	R _{DS(on)} (MAX) @ 1 A
600 V	4.8 Ω



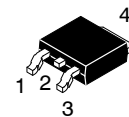
NDF02N60ZG
TO-220FP
CASE 221D



NDF02N60ZH
TO-220FP
CASE 221AH



NDD02N60Z-1G
IPAK
CASE 369D



NDD02N60ZT4G
DPAK
CASE 369AA

ORDERING AND MARKING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

NDF02N60Z, NDD02N60Z

Thermal Resistance

Parameter	Symbol	Value	Unit	
Junction-to-Case (Drain)	$R_{\theta JC}$	NDF02N60Z	4.9	°C/W
		NDD02N60Z	2.2	
Junction-to-Ambient Steady State	$R_{\theta JA}$	(Note 3) NDF02N60Z	51	
		(Note 4) NDD02N60Z	41	
		(Note 3) NDD02N60Z-1	80	

3. Insertion mounted

4. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	BV_{DSS}	600			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D = 1\text{ mA}$	$\Delta BV_{DSS}/\Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	25°C		1	μA
			150°C		50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	I_{GSS}			±10	μA

ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$	$R_{DS(on)}$		4.0	4.8	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	$V_{GS(th)}$	3.0	4.0	4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 1.2\text{ A}$	g_{FS}		1.7		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 6)	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	C_{iss}	215	274	325	pF
Output Capacitance (Note 6)		C_{oss}	25	34	45	
Reverse Transfer Capacitance (Note 6)		C_{rss}	4.0	7.0	10	
Total Gate Charge (Note 6)	$V_{DD} = 300\text{ V}, I_D = 2.4\text{ A},$ $V_{GS} = 10\text{ V}$	Q_g	5.0	10	16	nC
Gate-to-Source Charge (Note 6)		Q_{gs}	1.5	2.4	4.0	
Gate-to-Drain ("Miller") Charge (Note 6)		Q_{gd}	3.5	5.3	8.0	
Plateau Voltage		V_{GP}		6.4		V
Gate Resistance		R_g		4.9		Ω

RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 2.4\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ }\Omega$	$t_{d(on)}$		9.0		ns
Rise Time		t_r		7.0		
Turn-Off Delay Time		$t_{d(off)}$		15		
Fall Time		t_f		7.0		

SOURCE-DRAIN DIODE CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	$I_S = 2.4\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 2.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}		240		ns
Reverse Recovery Charge		Q_{rr}		0.7		μC

5. Pulse Width $\leq 380\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Guaranteed by design.

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TYPICAL CHARACTERISTICS

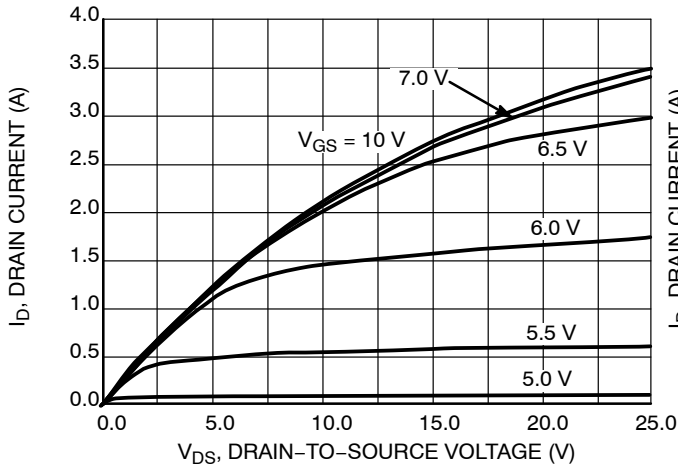


Figure 1. On-Region Characteristics

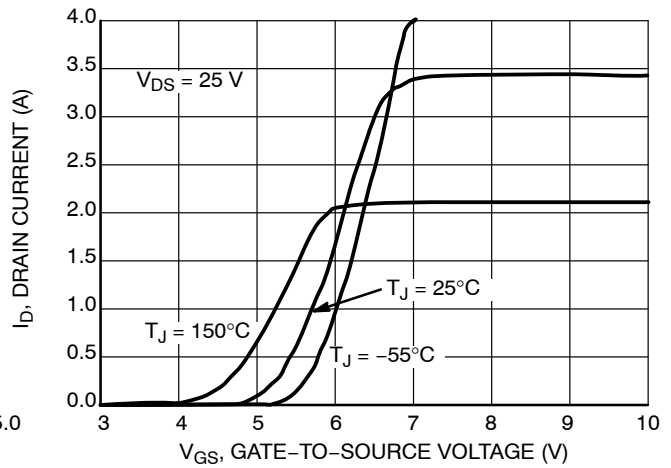


Figure 2. Transfer Characteristics

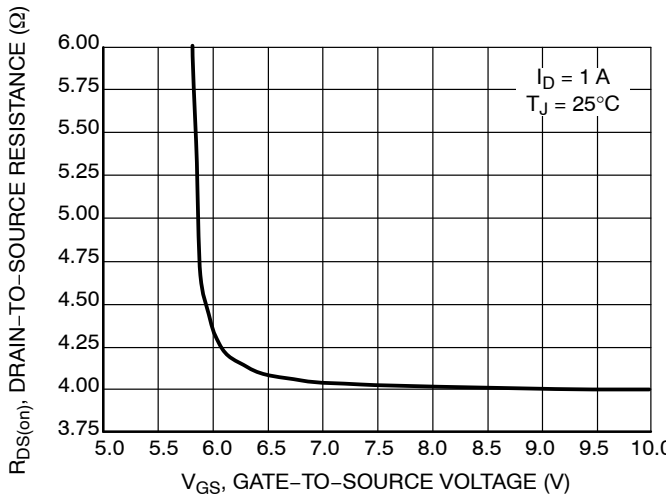


Figure 3. On-Region versus Gate-to-Source Voltage

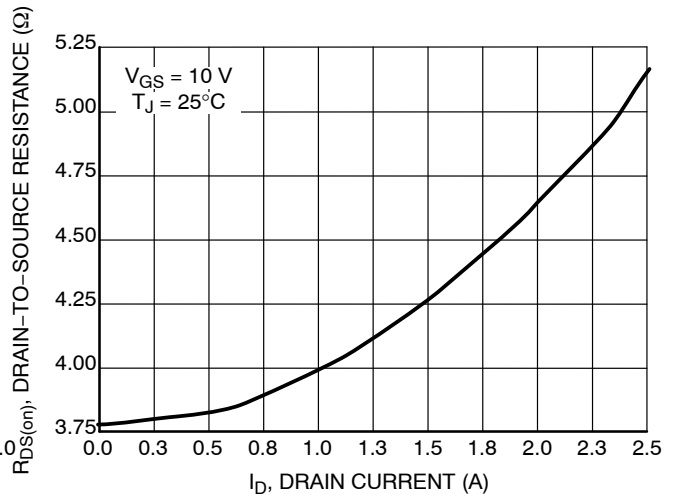


Figure 4. On-Resistance versus Drain Current and Gate Voltage

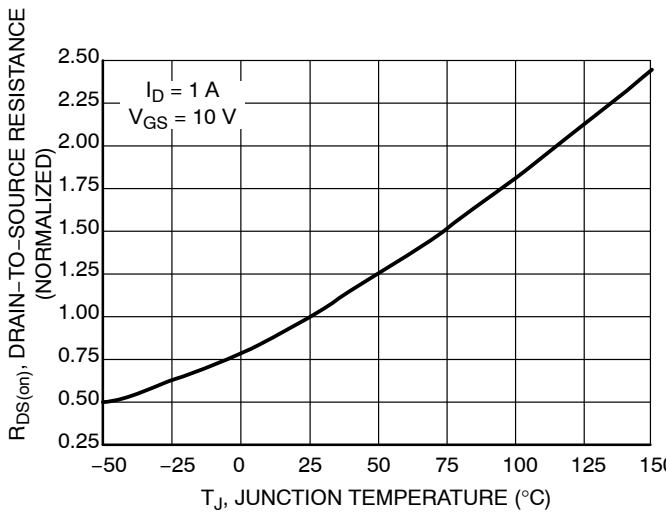


Figure 5. On-Resistance Variation with Temperature

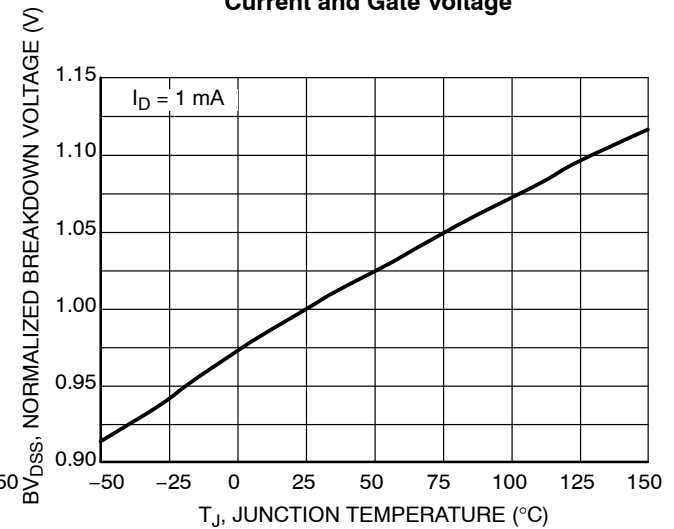


Figure 6. BV_{DSS} Variation with Temperature

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TYPICAL CHARACTERISTICS

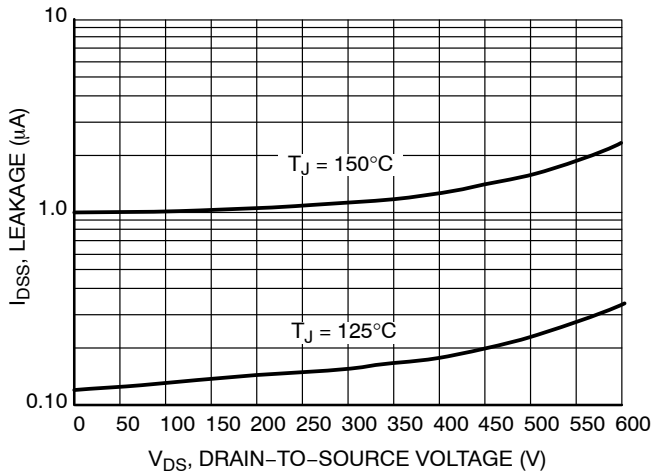


Figure 7. Drain-to-Source Leakage Current versus Voltage

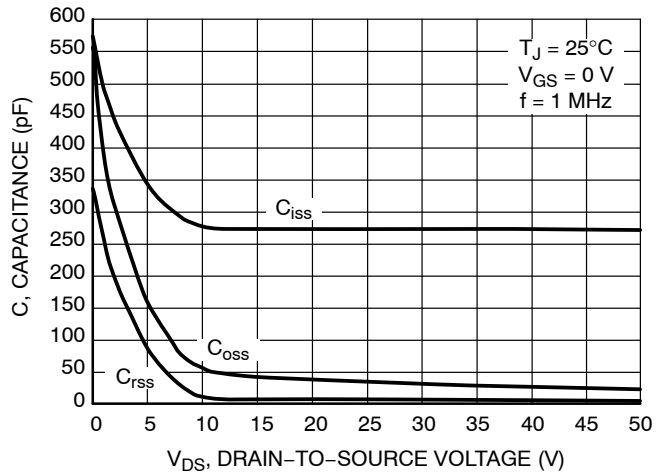


Figure 8. Capacitance Variation

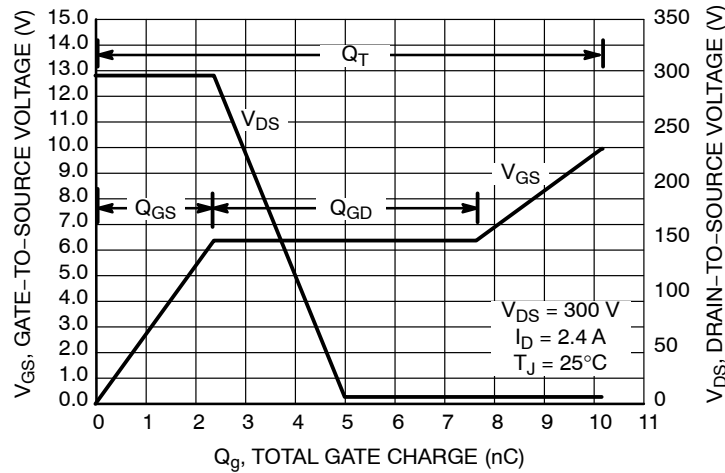


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

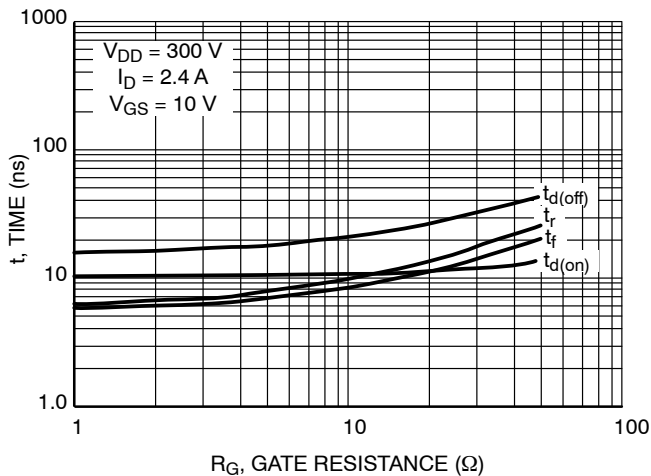


Figure 10. Resistive Switching Time Variation versus Gate Resistance

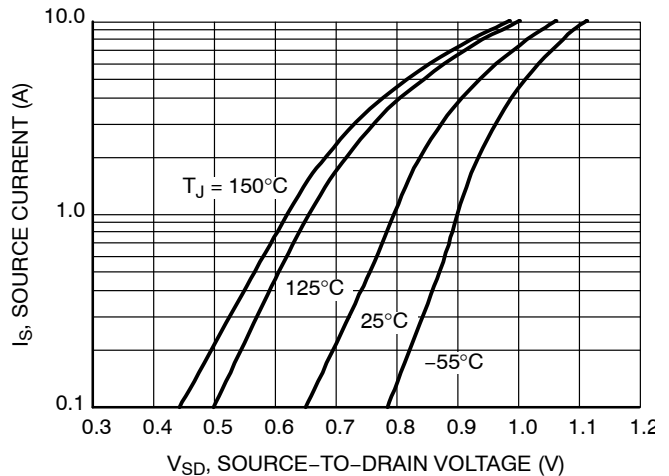


Figure 11. Diode Forward Voltage versus Current

NDF02N60Z, NDD02N60Z

TYPICAL CHARACTERISTICS

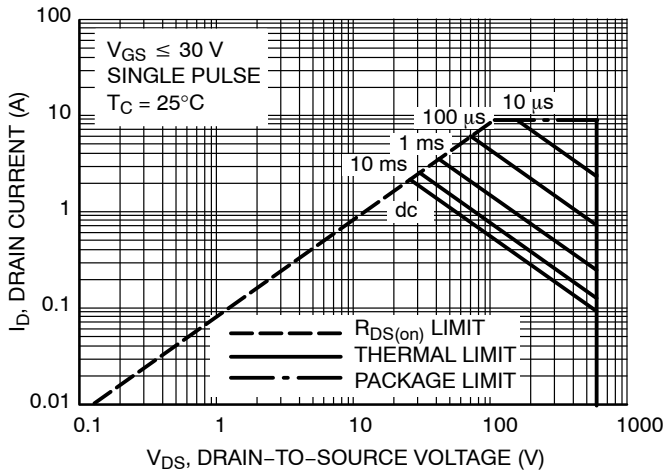


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD02N60Z

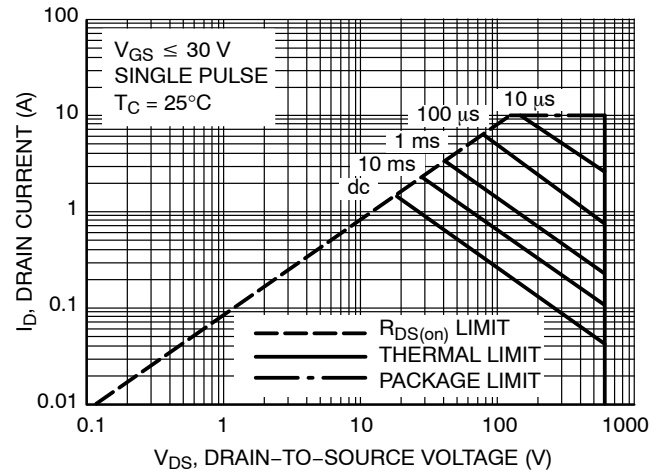


Figure 13. Maximum Rated Forward Biased Safe Operating Area NDF02N60Z

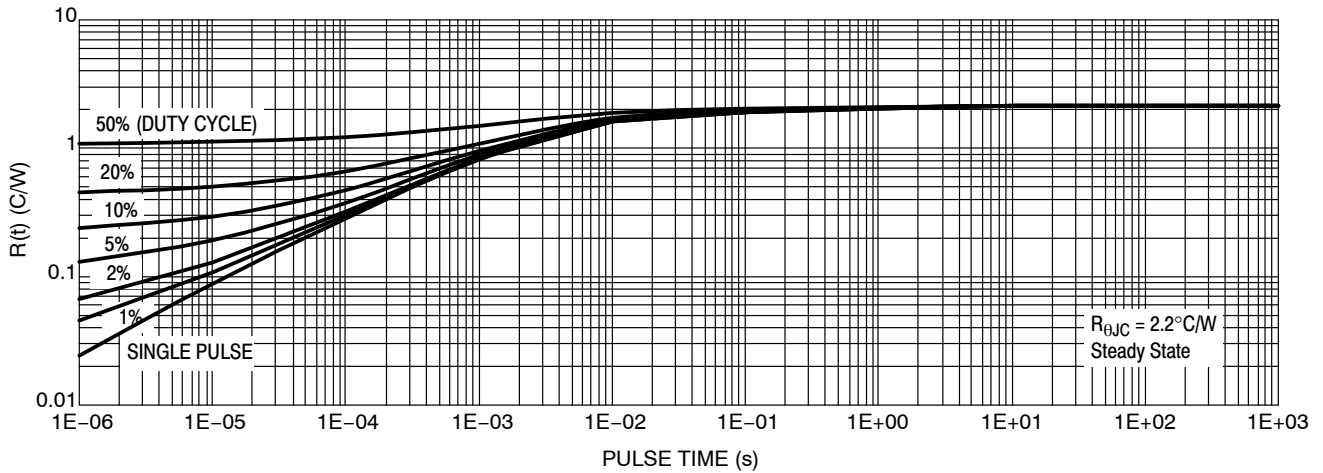


Figure 14. Thermal Impedance (Junction-to-Case) for NDD02N60Z

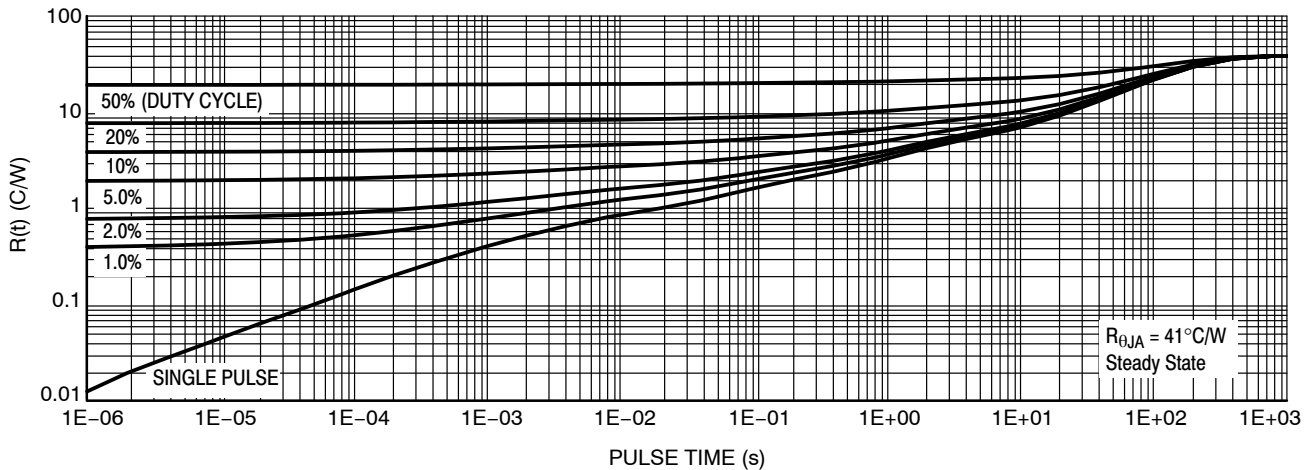


Figure 15. Thermal Impedance (Junction-to-Ambient) for NDD02N60Z

NDF02N60Z, NDD02N60Z

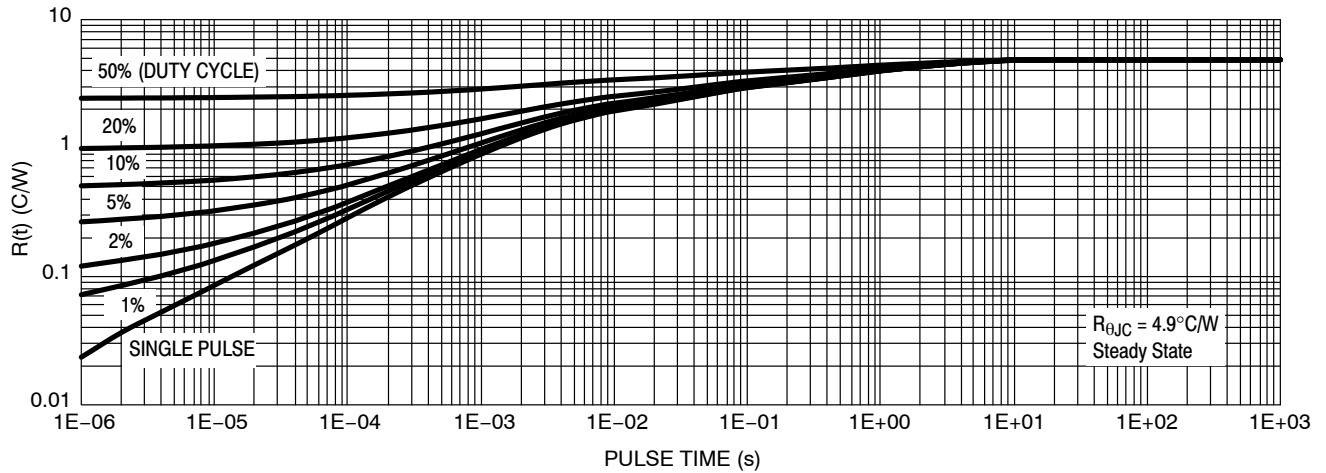


Figure 16. Thermal Impedance (Junction-to-Case) for NDF02N60Z

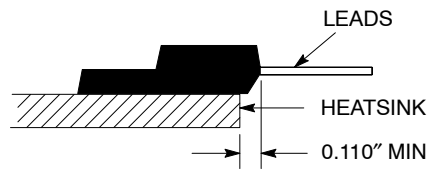


Figure 17. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

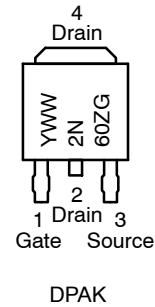
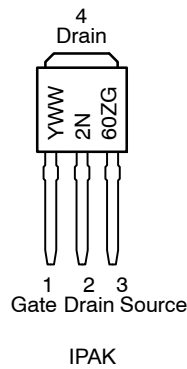
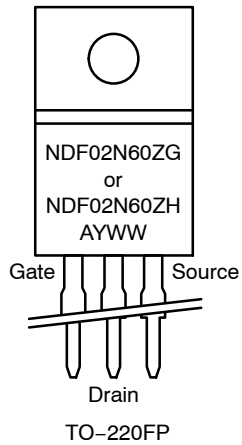
NDF02N60Z, NDD02N60Z

ORDERING INFORMATION

Order Number	Package	Shipping†
NDF02N60ZG	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDF02N60ZH	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDD02N60Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD02N60ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

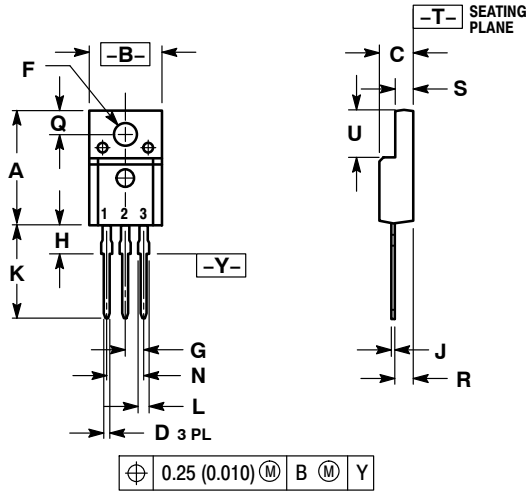


A = Location Code
 Y = Year
 WW = Work Week
 G, H = Pb-Free, Halogen-Free Package

NDF02N60Z, NDD02N60Z

PACKAGE DIMENSIONS

TO-220 FULLPAK CASE 221D-03 ISSUE K

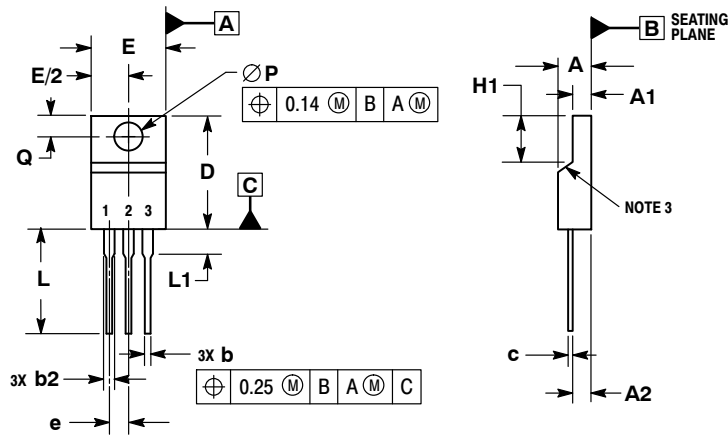


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH
 3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

- STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

TO-220 FULLPACK, 3-LEAD CASE 221AH ISSUE D



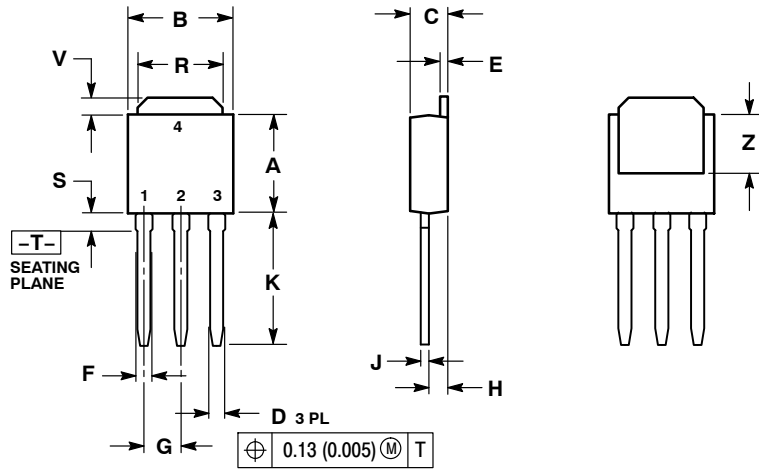
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. CONTOUR UNCONTROLLED IN THIS AREA.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
 5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.

DIM	MILLIMETERS	
	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.70
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.70	7.10
L	12.70	14.73
L1	---	2.10
P	3.00	3.40
Q	2.80	3.20

NDF02N60Z, NDD02N60Z

PACKAGE DIMENSIONS

IPAK
CASE 369D
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

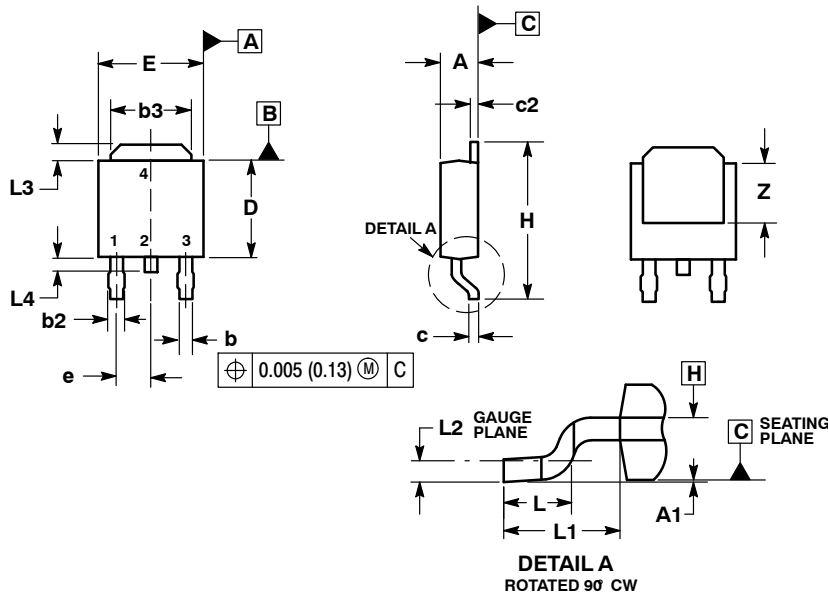
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NDF02N60Z, NDD02N60Z

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369AA ISSUE B

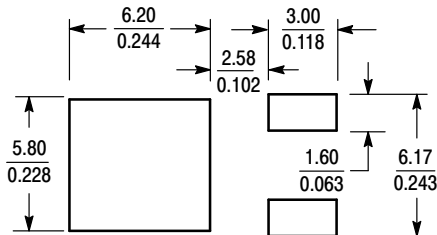


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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