TOP412/414

TOPSwitch® Family

Three-terminal DC to DC PWM Switch

Product Highlights

Low Cost Replacement for Discrete Switchers
- Up to 15 fewer components - cuts cost, increases reliability
- Allows for a smaller and lighter solution under 12 mm height, all surface mount components

Over 80% Efficiency in Flyback Topology
- Built-in start-up and current limit reduce DC losses
- Low capacitance MOSFET cuts switching losses
- CMOS controller/gate driver consumes only 7 mW
- 70% maximum duty cycle minimizes conduction losses

Simplifies Design - Reduces Time to Market
- Integrated PWM Controller and high power MOSFET
- Only one external capacitor needed for compensation, bypass and start-up/auto-restart functions

System Level Fault Protection Features
- Auto-restart and cycle by cycle current limiting functions handle both primary and secondary faults
- On-chip latching thermal shutdown protects the entire system against overload

Highly Versatile
- Implements Buck, Boost, Flyback or Forward topology
- Easily interfaces with both opto and primary feedback
- Supports continuous or discontinuous mode of operation
- Specified for operation down to 16 V DC input

Description

The *TOPSwitch* family implements, with only three terminals, all functions necessary for a DC to DC, converter: high voltage N-channel power MOSFET with controlled turn-on gate driver, voltage mode PWM controller with integrated 120 kHz oscillator, high voltage start-up bias circuit, bandgap derived reference, bias shunt regulator/error amplifier for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or self oscillating (RCC) switching converter solutions, a *TOPSwitch* integrated circuit can reduce total cost, component count, size, weight and at the same time increase efficiency and system reliability. This device is well suited for Telecom, Cablecom and other DC to DC converter applications up to 21 W of output power. Internally, the lead frame of the SMD-8 package uses six of its pins to transfer heat from the chip directly to the board, eliminating the cost of a heat sink.

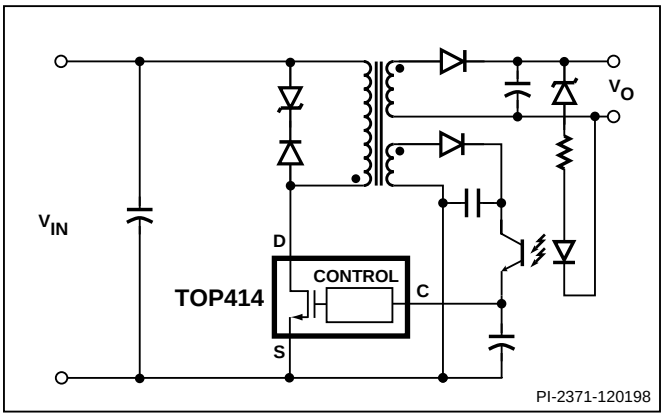


Figure 1. Typical Application.

Output Power Capability[1-4]		
MINIMUM INPUT VOLTAGE	ORDER PART NUMBER	
	TOP412G	TOP414G
18 VDC	3 W	4 W
24 VDC	5 W	6 W
36 VDC	7 W	9 W
48 VDC	9 W	12 W
60 VDC	12 W	15 W
72 VDC	15 W	18 W
90 VDC	18 W	21 W

Table 1. TOP412/414 Output Power.

Notes: **1**. Assumes maximum junction temperature of 100 °C **2**. Assumes output of 5 V and K_{RP} of 0.4 **3.** Soldered to 1 sq. inch (645 mm^2), 2 oz. copper clad (610 gm/mm^2) **4**. The continuous power capability in a given application depends on thermal environment, transformer design, efficiency required, input storage capacity, etc.

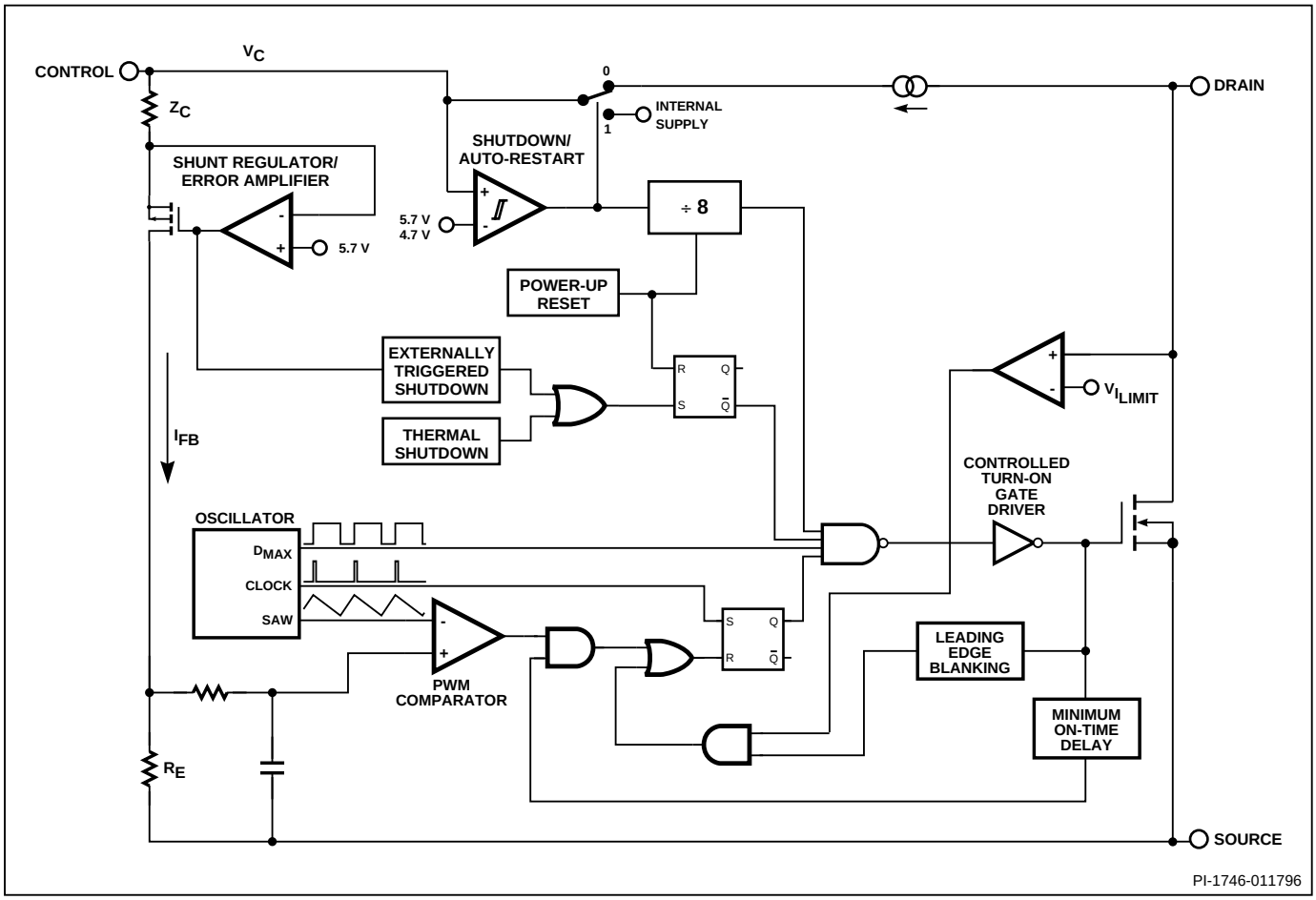


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN Pin:
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

CONTROL Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. Trigger input for latching shutdown. It is also used as the supply bypass and auto-restart/ compensation capacitor connection point.

SOURCE Pin:
Output MOSFET source connection. Primary-side circuit common, power return, and reference point.

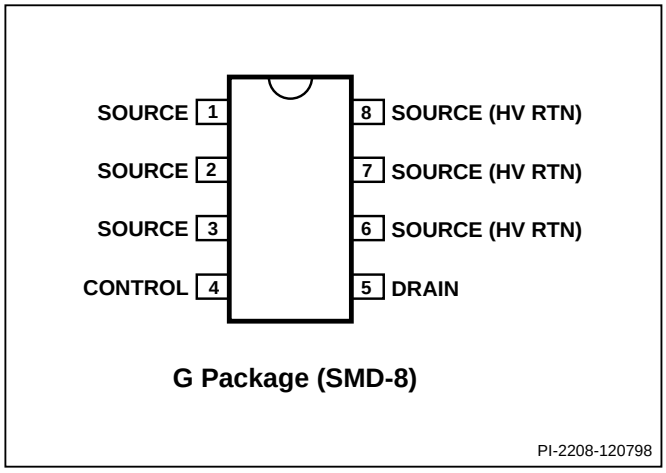


Figure 3. Pin Configuration.

TOPSwitch Family Functional Description

TOPSwitch is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the internal output MOSFET duty cycle linearly decreases with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

Control Voltage Supply

CONTROL pin voltage V_C is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin (C_T) also sets the auto-restart timing as well as control loop compensation. V_C is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, V_C current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance (C_T).

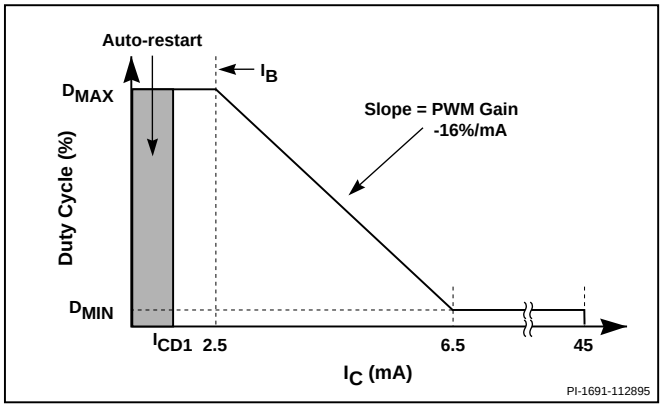


Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

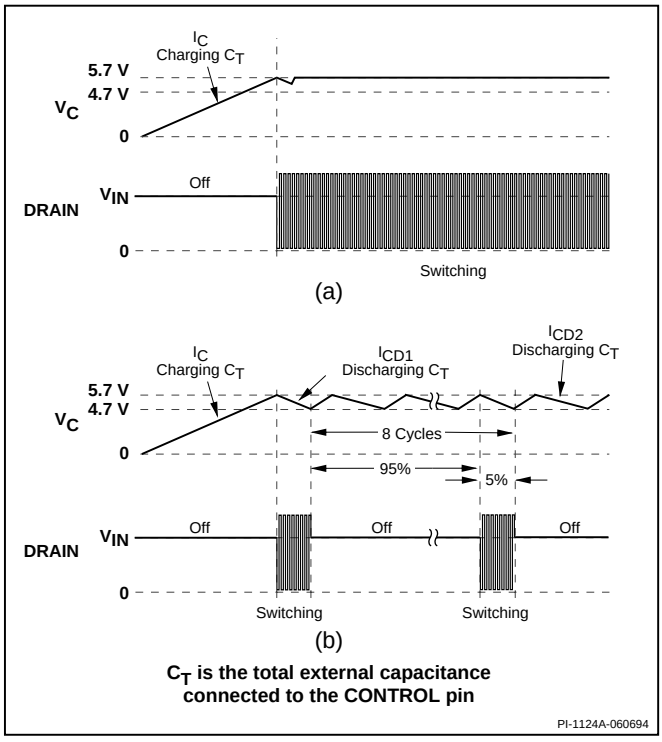


Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.

TOPSwitch Family Functional Description (cont.)

The first time V_C reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the V_C supply current. The shunt regulator keeps V_C at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor R_E. The low dynamic impedance of this pin (Z_C) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pins total external capacitance (C_T) should discharge to the lower threshold, the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source is turned on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps V_C within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

Bandgap Reference

All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

Oscillator

The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 120 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves the frequency accuracy.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current flowing into the CONTROL pin. The error signal across R_E is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

Gate Driver

The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as the error signal.

Cycle-By-Cycle Current Limit

The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON),}$ with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize variation of the effective peak current limit due to temperature related changes in output MOSFET $R_{DS(ON)}$.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

Shutdown/Auto-restart

To minimize *TOPSwitch* power dissipation, the shutdown/auto-restart circuit turns the power supply on and off at a duty cycle of typically 5% if an out of regulation condition persists. Loss of regulation interrupts the external current into the

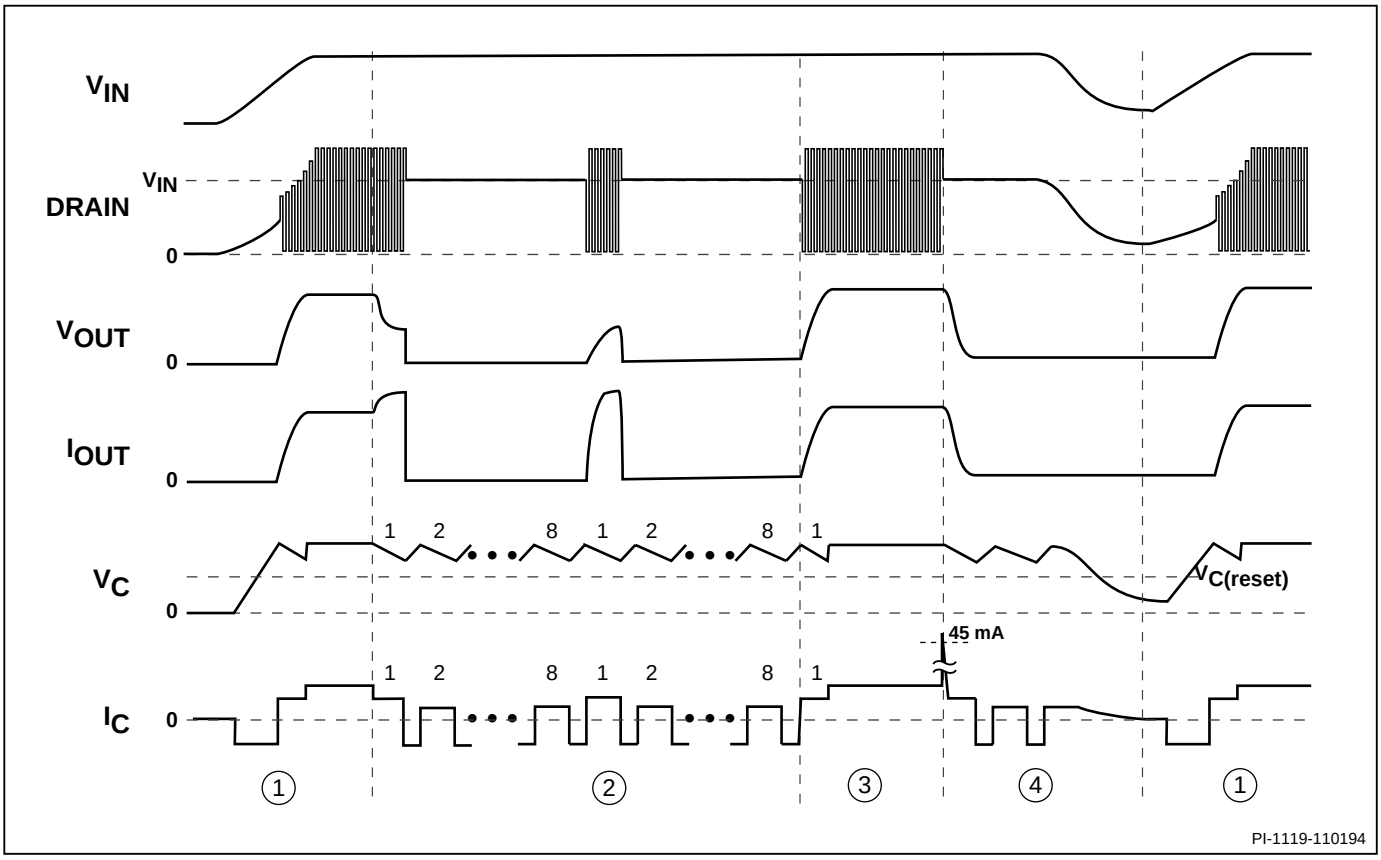


Figure 6. Typical Waveforms for (1) Normal Operation, (2) Auto-restart, (3) Latching Shutdown, and (4) Power Down Reset.

CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode described above. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Latching Shutdown

The output overvoltage protection latch is activated by a high-current pulse into the CONTROL pin. When set, the latch turns off the *TOPSwitch* output. Activating the power-up reset circuit by removing and restoring input power, or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

Over-Temperature Protection

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (typically 145 °C). Activating the power-up reset circuit by removing and restoring input power or momentarily pulling the CONTROL pin below the power-up reset threshold resets the latch and allows *TOPSwitch* to resume normal power supply operation. V_C is regulated in hysteretic mode when the power supply is latched off.

High-voltage Bias Current Source

This current source biases *TOPSwitch* from the DRAIN pin and charges the CONTROL pin external capacitance (C_T) during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart and latched shutdown. The current source is switched on and off with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching.

General Circuit Operation

Figure 7 shows a typical DC-DC converter application using the TOP414G. This supply delivers 5 V at 2 A and works over a wide input range from 36-72 VDC. The power supply operates at an ambient temperature of 0-50 °C.

In order to achieve the highest possible efficiency and smallest possible circuit board area, the primary and secondary current waveform is shaped to have the lowest possible RMS and ripple current. This is achieved by running very continuous and utilizing the maximum duty cycle available.

For the example shown, the maximum component height is 12 mm. The EFD-20 transformer core was chosen to match this maximum component height. The TOP414G has a high current limit, which means that the EF20 core will saturate during startup, until regulation is achieved. This is acceptable with the TOP414G and does not cause device stress (provided the maximum drain voltage is below 250 V peak and provided a Zener is used for clamping). A Zener diode clamp circuit (VR1 and D1) is used in order to clamp the leakage inductance spike to a fixed maximum voltage (an RCD, resistor capacitor diode, clamp circuit would not be acceptable for this application).

In the example circuit, C1 provides local decoupling of the DC input. This is required when the DC input source is distant from this converter. A shottky diode (D2) with low voltage drop provides secondary rectification and does not require additional heat sinking (PC-board provides adequate heat sinking when used with DPAK diode package). Tantalum capacitors (C3,C4) provide low profile and small outline for secondary capacitance (electrolytic capacitors can also be used as replacement). Inductor L1 filters high frequency switching noise forming a π filter with the output capacitors (C3-C6). The control loop gain is set by resistor R2 and the stability is influenced by R1, C3 ,C4, C5 and C6. Resistors R3 and R4 set the DC regulation point and shunt regulator U3 along with bypass capacitor C8, provide the drive for the optocoupler U2. Any remaining switching noise in the system is filtered by ceramic capacitor C9.

Capacitor C2 and resistor R1 form part of the CONTROL pin feedback circuit. Capacitor C_X is used solely to decouple high frequency noise on the control pin.

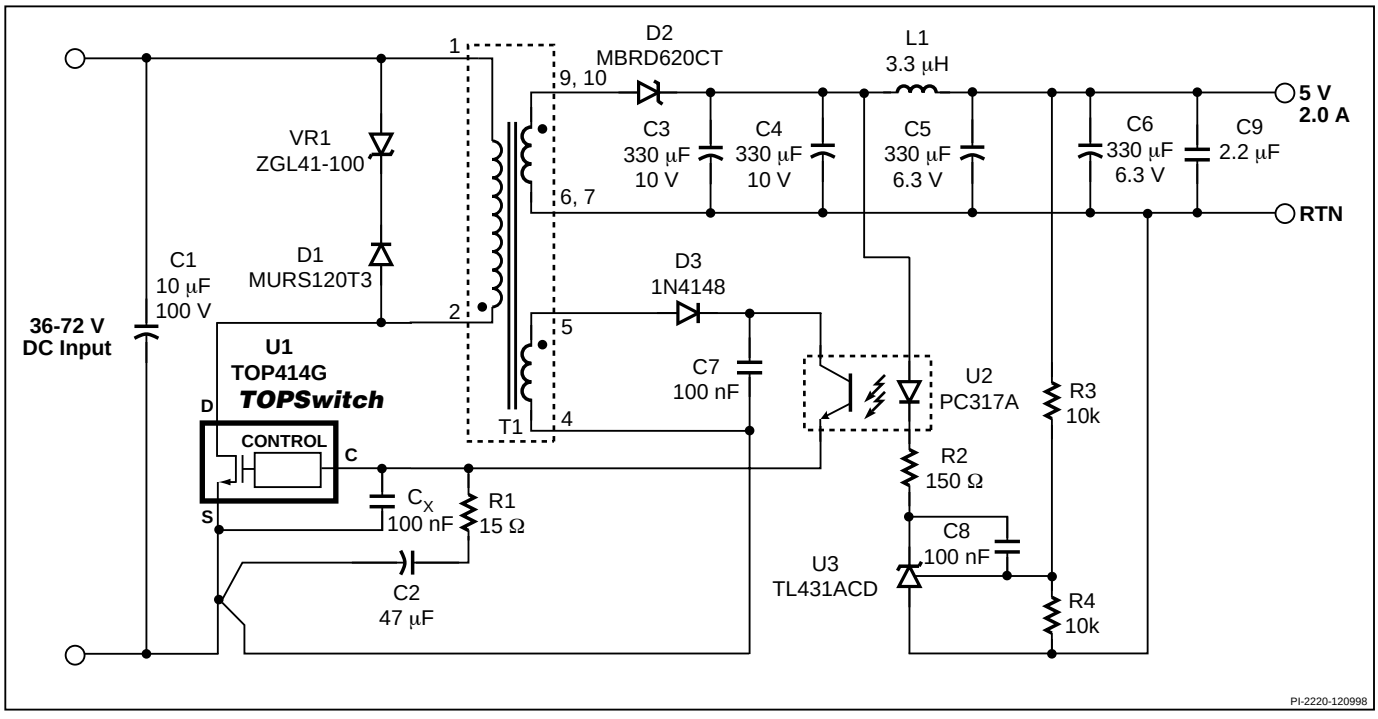


Figure 7. Schematic Diagram of a 5 V, 10 W Isolated DC to DC Converter.

Key Application Issues

Use a Kelvin connection to the SOURCE pin for the CONTROL pin bypass capacitor. Use single point grounding techniques at the SOURCE pin as shown in Figure 8. Use a ceramic high frequency decoupling capacitor to bypass noise transients which might appear on the CONTROL pin. The TOP412 and TOP414 have an over current latching shutdown feature. Failure to use a high frequency decoupling capacitor may allow incidental noise to accidentally trigger this feature.

Limit peak voltage and ringing on the DRAIN voltage at turn-off to a safe value. Use a Zener or TVS Zener diode to clamp the DRAIN voltage.

Do not plug the *TOPSwitch* device into a "hot" IC socket during test. External CONTROL pin capacitance may deliver a surge current sufficient to trigger the shutdown latch which turns the *TOPSwitch* off.

Under some conditions, externally provided bias or supply current driven into the CONTROL pin can hold the *TOPSwitch* in one of the 8 auto-restart cycles indefinitely and prevent starting. Shorting the CONTROL pin to the SOURCE pin will reset the *TOPSwitch*. To avoid this problem when doing bench evaluations, it is recommended that the V_C power supply be turned on before the DRAIN voltage is applied.

CONTROL pin currents during auto-restart operation are much lower at low input voltages (< 20 V) which increases the auto-restart cycle period (see the I_C vs. Drain Voltage Characteristic curve).

In some cases, minimum loading may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to the minimum ON-time.

For additional applications information regarding the *TOPSwitch* family, refer to Web site, *www.powerint.com*.

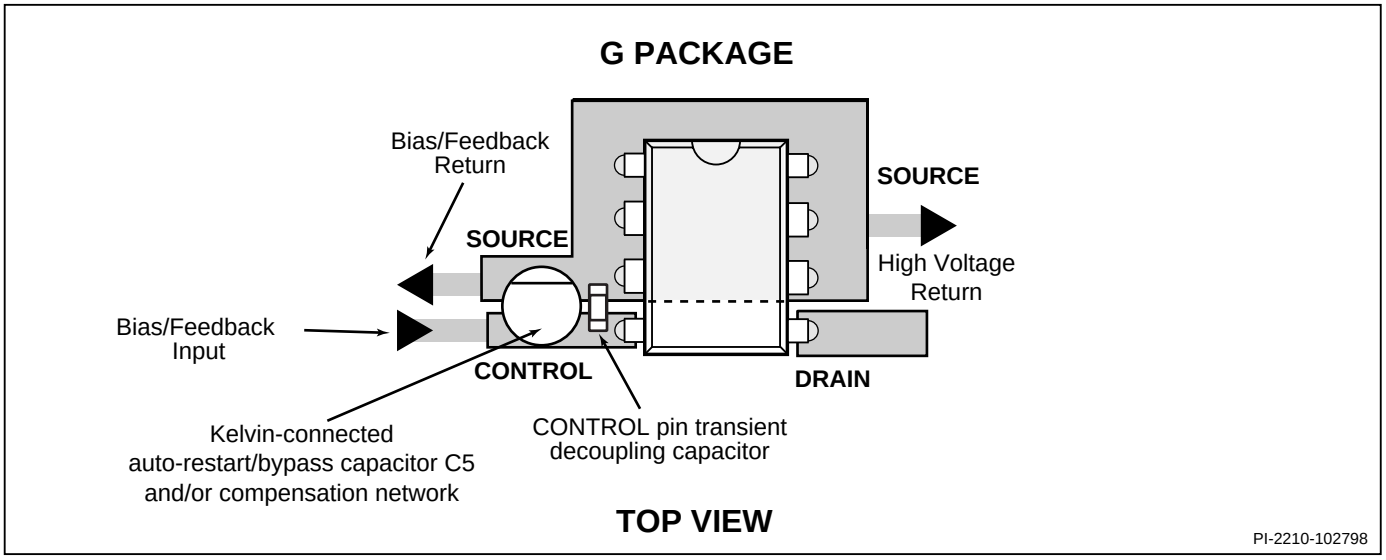


Figure 8. Recommended TOPSwitch Layout.

ABSOLUTE MAXIMUM RATINGS(1)

DRAIN Voltage ..... -0.3 to 350 V
CONTROL Voltage ..... - 0.3 V to 9 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature(2) ..... -40 to 150 °C
Lead Temperature(3) ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

THERMAL IMPEDANCE

Thermal Impedance (θ_{JA}) ..... 35 °C/W(1)
Thermal Impedance (θ_{JC}) ..... 11 °C/W

1. Soldered to 1 sq. inch (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 11 SOURCE = 0 V T_J = -40 to 125 °C		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	I_C = 4 mA, T_J = 25 °C		108	120	132	kHz
Maximum Duty Cycle	DC_{MAX}	$I_C = I_{CD1}$ + 0.5 mA, See Figure 9		64	67	70	%
Minimum Duty Cycle	DC_{MIN}	I_C = 10 mA, See Figure 9	TOP412	1.0	1.8	3.0	%
			TOP414	1.3	2.1	3.3	
PWM Gain		I_C = 4 mA, T_J = 25 °C See Figure 4		-21	-16	-11	%/mA
PWM Gain Temperature Drift		See Note A			-0.05		%/mA/°C
External Bias Current	I_B	See Figure 4		1.5	2.5	4	mA
Dynamic Impedance	Z_C	I_C = 4 mA, T_J = 25 °C See Figure 10		10	15	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 11 SOURCE = 0 V T_J = -40 to 125 °C		Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	I_C	T_J = 25 °C	V_C = 0 V	-2.4	-1.9	-1.2	mA
			V_C = 5 V	-2.0	-1.5	-0.8	
Charging Current Temperature Drift		See Note A			0.4		%/°C
Auto-restart Threshold Voltage	$V_{C(AR)}$	S1 open			5.7		V
UV Lockout Threshold Voltage		S1 open			4.7		V
Auto-restart Hysteresis Voltage		S1 open		0.6	1.0		V
Auto-restart Duty Cycle		S1 open			5	8	%
Auto-restart Frequency		S1 open			1.2		Hz
CIRCUIT PROTECTION							
Self-protection Current Limit	I_{LIMIT}	TOP412 di/dt = 400 mA/µs, T_J = 25 °C		2.00		2.90	A
		TOP414 di/dt = 600 mA/µs, T_J = 25 °C		2.95		4.25	
Leading Edge Blanking Time	t_{LEB}	I_C = 4 mA			150		ns
Current Limit Delay	t_{ILD}	I_C = 4 mA			100		ns
Thermal Shutdown Temperature		I_C = 4 mA		125	145		°C
Latched Shutdown Trigger Current	I_{SD}	See Figure 10		25	45	75	mA
Power-up Reset Threshold Voltage	$V_{C(RESET)}$	S2 open		2.0	3.3	4.2	V

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 11 SOURCE = 0 V T_J = -40 to 125 °C		Min	Typ	Max	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	TOP412 I_D = 270 mA	T_J = 25 °C		2.6	3.0	Ω
			T_J = 100 °C		4.2	5.0	
		TOP414 I_D = 400 mA	T_J = 25 °C		1.7	2.0	
			T_J = 100 °C		2.8	3.3	
OFF-State Current	I_{DSS}	Device in Latched Shutdown I_C = 4 mA, V_{DS} = 280 V, T_A = 125 °C				500	µA
Breakdown Voltage	BV_{DSS}	Device in Latched Shutdown I_C = 4 mA, I_D = 500 µA, T_A = 25 °C		350			V
Rise Time	t_R	Measured With Figure 7 Schematic			100		ns
Fall Time	t_F	Measured With Figure 7 Schematic			50		ns
SUPPLY							
DRAIN Supply Voltage		See Note B		36			V
Shunt Regulator Voltage	$V_{C(SHUNT)}$	I_C = 4 mA		5.5	5.8	6.1	V
Shunt Regulator Temperature Drift					±50		ppm/°C
CONTROL Supply/ Discharge Current	I_{CD1}	Output MOSFET Enabled	TOP412	0.6	1.2	1.6	mA
			TOP414	0.8	1.4	1.8	
	I_{CD2}	Output MOSFET Disabled		0.5	0.8	1.1	

Specification	Symbol	Conditions (Unless Otherwise Specified) See Figure 11 VS2 = 16 V R1 = 0 Ω SOURCE = 0 V T_J = -40 to 125 °C		Min	Typ	Max	Units
LOW INPUT VOLTAGE OPERATION (See Note C)							
DRAIN Supply Voltage		See Note D		16			Volts
CONTROL Pin Charging Current		T_J = 25 °C	V_C= 0 V	-2.30	-1.65	-1.00	mA
			V_C= 5 V	-1.20	-0.64	-0.28	mA
Auto-restart Duty Cycle		S1/Open			4	8	%
Auto-restart Frequency		S1/Open			0.85		Hz

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. It is possible to start up and operate *TOPSwitch* at DRAIN voltages well below 36 V. Refer to the "Low Input Voltage" Specification section for details.

C. This section specifies only parameters affected by low input voltage operation (Drain Voltages less than 36 V). All other parameters remain unchanged.

D. For low input voltage applications, the primary peak current could be set to a lower value than the current limit to increase efficiency. Refer to the Output Characteristics graph (Drain Current vs. Drain Voltage). The voltage across the transformer primary during the ON time is the difference between the input voltage and the drain voltage ($V_{DS(ON)}$).

For example, if the input voltage is 16 VDC and a TOP414 (2.95 A minimum current limit) is used at a primary peak current of 1A. Then the ($V_{DS(ON)}$) is 3 V at 100 °C and the energizing voltage across the transformer primary is 13 V.

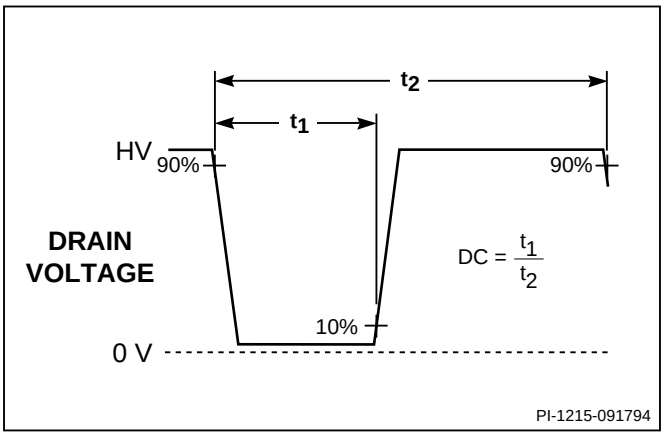


Figure 9. TOPSwitch Duty Cycle Measurement.

TYPICAL CONTROL PIN I-V CHARACTERISTIC

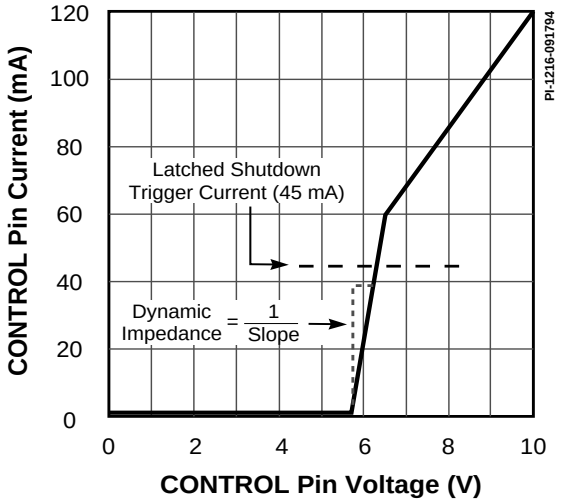
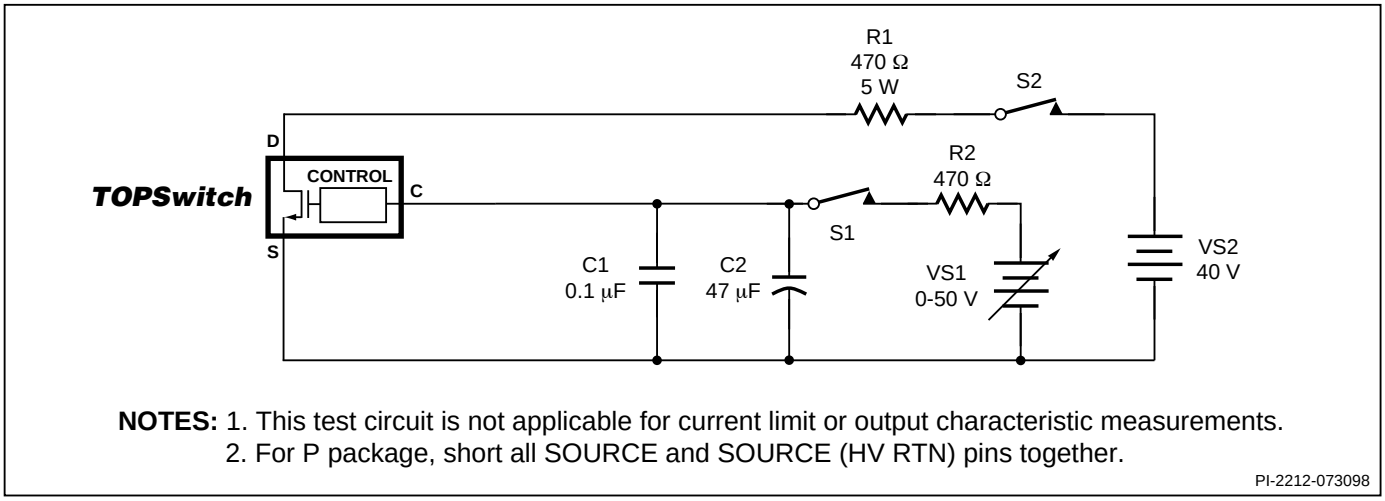


Figure 10. TOPSwitch CONTROL Pin I-V Characteristic.



NOTES: 1. This test circuit is not applicable for current limit or output characteristic measurements.
2. For P package, short all SOURCE and SOURCE (HV RTN) pins together.

PI-2212-073098

Figure 11. TOPSwitch General Test Circuit.

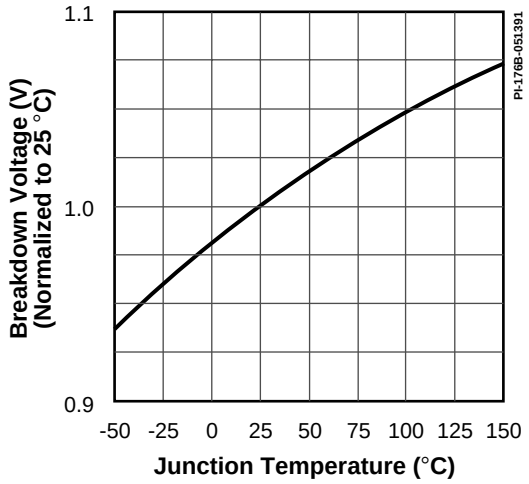
BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *TOPSwitch* by itself outside of a power supply. The schematic shown in Figure 11 is suggested for laboratory testing of *TOPSwitch*.

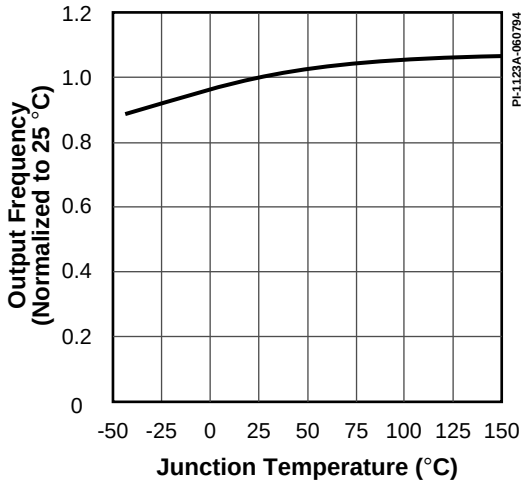
When the DRAIN supply is turned on, the part will be in the auto-restart mode. The CONTROL pin voltage will be oscillating at a low frequency from 4.7 to 5.7 V and the DRAIN is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this auto-restart mode, there is only a 12.5% chance that the CONTROL pin oscillation will be in the correct state (DRAIN active state) so that the continuous DRAIN voltage waveform may be observed. It is recommended that the V_C power supply be turned on first and the DRAIN power supply second if continuous drain voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the 8:1 counter.

Typical Performance Characteristics

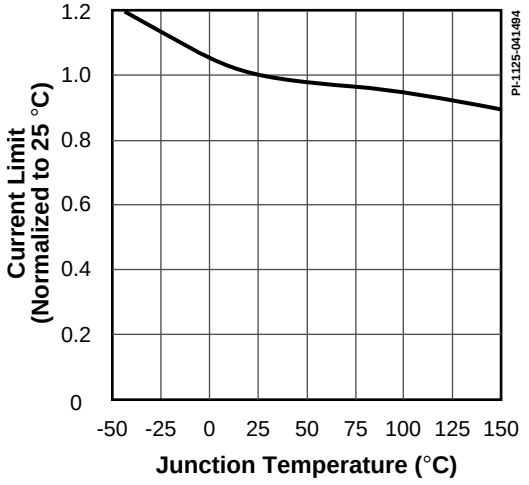
BREAKDOWN vs. TEMPERATURE



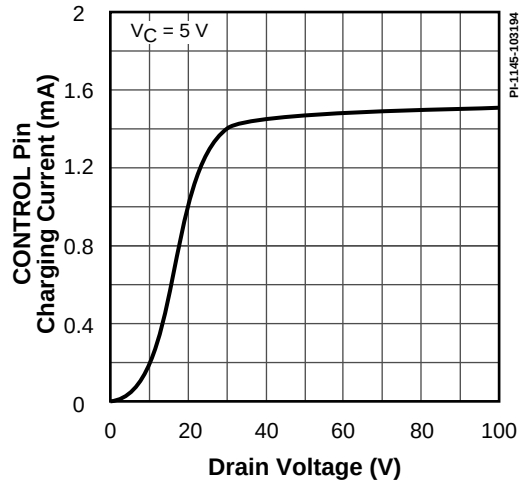
FREQUENCY vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE

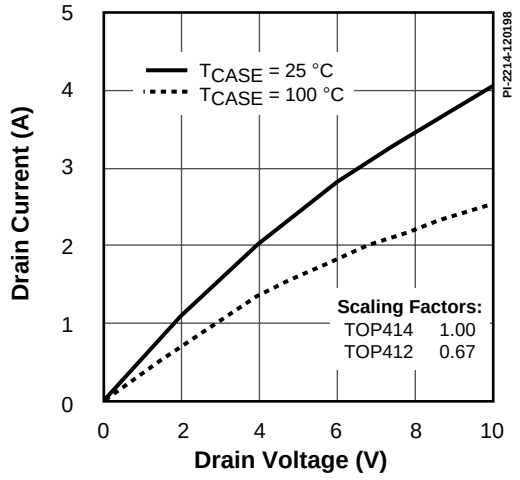


I_C vs. DRAIN VOLTAGE

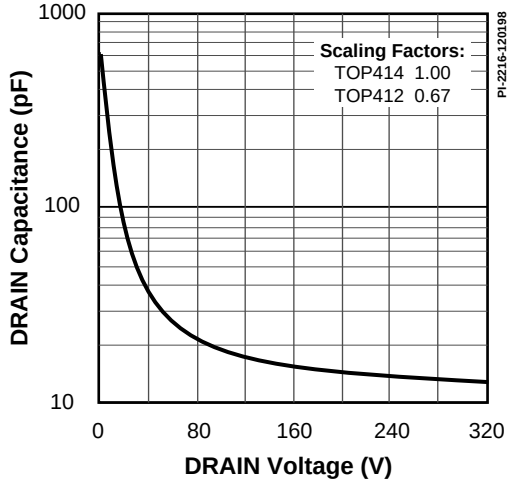


Typical Performance Characteristics (cont.)

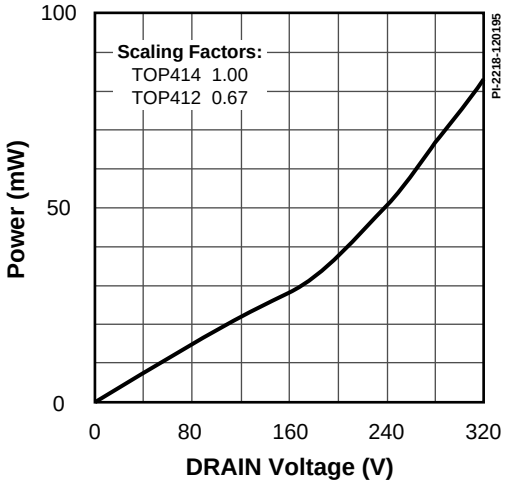
OUTPUT CHARACTERISTICS



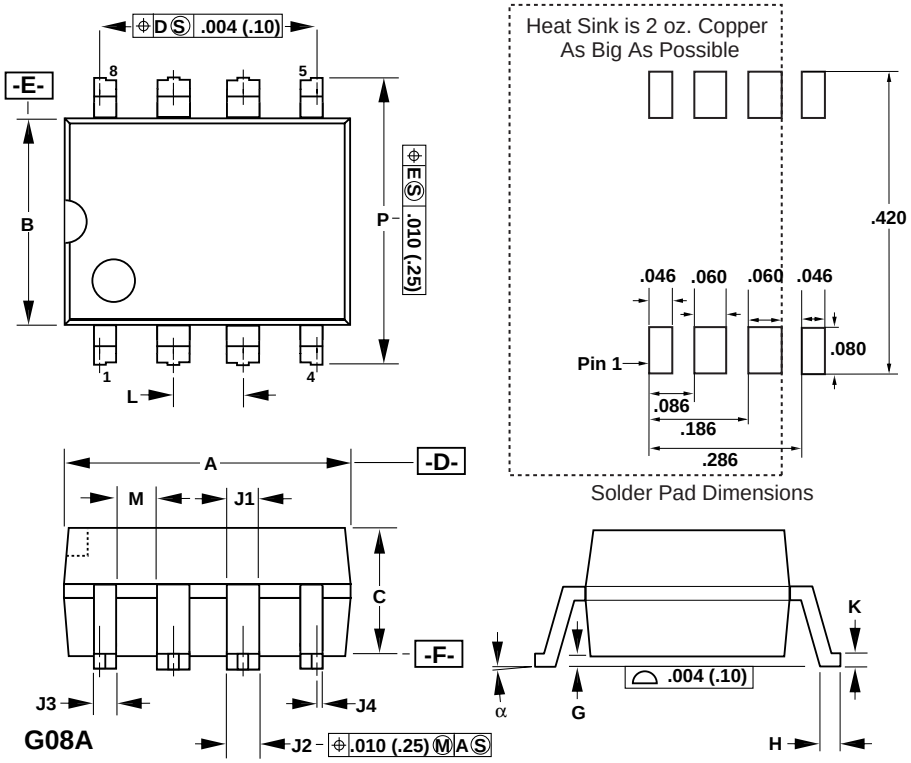
C_{OSS} vs. DRAIN VOLTAGE



DRAIN CAPACITANCE POWER



SMD-8



DIM	inches	mm
A	0.370-0.385	9.40-9.78
B	0.245-0.255	6.22-6.48
C	0.125-0.135	3.18-3.43
G	0.004-0.012	0.10-0.30
H	0.036-0.044	0.91-1.12
J1	0.060 (NOM)	1.52 (NOM)
J2	0.048-0.053	1.22-1.35
J3	0.032-0.037	0.81-0.94
J4	0.007-0.011	0.18-0.28
K	0.010-0.012	0.25-0.30
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
P	0.372-0.388	9.45-9.86
α	0-8°	0-8°

Notes:
1. **Package dimensions conform to JEDEC specification MS-001-AB (issue B, 7/85) except for lead shape and size.**
2. **Controlling dimensions are inches.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
4. **D, E and F are reference datums on the molded body.**

PI-2077-042601

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