

STS12NF30L

N-channel 30 V, 0.008 Ω, 12 A STripFET™ II Power MOSFET in SO-8 package

Datasheet — production data

Features

Order code	V _{DSS}	R _{DS(on)}	I _D
STS12NF30L	30 V	< 0.009 Ω	12 A

- Standard outline for easy automated surface mount assembly
- Low threshold drive

Applications

Switching application

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

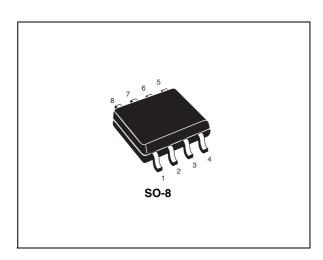


Figure 1. Internal schematic diagram

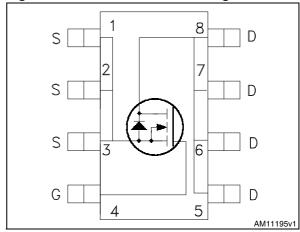


Table 1. Device summary

Order code	Marking	Package	Packaging
STS12NF30L	12F30L	SO-8	Tape and reel

Contents STS12NF30L

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STS12NF30L Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate- source voltage	±16	V
I _D	Drain current (continuos) at T _C = 25 °C	12	Α
I _D	Drain current (continuos) at T _C = 100 °C	7.5	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	48	Α
P _{TOT}	Total dissipation at T _a = 25 °C	2.5	W
T _J	Maximum operating junction temperature	150	°C
T _{stg}	Storage temperature	-55 to 150	°C

^{1.} Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-a} (1)	Thermal resistance junction-ambient max	50	°C/W

^{1.} When mounted on FR-4 board of 1inch 2 , 2oz Cu, t < 10 sec

Electrical characteristics STS12NF30L

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
lass	Zero gate voltage	V _{DS} = 30 V			1	μΑ
I _{DSS}	Drain current (V _{GS} = 0)	V _{DS} = 30 V, T _C =125 °C			10	μΑ
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1			V
R _{DS(on)}	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 6 \text{ A}$		0.008 0.01	0.009 0.011	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance			2400		pF
C _{oss}	Output capacitance	$V_{DS} = 25 \text{ V, f} = 1 \text{ MHz,}$	-	590		pF
C _{rss}	Reverse transfer capacitance	V _{GS} = 0		200		pF
Qg	Total gate charge	V _{DD} = 24 V, I _D = 12 A,		35	50	nC
Q_gs	Gate-source charge	$V_{DD} = 24 \text{ V}, I_D = 12 \text{ A},$ $V_{GS} = 4.5 \text{ V}$	-	9		nC
Q_{gd}	Gate-drain charge	(see Figure 13)		18		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time Rise time	$V_{DD} = 15 \text{ V}, I_{D} = 6 \text{ A},$ $R_{G} = 4.7 \Omega$	-	35 90	-	ns ns
t _{d(off)}	Turn-off-delay time Fall time	V _{GS} = 4.5 V (see Figure 12)	-	80 35	-	ns ns
t _{r(Voff)} t _f t _c	Off-voltage rise time fall time cross-over time	V_{DD} =24 V, I_D =12 A, R_G =4.7 Ω , V_{GS} =4.5 V (see Figure 14)	-	35 35 80	1	ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current				12	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		48	Α
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 12 \text{ A}, V_{GS} = 0$	-		1.3	٧
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 12 \text{ A}, V_{DD} = 15 \text{ V}$ di/dt = 100 A/ μ s, $T_j = 150 ^{\circ}\text{C}$ (see Figure 14)	-	114 456 8		ns nC A

^{1.} Pulse width limited by safe operating area.

^{2.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%

Electrical characteristics STS12NF30L

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

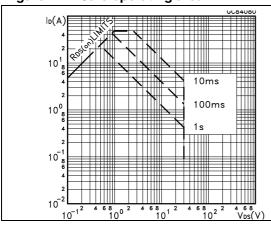


Figure 3. Thermal impedance

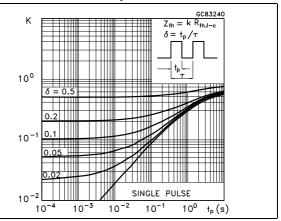


Figure 4. Output characteristics

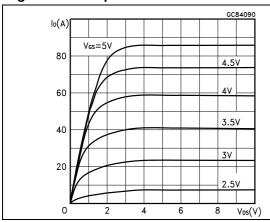


Figure 5. Transfer characteristics

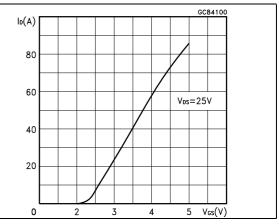
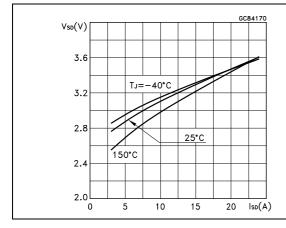


Figure 6. Source-drain diode forward characteristics

Figure 7. Static drain-source on resistance



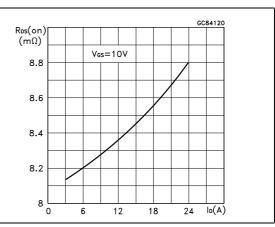
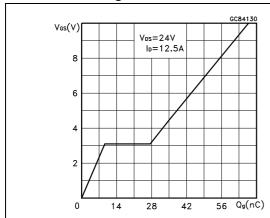


Figure 8. Gate charge vs. gate-source voltage

Figure 9. **Capacitance variations**



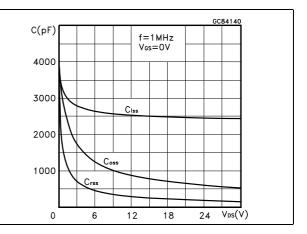
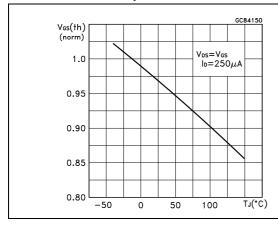
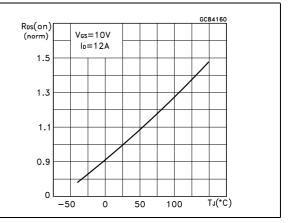


Figure 10. Normalized gate threshold voltage Figure 11. Normalized on-resistance vs. vs. temperature

temperature





Test circuit STS12NF30L

3 Test circuit

Figure 12. Switching times test circuit for resistive load

Figure 13. Gate charge test circuit

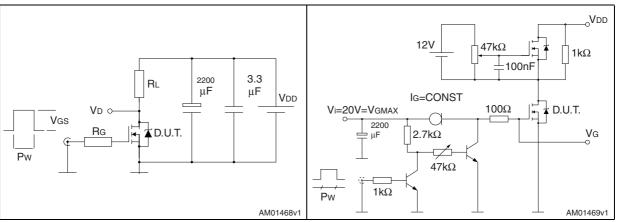


Figure 14. Test circuit for inductive load switching and diode recovery times

Figure 15. Unclamped Inductive load test circuit

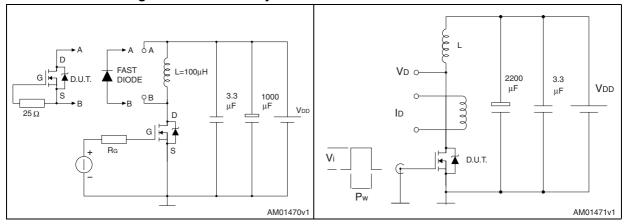
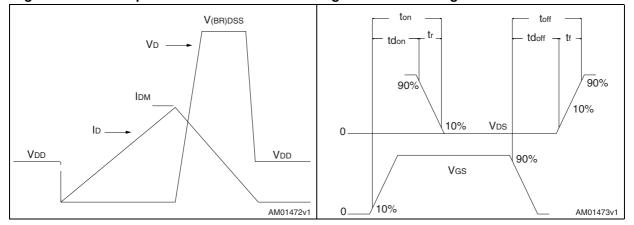


Figure 16. Unclamped inductive waveform

Figure 17. Switching time waveform



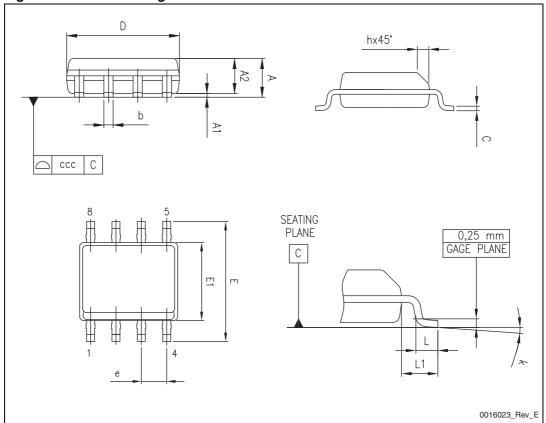
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. SO-8 mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
Α			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
С	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
е		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc	_		0.10

Figure 18. SO-8 drawing



Revision history STS12NF30L

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
09-Sep-2004	6	Complete version
17-Aug-2006	7	New template, no content change
31-Jan-2007	8	Typo mistake on <i>Table 2</i> .
08-May-2007	9	Mistake on Table 7
14-Mar-2012	10	Table 1: Device summary has been corrected. Minor text changes.

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