PRELIMINARY

CYW43903

WICED™ IEEE 802.11 a/b/g/n SoC with an Embedded Applications Processor

General Description

The Cypress CYW43903 embedded wireless system-on-a-chip (SoC) is uniquely suited for Internet-of-Things applications. It supports all rates specified in the IEEE 802.11 b/g/n specifications.The device includes an ARM Cortex-based applications processor, a single stream IEEE 802.11n MAC/baseband/radio, a power amplifier (PA), and a receive low-noise amplifier (LNA). It also supports optional antenna diversity for improved RF performance in difficult environments.

The CYW43903 is an optimized SoC targeting embedded Internet-of-Things applications in the industrial and medical sensor, home appliance markets. Using advanced design techniques and process technology to reduce active and idle power, the device is designed for embedded applications that require minimal power consumption and a compact size.

The device includes a PMU for simplifying system power topology and allows for direct operation from a battery while maximizing battery life.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM43903	CYW43903
BCM43903KRFBG	CYW43903KRFBG

Features

Application Processor Features

- ARM Cortex-R4 32-bit RISC processor.
- 1 MB of on-chip SRAM for code and data.
- DDR3/DDR3L SDRAM
- An on-chip cryptography core
- 640 KB of ROM containing WICED SDK components such as RTOS and TCP/IP stack.
- 17 GPIOs supported.
- Q-SPI serial flash interface to support up to 40 Mbps of peak transfer.
- Support for UART (3), SPI or BSC master, interfaces. (Broadcom Serial Control (BSC) is an I^2C-compatible interface.)
- Dedicated fractional PLL for audio clock (MCLK) generation.
- USB 2.0 host and device modes.
- HSIC interface support.
- SDIO 3.0 host and device modes.

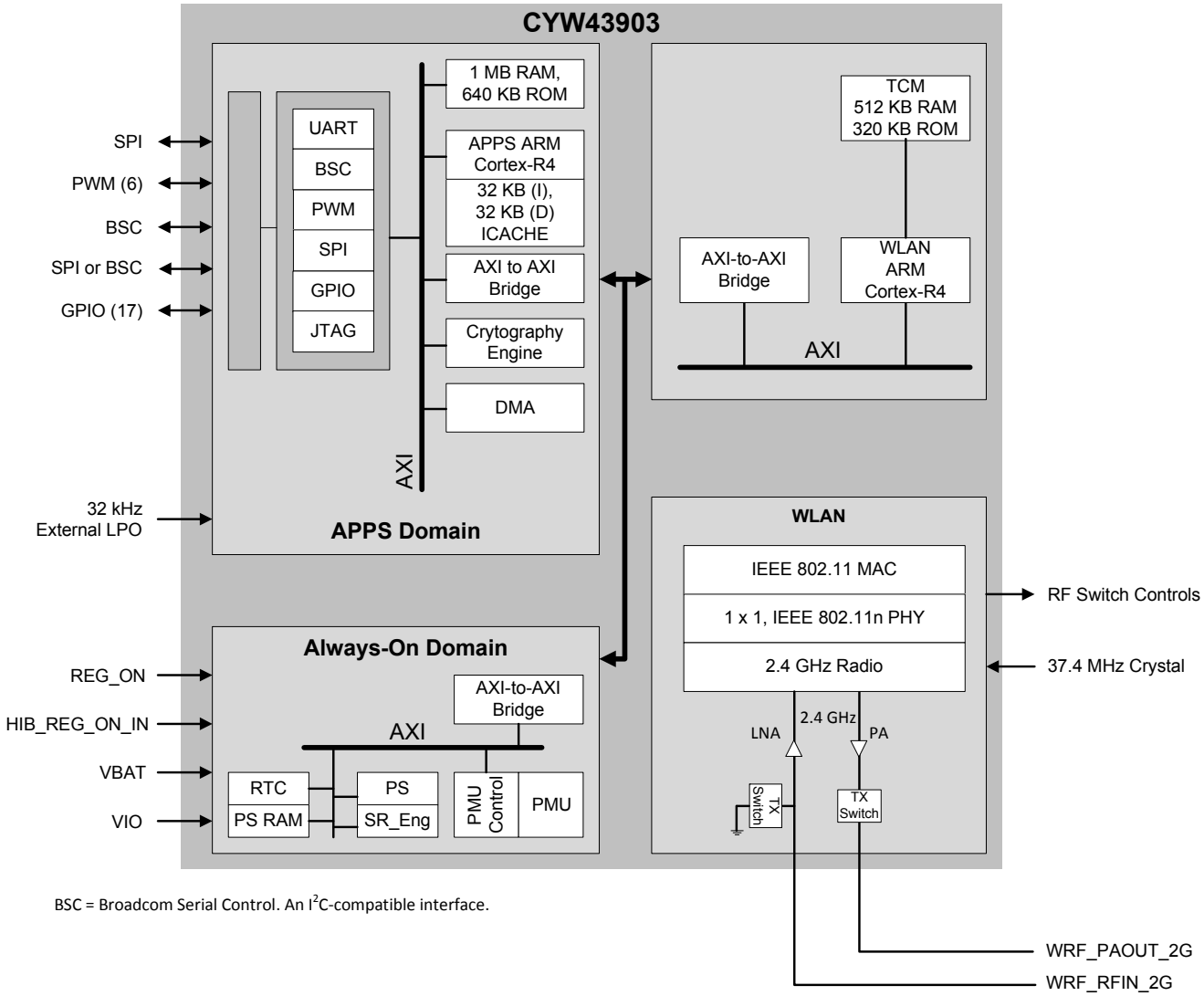
Key IEEE 801.11x Features

- IEEE 802.11n compliant.
- Single-stream spatial multiplexing up to 150 Mbps.
- Supports 20 MHz channels with optional SGI.
- Full IEEE 802.11 b/g legacy compatibility with enhanced performance.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- On-chip power and low-noise amplifiers.
- An internal fractional nPLL allows support for a wide range of reference clock frequencies.
- Integrated ARM Cortex-R4 processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions (to further minimize power consumption while maintaining the ability to upgrade to future features in the field).
- Software architecture supported by standard WICED SDK allows easy migration from existing discrete MCU designs and to future devices.
- Security support:
  - WPA and WPA2 (Personal) support for powerful encryption and authentication.
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility.
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, and CCX 5.0).
  - Wi-Fi Protected Setup and Wi-Fi Easy-Setup
- Worldwide regulatory support: Global products supported with worldwide design approval.

General Features

- Supports battery voltage range from 3.0V to 4.8V with an internal switching regulator.
- Programmable dynamic power management.
- 6 Kb OTP memory for storing board parameters.
- 338-ball FCFBGA (10mm × 10mm, 0.4 mm pitch).

Figure 1. Functional Block Diagram



BSC = Broadcom Serial Control. An I^2C-compatible interface.

Contents

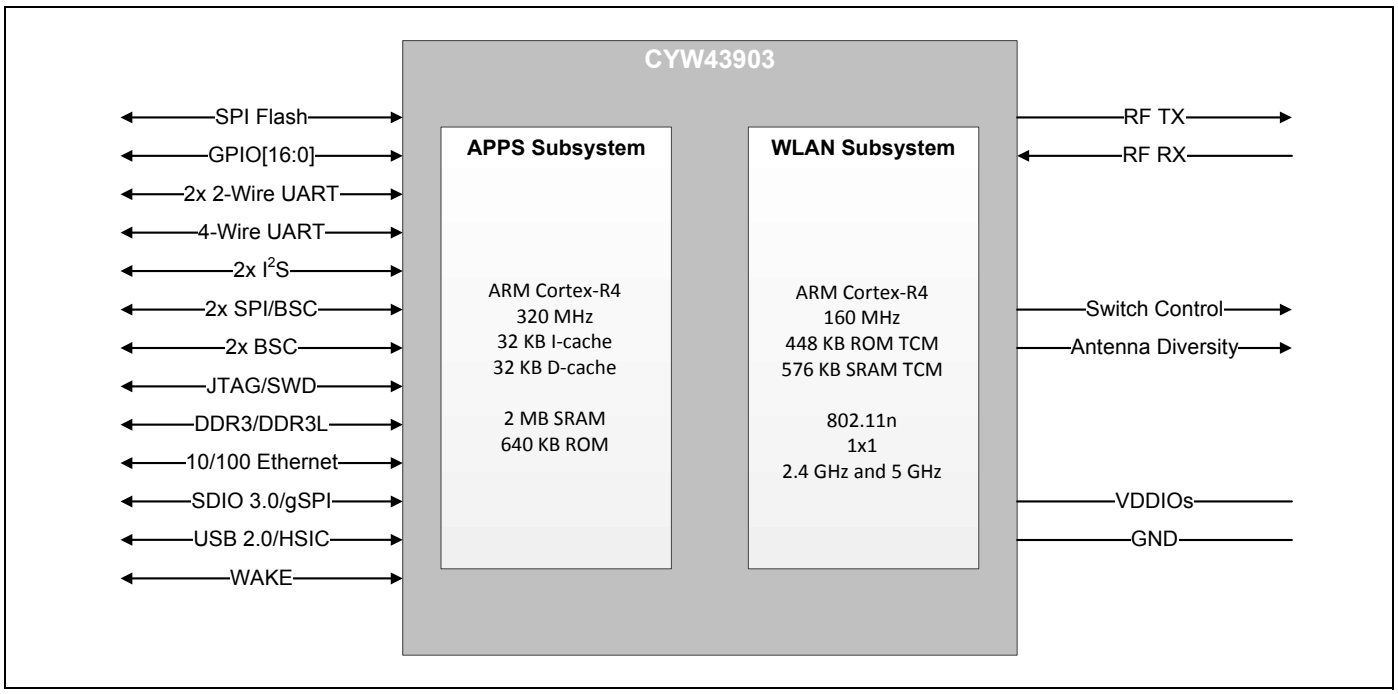
1. Overview

1.1 Introduction

The Cypress CYW43903 is a single-chip device that provides the highest level of integration for an embedded system-on-a-chip with integrated IEEE 802.11 a/b/g/n MAC/baseband/radio and a separate ARM Cortex-R4 applications processor. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for an embedded system with flexibility in size, form, and function. Comprehensive power management circuitry and software ensure that the system can meet the needs of highly embedded systems that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the CYW43903 and their associated external interfaces, which are described in greater detail in Applications Subsystem External Interfaces.

Figure 2. Block Diagram and I/O



1.1.1 Features

The CYW43903 supports the following features:

- ARM Cortex-R4 clocked at 160 MHz (in 1× mode) or up to 320 MHz (in 2× mode).
- 1 MB of SRAM and 640 KB ROM available for the applications processor.
- One high-speed 4-wire UART interface with operation up to 4 Mbps.
- Two low-speed 2-wire UART interfaces multiplexed on general purpose I/O (GPIO) pins.
- Two dedicated BSC[1] interfaces.
- Two SPI master/slave interfaces with operation up to 24 MHz.

Note: Either or both of the SPI interfaces can be used as BSC master interfaces. This is in addition to the two dedicated BSC interfaces.

1.Broadcom Serial Control (BSC) is an I2C-compatible interface.

- One SPI master interface for serial flash.
- Six dedicated PWM outputs.
- Two I^2S interfaces.
- 17 GPIOs.
- IEEE 802.11 a/b/g/n 1×1 2.4 GHz and 5 GHz radio.
- Single- and dual-antenna support.

1.2 Standards Compliance

The CYW43903 supports the following standards:

- IEEE 802.11n
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i
- Security:
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (hardware accelerator)
  - TKIP (hardware accelerator)
  - CKIP (software support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
  - WFAEC

The CYW43903 supports the following additional standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
- IEEE 802.11e QoS enhancements (already supported as per the WMM specification)
- IEEE 802.11i MAC enhancements
- IEEE 802.11k radio resource measurement

2. Power Supplies and Power Management

2.1 Power Supply Topology

One core buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW43903. All regulators are programmable via the PMU. These blocks simplify power supply design for application and WLAN functions in embedded designs.

A single VBAT (3.0V to 4.8V DC maximum) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW43903.

The REG_ON control signal is used to power up the regulators and take the appropriate sections out of reset. The CBUCK, CLDO, LNLDO, and other regulators power up when any of the reset signals are deasserted. All regulators are powered down only when REG_ON is deasserted. The regulators may be turned off/on based on the dynamic demands of the digital baseband.

The CYW43903 provides a low power-consumption mode whereby the CBUCK, CLDO, and LNLDO regulators are shut down. When in this state, the low-power linear regulator (LPLDO1) supplied by the system VIO supply provides the CYW43903 with all required voltages.

2.2 CYW43903 Power Management Unit Features

The CYW43903 supports the following Power Management Unit (PMU) features:

- VBAT to 1.35Vout (550 mA maximum) core buck (CBUCK) switching regulator
- VBAT to 3.3Vout (450 mA maximum) LDO3P3
- 1.35V to 1.2Vout (150 mA maximum) LNLDO
- 1.35V to 1.2Vout (350 mA maximum) CLDO with bypass mode for deep-sleep
- 1.35V to 1.2Vout (55 mA maximum) LDO for HSIC
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from the low power-consumption mode.

Figure 3 and Figure 4 show the regulators and a typical power topology.

Figure 3. Typical Power Topology (Page 1 of 2)

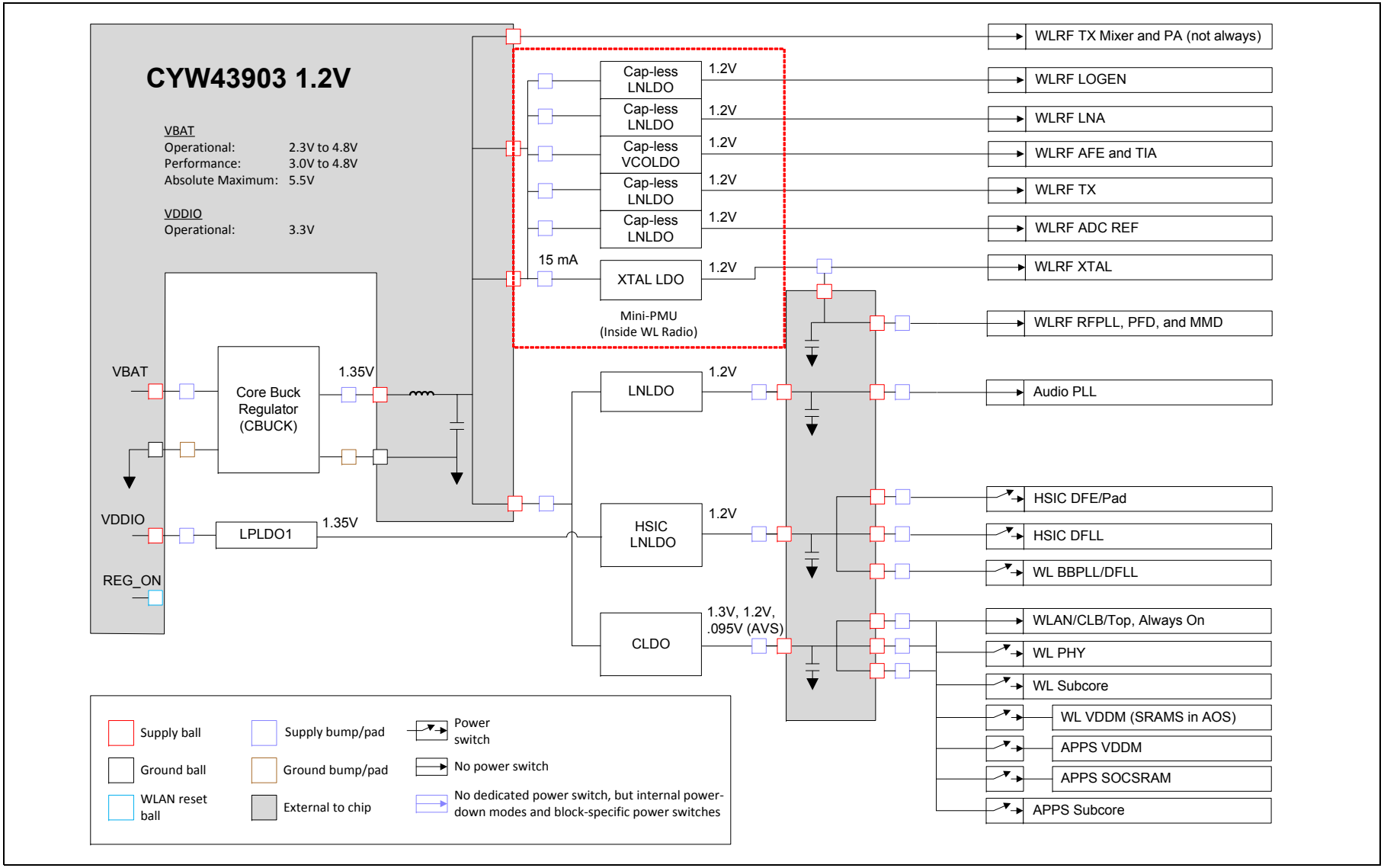
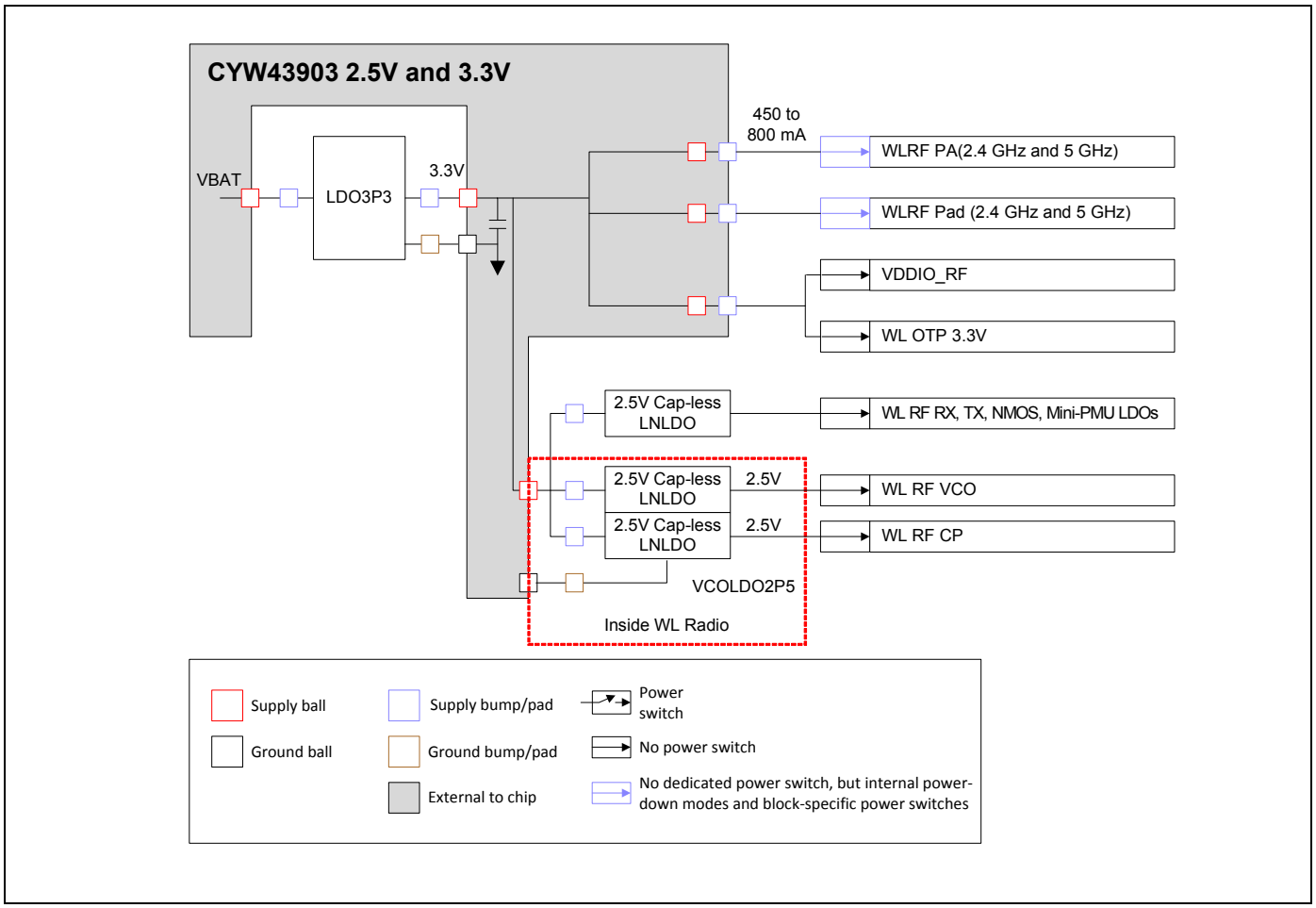


Figure 4. Typical Power Topology (Page 2 of 2)



2.3 Power Management

The CYW43903 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW43903 includes an advanced Power Management Unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW43903 into various power management states appropriate to the environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at a 32.768 kHz LPO clock) in the PMU sequencer are used to turn on and turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) as a function of the mode. Slower clock speeds are used whenever possible.

Table 2 provides descriptions for the CYW43903 power modes.

Table 2. CYW43903 Power Modes

Mode	Description
Active	All WLAN blocks in the CYW43903 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
Doze	The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW43903 remains powered up in an idle state. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to minimize active power consumption. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
Deep-sleep	Most of the chip, including both analog and digital domains and most of the regulators, is powered off. Logic states in the digital core are saved and preserved in a retention memory in the Always-On domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt, or a host resume through the USB bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
Power-down	The CYW43903 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer minimizes system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests can come from several sources: clock requests from cores, the minimum resources defined in the *ResourceMin* register, and the resources requested by any active resource-request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of the following four states:

- enabled
- disabled
- transition_on
- transition_off

The timer contains 0 when the resource is enabled or disabled and a nonzero value when in a transition state. The timer is loaded with the time_on or time_off value of the resource after the PMU determines that the resource must be enabled or disabled and decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit of the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, is no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW43903 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other system devices remain operational. When the CYW43903 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW43903 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the CYW43903, all outputs are tristated and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW43903 to be fully integrated in an embedded device while taking full advantage of the lowest power-saving modes.

When the CYW43903 is powered on from this state, it is the same as a normal power-up and does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW43903 has two signals (see Table 3) that enable or disable circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Power-Up Sequence and Timing.

Table 3. Power-Up/Power-Down/Reset Control Signals

Signal	Description
REG_ON	This signal is used by the PMU to power up the CYW43903. It controls the internal CYW43903 regulators. When this pin is high, the regulators are enabled and the device is out of reset. When this pin is low, the device is in reset and the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
HIB_REG_ON_IN	This signal is used by the hibernation block to decide whether or not to power down the internal CYW43903 regulators. If HIB_REG_ON_IN is low, the regulators will be disabled. For a signal at HIB_REG_ON_IN to function as intended, HIB_REG_ON_OUT must be connected to REG_ON.

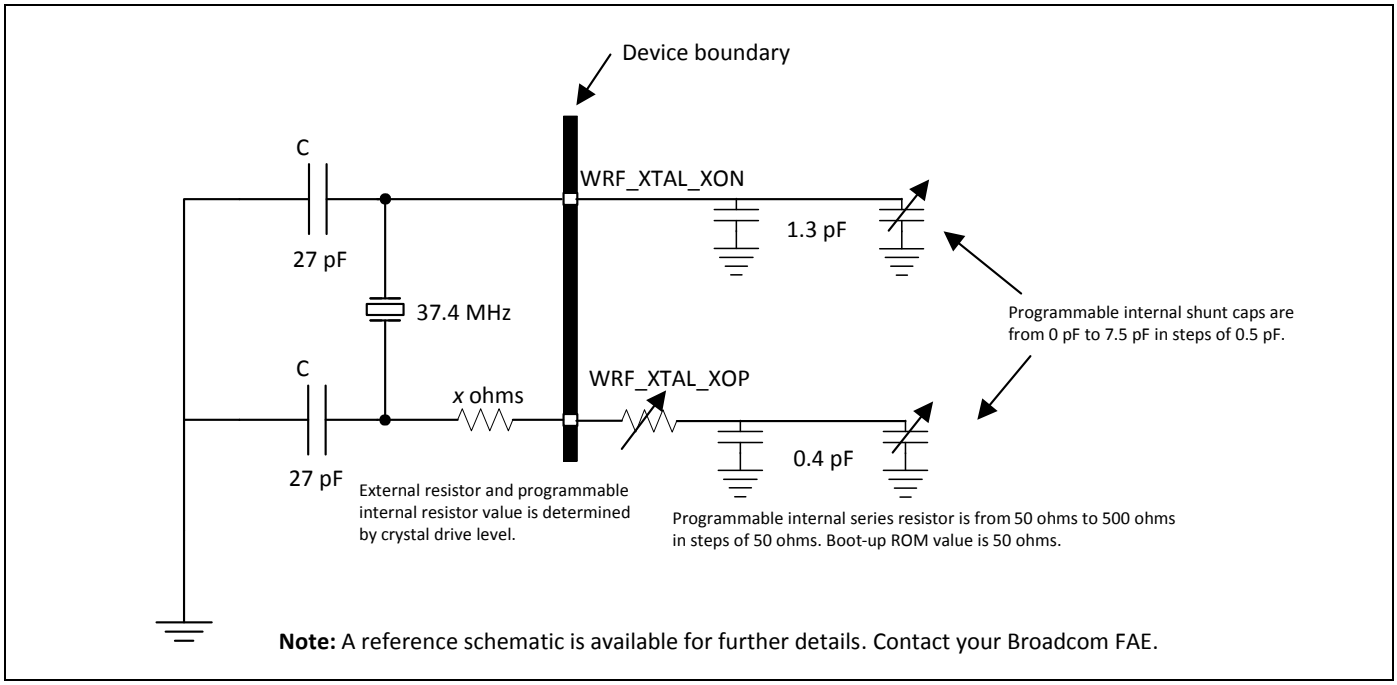
3. Frequency References

An external crystal is used for generating all radio frequencies and normal-operation clocking. As an alternative, an external frequency reference can be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW43903 can use an external crystal to provide a frequency reference. The recommended crystal oscillator configuration, including all external components, is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW43903 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal interface are listed in Table 4.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be used, provided that it meets the phase noise requirements listed in Table 4.

If used, the external clock should be connected to the WRF_XTAL_XON pin through an external 1000 pF coupling capacitor, as shown in Figure 6. The internal clock buffer connected to this pin will be turned off when the CYW43903 goes into sleep mode. When the clock buffer turns on and off, there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P35 pin.

Figure 6. Recommended Circuit to Use With an External Reference Clock

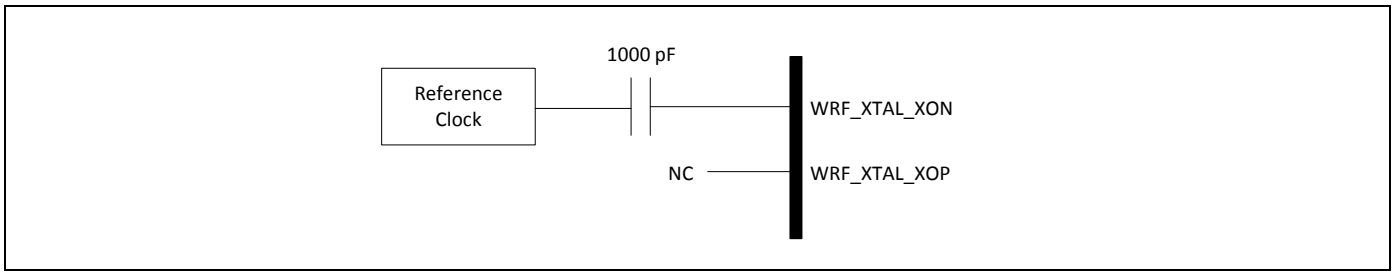


Table 4. Crystal Oscillator and External Clock—Requirements and Performance

Parameter	Conditions/Notes	Crystal[1]			External Frequency Reference[2 3]			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency	2.4 GHz band: IEEE 802.11n operation and legacy IEEE 802.11b/g operation	Between 19 MHz and 52 MHz [4]						
	5 GHz band, IEEE 802.11n operation only	19	–	52	35	–	52	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[5]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capacitance	–	–	16	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_XON)	Resistive	–	–	–	30k	100k	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
WRF_XTAL_XON Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_XON Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_XON input voltage (see Figure 6)	IEEE 802.11a/b/g operation only	–	–	–	400	–	1200	mV_{p-p}
WRF_XTAL_XON input voltage (see Figure 6)	IEEE 802.11n AC-coupled analog input	–	–	–	1	–	–	V_{p-p}
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase noise[6] (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase noise[6] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–144	dBc/Hz
Phase noise[6] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz

Table 4. Crystal Oscillator and External Clock—Requirements and Performance (Cont.)

Parameter	Conditions/Notes	Crystal[1]			External Frequency Reference[2 3]			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Phase noise[6] (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/Hz

1. (Crystal) Use WRF_XTAL_XON and WRF_XTAL_XOP.
2. See External Frequency Reference on page 13 for alternative connection methods.
3. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
4. The frequency step size is approximately 80 Hz.
5. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
6. Assumes that external clock has a flat phase noise response above 100 kHz.

3.3 Frequency Selection

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset reference frequencies of 19.2, 19.8, 24, 26, 33.6, 37.4, 38.4, and 52 MHz, but also other frequencies in this range, with approximately 80 Hz resolution. The CYW43903 must have the reference frequency set correctly in order for any of the external interfaces to function correctly, since all bit timing is derived from the reference frequency.

Note: The fractional-N synthesizer can support many reference frequencies. However, frequencies other than the default require support to be added in the driver plus additional, extensive system testing. Contact Cypress for more information.

The reference frequency for the CYW43903 may be set in the following ways:

- Set the xtalfreq=xxxxx parameter (in Hertz) in the nvram.txt file (used to load the driver) to correctly match the crystal frequency.
- Auto-detect any of the standard handset reference frequencies using an external LPO clock.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the CYW43903 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for automatic frequency detection to work correctly, the CYW43903 must have a valid and stable 32.768 kHz LPO clock that meets the requirements listed in Table 5 and is present during a power-on reset.

3.4 External 32.768 kHz Low-Power Oscillator

The CYW43903 uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one tradeoff caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 5.

Table 5. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[1]	>100k <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

1. When power is applied or switched off.

4. Applications Subsystem

4.1 Overview

The Applications subsystem contains the general use CPU, memory, the standalone DMA core, the cryptography core, and the majority of the external interfaces.

4.2 Applications CPU and Memory Subsystem

This subsystem has an integrated 32-bit ARM Cortex-R4 processor with an internal 32 KB D-cache and an internal 32 KB I-cache. The ARM Cortex-R4 is a low-power processor that features a low gate count, low interrupt latency, and low-cost debugging capabilities. It is intended for deeply embedded applications that require fast interrupt response features. The ARM Cortex-R4 implements the ARM v7-R architecture and supports the Thumb-2 instruction set.

At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on a MIPS/µW basis. It also supports integrated sleep modes.

Using multiple technologies to reduce cost, the ARM Cortex-R4 enables improved memory utilization, reduced pin overhead, and reduced silicon area. It also has extensive debugging features, including real-time tracing of program execution.

On-chip memory for the CPU includes 1 MB SRAM, 640 KB ROM, and an 8 KB RAM powered independently of the application subsystem.

4.3 Memory-to-Memory DMA Core

The CYW43903 memory-to-memory DMA (M2MDMA) engine contains eight DMA channel pairs, each containing one transmit/pull engine and one receive/push engine.

The DMA engine provides general purpose data movement between memories that can be on the device, attached directly to the device, or accessed through a host interface. The transmit/pull engine reads data from the source memory and immediately passes it to the paired receive/push engine, which proceeds to write it to the destination memory. Multiple masters can program the individual channels, and multiple interrupts are provided so that interrupts for different channels can be routed separately to different masters.

4.4 Cryptography Core

This core provides general purpose data movement between memories, which may be either on the device, attached directly to the device, or accessed through a host interface. The transmit/pull engine reads data from the source memory and passes it immediately to the paired receive/push engine that proceeds to write it to the destination memory. Multiple masters may program the individual channels, and multiple interrupts are provided so that interrupts for different channels can be routed separately to different masters.

The cryptography block provides a hardware accelerator for enciphering and deciphering data that has undergone processing using standards-based encryption algorithms. The cryptography block includes the following primary features:

- Encryption and hash engines that support single pass AUTH-ENC or ENC-AUTH processing.
- A scalable AES module that supports CBC, ECB, CTR, CFB, OFB, and XTS encryption with 128-, 192-, and 256-bit key sizes.
- A scalable DES module that supports DES and 3DES in ECB and CBC modes.
- An RC4 stream cipher module that supports state initialization, state update, and key-stream generation.
- MD5, SHA1, SHA224, and SHA256 engines that support pure hash or HMAC operations.
- A built-in 512-byte key cache for locally protected key storage.

OTP memory is used to store authentication keys.

5. Applications Subsystem External Interfaces

5.1 DDR3/DDR3L

The memory interface controls main memory accesses and provides for a maximum of 128 MB of main memory.

The CYW43903 supports a variety of SDRAM configurations. The memory controller supports ×16 and ×8 configurations with 16 multiplexed address lines. The ×8 configuration requires two devices to support 128 MB of memory.

Table 6. DDR SDRAM Controller

Feature	DDR3	DDR3L
SDRAM voltage	1.5V	1.35V
SDRAM clock (MHz)	320	320
Data rate (MHz)	640	640
Data bus width (bits)	16	16
Number of address bits	16	16
DRAM density supported[1]	Up to 16 Gb	Up to 16 Gb

1. The number of bytes that can be addressed is limited internally to 128 MB even if a denser SDRAM is supported.

5.2 Ethernet MAC Controller (MII/RMII)

The CYW43903 integrates a high performance Ethernet MAC controller. The controller interfaces to an external PHY either over a Media Independent Interface (MII) or a Reduced Media Independent Interface (RMII). The controller can transmit and receive data at 10 Mbps and 100 Mbps.

5.3 GPIO

There are 17 general-purpose I/O (GPIO) pins available on the CYW43903. The GPIOs can be used to connect to various external devices.

Upon power-up and reset, these pins are tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions.

Apart from other functions, GPIOs are used to set bootstrap options and use the JTAG interface for debugging during software development.

5.4 Broadcom Serial Control

The CYW43903 has two Cypress Serial Control (BSC[2]) master interfaces for external communication with codecs, DACs, NVRAM, etc. The I/O pads can be configured as pull-ups or pull-ups can be installed on the reference design to support a multimaster on an open drain bus.

2.Broadcom Serial Control is an I^2C compatible interface.

5.5 I²S

The CYW43903 has two I²S interfaces for audio signal data. The two interfaces are identical. Each interface supports both Master and Slave modes.

The following signals apply to the first I²S interface:

- I²S bit clock: I2S_SCLK0 (sometimes referred to as I2S_BITCLK)
- I²S word select: I2S_LRCK0 (sometimes referred to as I2S_WS)
- I²S serial data out: I2S_SDATAO0
- I²S serial data in: I2S_SDATAI0
- I²S master clock: I2S_MCLK0

The following signals apply to the second I²S interface:

- I²S bit clock: I2S_SCLK1 (sometimes referred to as I2S_BITCLK)
- I²S word select: I2S_LRCK1 (sometimes referred to as I2S_WS)
- I²S serial data out: I2S_SDATAO1
- I²S serial data in: I2S_SDATAI1
- I²S master clock: I2S_MCLK1

I²S_SDATAO0 and I2S_SDATAO1 are outputs.

I²S_MCLK, I2S_SCLK and I2S_LRCLK can be configured as either inputs or outputs depending on whether the master clock source is on- or off-chip and whether the I²S is operating in Slave or Master mode.

Channel word lengths of 16 bits, 20 bits, 24 bits, and 32 bits are supported, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit-clock cycle after the I²S_LRCK transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when I²S_LRCK is low, and right-channel data is transmitted when I²S_LRCK is high. An embedded 128 × 32-bit single-port SRAM for data processing enhances the performance of the interface.

An audio PLL generates an internal master clock (for I²S_MCLK0 and I²S_MCLK1) that provides support for various sampling rates.

Table 7 shows the MCLK rates (in MHz) associated with each of the various sample rates. In the table, FS refers to the sample rate in kHz and typical MCLK rates are shaded.

Table 7. Variable Sample Rate and MCLK Rate Support[1]

Sample Rate (kHz)	MCLK Rate (MHz)[2]							
	128 × FS	192 × FS	256 × FS	384 × FS	512 × FS	640 × FS	768 × FS	1152 × FS
8	1.024	1.536	2.048	3.072	4.096	5.12	6.144	9.216
11.025	1.4112	2.1168	2.8224	4.2336	5.6448	7.056	8.4672	12.7008
12	1.536	2.304	3.072	4.608	6.144	7.68	9.216	13.824
16	2.048	3.072	4.096	6.144	8.192	10.24	12.288	18.432
22.05	2.8224	4.2336	5.6448	8.4672	11.2896	14.112	16.9344	25.4016
24	3.072	4.608	6.144	9.216	12.288	15.36	18.432	27.648
32	4.096	6.144	8.192	12.288	16.384	20.48	24.576	36.864
44.1	5.6448	8.4672	11.2896	16.9344	22.5792	28.224	33.8688	–
48	6.144	9.216	12.288	18.432	24.576	30.72	36.864	–
64	8.192	12.288	16.384	24.576	32.768	–	–	–
88.2	11.2896	16.9344	22.5792	33.8688	–	–	–	–
96	12.288	18.432	24.576	36.864	–	–	–	–
192	24.576	36.864	–	–	–	–	–	–

1. All data in the table assumes a crystal frequency of 37.4 MHz.

2. MCLK frequency errors are less than 1 ppb.

For an MCLK specification, see Table 48.

An external MCLK source can be provided to the device instead of using the internal MCLK source.

The CYW43903 needs an external clock source input on the slave clock pin for the I^2S interface to work properly in Slave mode. The slave clock frequency is dependent upon the audio sample rate and the external I^2S codec.

5.6 JTAG and ARM Serial Wire Debug

The CYW43903 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

The CYW43903 also supports ARM Serial Wire Debug (SWD) for connecting a JTAG debugger directly to both ARM Cortex-R4s. For SWD, the combination of a clock and a bidirectional signal (on a single pin) provides normal JTAG debug and test functionality. The reduced pin-count SWD interface is a high-performance alternative to the JTAG interface.

Table 8 shows the JTAG_SEL and TAP_SEL states for test and debug function selection. Test and debug function selection is independent of the debugging interface (JTAG or SWD) being used.

Table 8. JTAG_SEL and TAP_SEL States for Test and Debug Function Selection

JTAG_SEL State	TAP_SEL State	Test and Debug Function
0	0	JTAG not used.
0	1	JTAG not used.
1	0	Access the LV tap directly for ATE and bring-up.
1	1	Access either of the ARM Cortex-R4's directly via either the 5-pin JTAG port or the 2-pin SWD configuration.

5.7 PWM

The CYW43903 provides up to six independent pulse width modulation (PWM) channels. The following features apply to the PWM channels:

- Each channel is a square wave generator with a programmable duty cycle.
- Each channel generates its duty cycle by dividing down the input clock.
- Both the high and low duration of the duty cycle can be divided down independently by a 16-bit divider register.
- Each channel can work independently or update simultaneously.
- Pairs of PWM outputs can be inverted for devices that need a differential output.
- Continuous or single pulses can be generated.
- The input clock can either be a high-speed clock from a PLL channel or a lower speed clock at the crystal frequency.

5.8 Real-Time Clock

The CYW43903 provides a real-time clock (RTC) provided that an accurate 32.768 kHz crystal is used. The RTC generates date/time using the 32.768 kHz reference and is always powered on when the chip is on, except while in Hibernation mode.

The RTC has a precision of seconds and will display the calendar day and time provided the initial start time is programmed correctly. The second, minute, hour, day, month, year, and 24-hour mode can be set individually.

Interrupts can be set on any periodic time event or on specific time events. The PMU uses the RTC interrupt to determine when to wake up the chip.

5.9 SDIO 3.0

5.9.1 SDIO 3.0—Device Mode

Description

The CYW43903 WLAN section supports SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
- HS: High-speed up to 50 MHz (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).

Note: The CYW43903 is backward compatible with SDIO v2.0 host interfaces.

The following three functions are supported:

- Function 0 Standard SDIO function (max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal SoC address space (max. BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (max. BlockSize/ByteCount = 512B)

SDIO Pins

Table 9. SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Figure 7. Signal Connections to an SDIO Host (SD 4-Bit Mode)

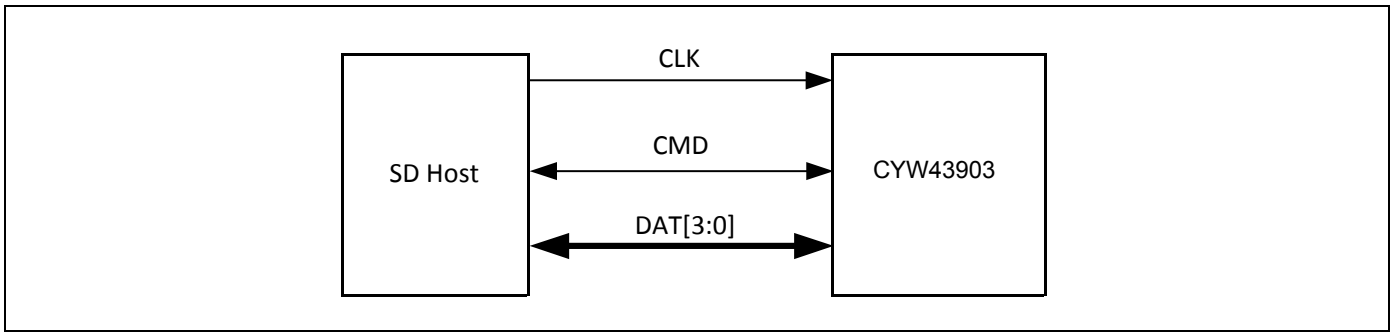
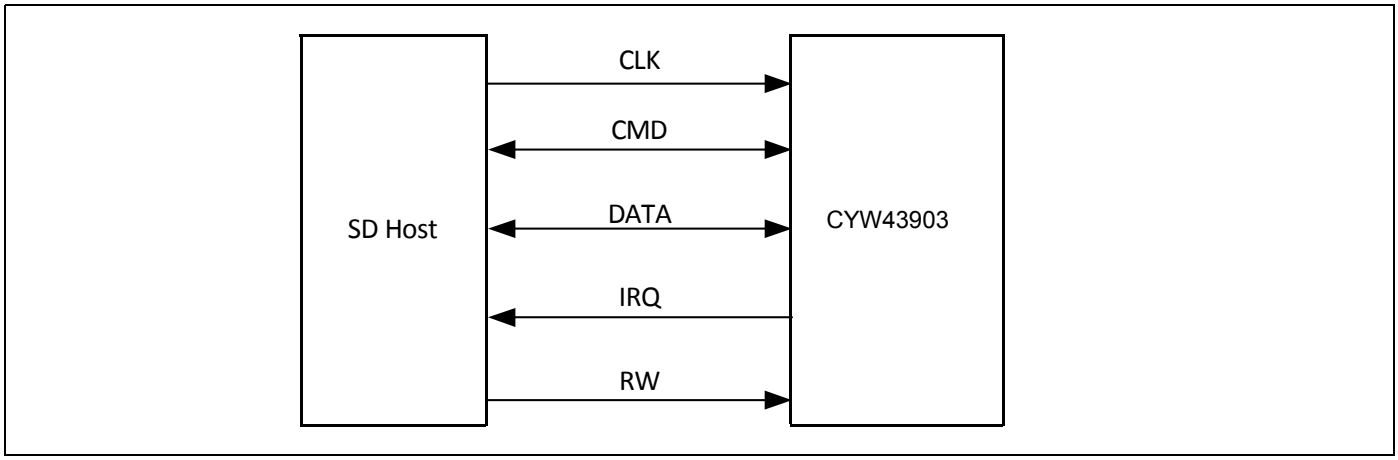


Figure 8. Signal Connections to an SDIO Host (SD 1-Bit Mode)



Note: Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four data (DATA) lines and the command (CMD) line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups

5.9.2 SDIO 3.0—Host Mode

The CYW43903 WLAN section supports SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
- HS: High-speed up to 50 MHz (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).

Note: The CYW43903 is backward compatible with SDIO v2.0 devices.

In this mode, the device supports the following features:

- ADMA2.
- Out-of-band signaling for card detection, write protection, and I/O voltage levels (which are available on GPIOs).
- Dynamic, specification-compliant shifting from 3.3V to 1.8V I/Os.

5.10 S/PDIF

S/PDIF is a serial audio data transport format used to connect consumer audio devices such as CD players, DVD players, and surround-sound receivers. Although S/PDIF can be used to transport uncompressed audio formats, the primary use case for the CYW43903 S/PDIF interface is to transport multichannel compressed audio for surround-sound applications, especially Dolby Digital and DTS, to an auxiliary external audio processor.

The CYW43903 can support two S/PDIF interfaces via the I2S_SDATA00 and I2S_SDATA01 pins. Because each S/PDIF interface uses an I^2S data line, only I^2S or S/PDIF functionality can be enabled on each I^2S interface.

Each S/PDIF interface has the following key requirements:

- S/PDIF transmissions that conform with IEC 60958-1 (receiver not required).
- Support for linear PCM audio data that conforms with IEC 60948-3.
- Support for nonlinear PCM audio data that conforms with IEC 60948-3.
- Support for priority payload formats that include IEC 61937-3 (AC-3) and IEC 61937-5 (DTS).
- Support for sample rates from 32 kHz to 192 kHz.
- Support for 16, 20, and 24-bit audio samples.
- Support for only one concurrent compressed audio stream.

5.11 SPI Flash

The SPI flash interface supports the following features:

- A SPI-compatible serial bus.
- An 80 MHz (maximum) clock frequency.
- Quad I/O, which provides increased throughput to 40 MB/s.
- Support for either ×1 or ×4 addresses with ×4 data.
- 3-bytes and 4-byte addressing modes.
- A configurable dummy-cycle count that is programmable from 1 to 15.
- Programmable instructions output to serial flash.
- An option to change the sampling edge from rising-edge to falling-edge for read-back data when in high-speed mode.

5.12 UART

A high-speed 4-wire CTS/RTS UART interface can be enabled by software and has dedicated pins. Provided primarily for debugging during development, this UART enables the CYW43903 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART and provides a FIFO size of 64 × 8 in each direction.

There are two low-speed UART interfaces on the CYW43903. Each functions as a standard 2-wire UART. They are also enabled as alternate functions on GPIOs and can be enabled independently of the 4-wire fast UART.

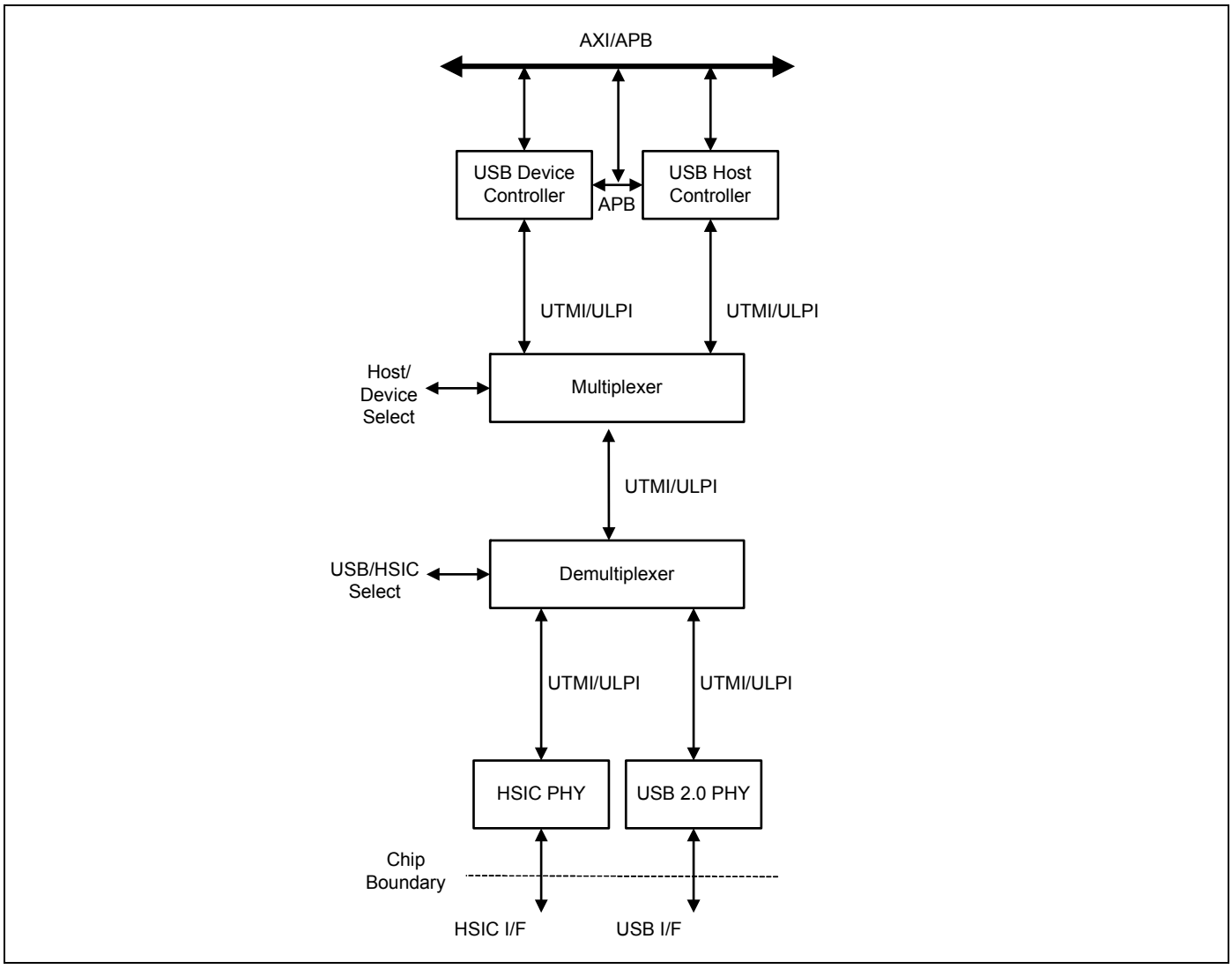
5.13 USB 2.0/HSIC

5.13.1 Overview

The USB 2.0 host controller (HC) and device controller (DC) interface to a backplane via Advanced eXtensible Interface (AXI) and Advanced Peripheral Bus (APB). They interface externally through a USB 2.0 and HSIC interfaces.

Figure 9 shows the topology of the USB 2.0 and HSIC cores.

Figure 9. Topology of the USB 2.0 and HSIC Cores



The CYW43903 contains both a USB 2.0 HC and DC. Therefore, it can operate in the host-only, device-only, and dual-role device (DRD) modes. In DRD mode, the CYW43903 can be configured as either the host or a device on the fly but must remain in the same mode until the next boot cycle. The restriction that the host or device mode remains fixed during a boot cycle is what differentiates DRD from On-the-Go (OTG).

The state of the GPIO_9 strap option selects the PHY type as either USB 2.0 or HSIC. The state of the USB2_DSEL pin sets the mode as either host or device for USB Type A and Type B connectors. For a USB Micro-AB connector, the USB2_DSEL pin sets the mode as either host or device while the overall mode is DRD.

Table 10 shows the five application cases supported, the USB mode and PHY type associated with each case, and the connector type as well as the USB2_DSEL and GPIO_9 states associated with each case.

Table 10. USB Application Cases

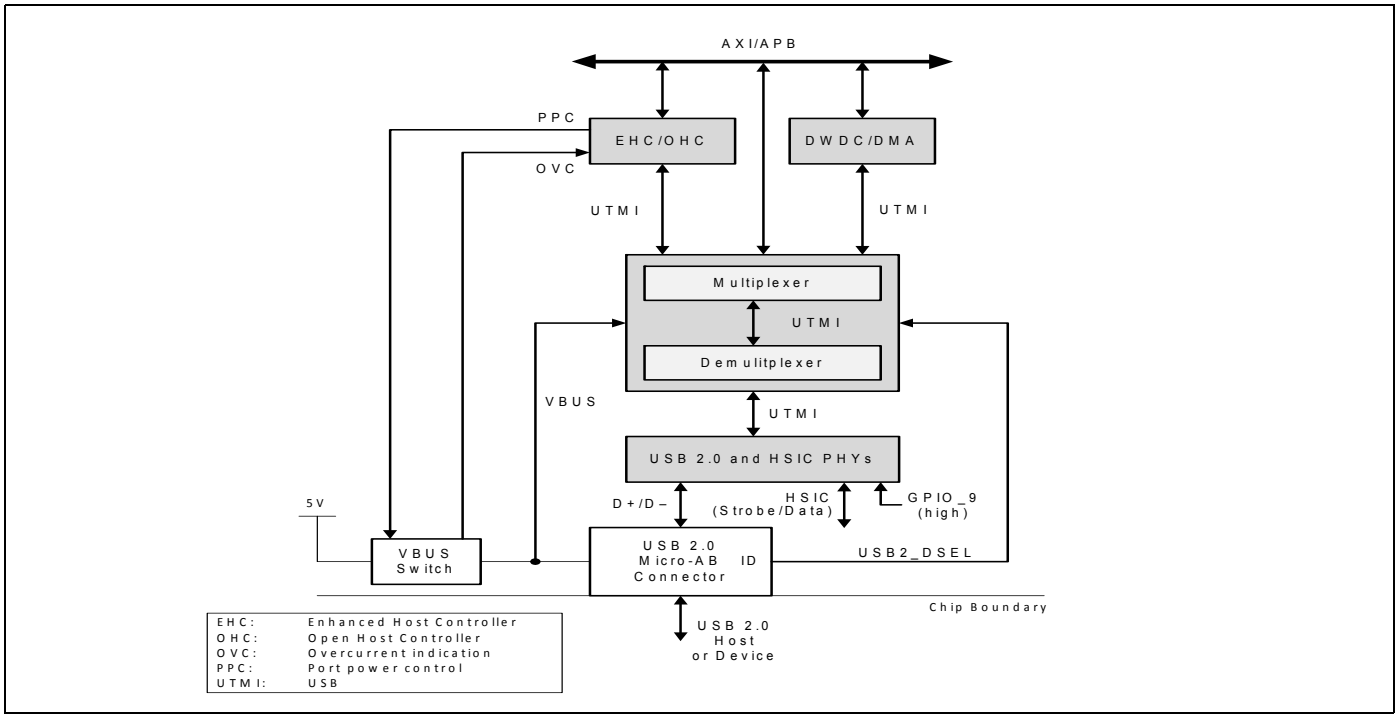
Application Case Shorthand	Mode	PHY	Pin States		Connector Information
			USB2_DSEL	GPIO_9	
DRD + USB 2.0 PHY	DRD-Host	USB 2.0	0	1	Type: Micro-AB Connect USB2_DSEL to the ID pin of the Micro-AB receptacle.
	DRD-Device	USB 2.0	1	1	
Host + USB 2.0 PHY	Host	USB 2.0	0	1	Type A
Device + USB2.0 PHY	Device	USB 2.0	1	1	Type B
Host + HSIC PHY	Host	HSIC	0	0	–
Device + HSIC PHY	Device	HSIC	1	0	–

Note: The combination of DRD + HSIC PHY does not exist because there is nothing that corresponds to the ID pin on the Micro-AB connector for an HSIC PHY.

Note: In host mode, the USB core can process an overcurrent event and take the appropriate action. The overcurrent event is input into the CYW43903 via the alternative mode pin USB20H_CTL.

Figure 10 shows the CYW43903 configured to operate in DRD mode with a USB 2.0 PHY.

Figure 10. CYW43903 Configured as a DRD + USB 2.0 PHY



The following information pertains to Figure 10:

- The Micro-AB receptacle connects the CYW43903 to an external host or device.
- The Micro-AB connector ID pin is connected to the CYW43903 USB2_DSEL pin.
- The CYW43903 GPIO_9 pin is high in order to select the USB 2.0 PHY.
- The PPC line indicates whether the USB 2.0 host controller supports port power control.
- The OVC line is used to indicate an overcurrent condition.
- Standard differential signal lines D+ (DP) and D– (DM) are used for the USB 2.0 interface
- Strobe and Data are used for the HSIC interface.

5.13.2 USB 2.0 Features

The following capabilities and features apply to the CYW43903 USB 2.0 PHY:

- Compliant with the UTMI+ level 2 specification.
- Functions as a host, device, or OTG PHY.
- Supports high speed (HS) at 480 Mbps, full speed (FS) at 12 Mbps, and low speed (LS) at 1.5 Mbps.
- Integrates pull-up and pull-down terminations with resistor support (per an engineering change notice to the USB 2.0 specification).
- Contains a calibrated 45Ω termination for HS TX/RX.
- Uses half-duplex differential data signaling with NRZI encoding.
- Recovers the data and clock from the data stream.
- Integrates a 960 MHz PLL with a single-ended reference clock.
- Supports host resume and remote wake-up.
- Supports L1 and L2 suspend, shallow sleep, and Link-Power Management (LPM).
- Supports legacy USB 1.1 devices through a serial interface.
- Supports dribble bits.
- Supports LS keep-alive packets (LS EOP).
- Support HS keep-alive packets (HS SYNC).
- Contains an onboard BERT for self-testing (PRBS and fixed patterns).
- Dissipates a maximum power of 150 mW for 1-port in loop-back mode.
- Contains an integrated 3.3V to 1.2V LDO.
- Uses 3.3V.

5.13.3 HSIC Features

The following capabilities, features, and limitations apply to the CYW43903 HSIC PHY:

- Supports chip-to-chip connections.
- Supports high-speed USB data rates.
- Supports a maximum trace length of 10 cm.
- Does not support hot plug and play.
- There is no chirping because the interface defaults to high-speed operation.
- 1.2V DDR signaling is used.
- Except for the two 1.2V pads, supply pads, and the PLL, the PHY uses purely digital logic.
- The PHY consumes low power.
- Supports powering of the host or peripheral in any order.

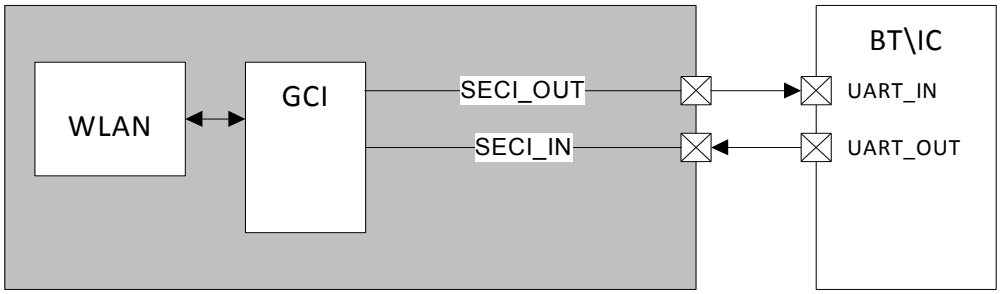
6. Global Functions

6.1 External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external colocated wireless device, such as Bluetooth, to manage wireless medium sharing for optimum performance.

Figure 11 shows the coexistence interface.

Figure 11. Cypress 2-Wire External Coexistence Interface



NOTES:

- SECI_OUT/BT_TXD and SECI_IN/BT_RXD are multiplexed on the GPIOs.
- The 2-wire coexistence interface is intended for future compatibility with the BT SIG 2-wire interface that is being standardized for Core 4.1.

6.2 One-Time Programmable Memory

Various hardware configuration parameters can be stored in an internal 6144-bit (768 bytes) One-Time Programmable (OTP) memory that is read by system software after a device reset. In addition, customer-specific parameters, including the system vendor ID and MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP memory device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP memory array can be programmed in a single write-cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits that are still in the 0 state can be altered during each programming cycle.

Prior to OTP memory programming, all values should be verified using the appropriate editable nvram.txt file. The nvram.txt file is provided with the reference board design package.

6.3 Hibernation Block

The Hibernation (HIB) block is a self-contained power domain that can be used to completely shut down the rest of the CYW43903. This optional block uses the HIB_REG_ON_OUT pin to drive the REG_ON pin. Therefore, for the HIB block to work as designed, the HIB_REG_ON_OUT pin must be connected to the REG_ON pin. To use the HIB block, software programs the HIB block with a wake count and then asserts a signal indicating that the chip should be put into hibernation. After assertion, the HIB block drives HIB_REG_ON_OUT low for the number of 32 kHz clock cycles programmed as the wake count. After the wake-count timer expires, HIB_REG_ON_OUT is driven high. Other than the logic state of the HIB block, no state is saved in the CYW43903 during hibernation.

6.4 System Boot Sequence

The following general sequence occurs after a CYW43903 is powered on:

1. Either REG_ON or HIB_REG_ON_IN is asserted.

Note: For HIB_REG_ON_IN to function as intended, HIB_REG_ON_OUT must be connected to REG_ON.

2. The core LDO (CLDO) and LDO3P3 outputs stabilize.
3. The OTP memory bits are used to initialize various functions, such as PMU trimming, package selection, memory size selection, etc.
4. The APP and WLAN cores are powered up.
5. The XTAL is powered up.
6. The APP and WLAN CPU bootup sequences start.

7. Wireless LAN Subsystem

7.1 WLAN CPU and Memory Subsystem

The CYW43903 WLAN section includes an integrated 32-bit ARM Cortex-R4 processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features a low gate count, a small interrupt latency, and low-cost debug capabilities. It is intended for deeply embedded applications that require fast interrupt response features. Delivering more than a 30% performance gain over ARM7TDMI, the ARM Cortex-R4 implements the ARM v7-R architecture with support for the Thumb-2 instruction set.

At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It also supports integrated sleep modes.

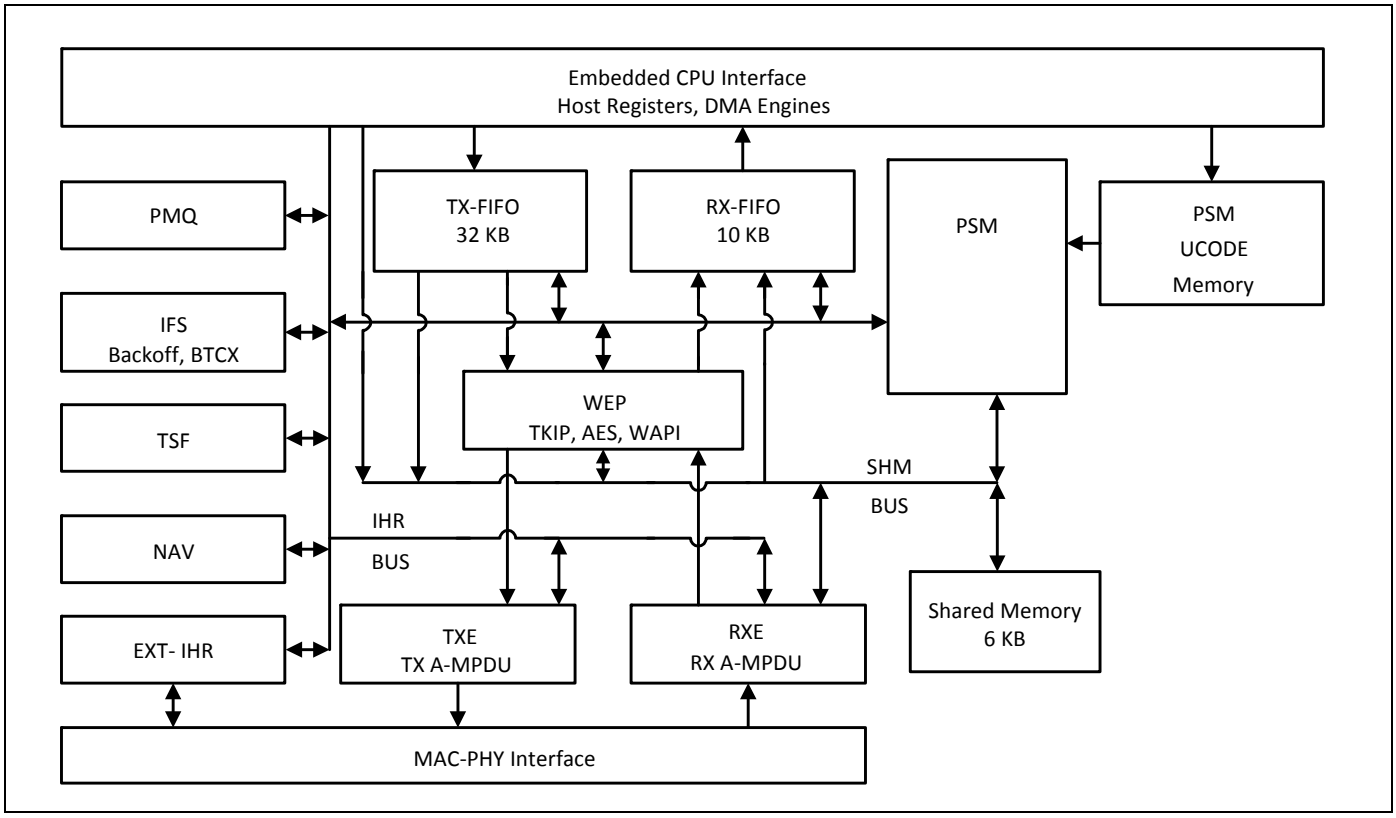
On-chip memory for this CPU includes 576 KB of SRAM and 448 KB of ROM.

7.2 IEEE 802.11n MAC

The CYW43903 WLAN media access controller (MAC) is designed to support high-throughput operation with low power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power-saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 12.

The following sections provide an overview of the important MAC modules.

Figure 12. WLAN MAC Architecture



The CYW43903 WLAN MAC supports features specified in the IEEE 802.11 base standard and amended by IEEE 802.11n. The key MAC features include:

- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT).
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP), and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Support for coexistence with Bluetooth and other external radios.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality.
- Statistics counters for MIB support.

7.2.1 PSM

The programmable state machine (PSM) is a microcoded engine that provides most of the low-level control to the hardware in order to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow-control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, allowing algorithms to be optimized very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are colocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations, the operands are obtained from shared memory, scratch-pad memory, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad memory, or IHRs.

There are two basic branch instructions: conditional branches and ALU-based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs) or on the results of ALU operations.

7.2.2 WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform encryption and decryption as well as MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to use. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the transmit engine (TXE) to encrypt and compute the MIC on transmit frames and the receive engine (RXE) to decrypt and verify the MIC on receive frames.

7.2.3 TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with the WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel-access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC has multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

7.2.4 RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

7.2.5 IFS

The IFS module contains the timers required to determine interframe-space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe-spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. When the timer expires, the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration, ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

7.2.6 TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

7.2.7 NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

7.2.8 MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface that can be controlled either by the host or the PSM to configure and control the PHY.

7.3 IEEE 802.11™ a/b/g/n PHY

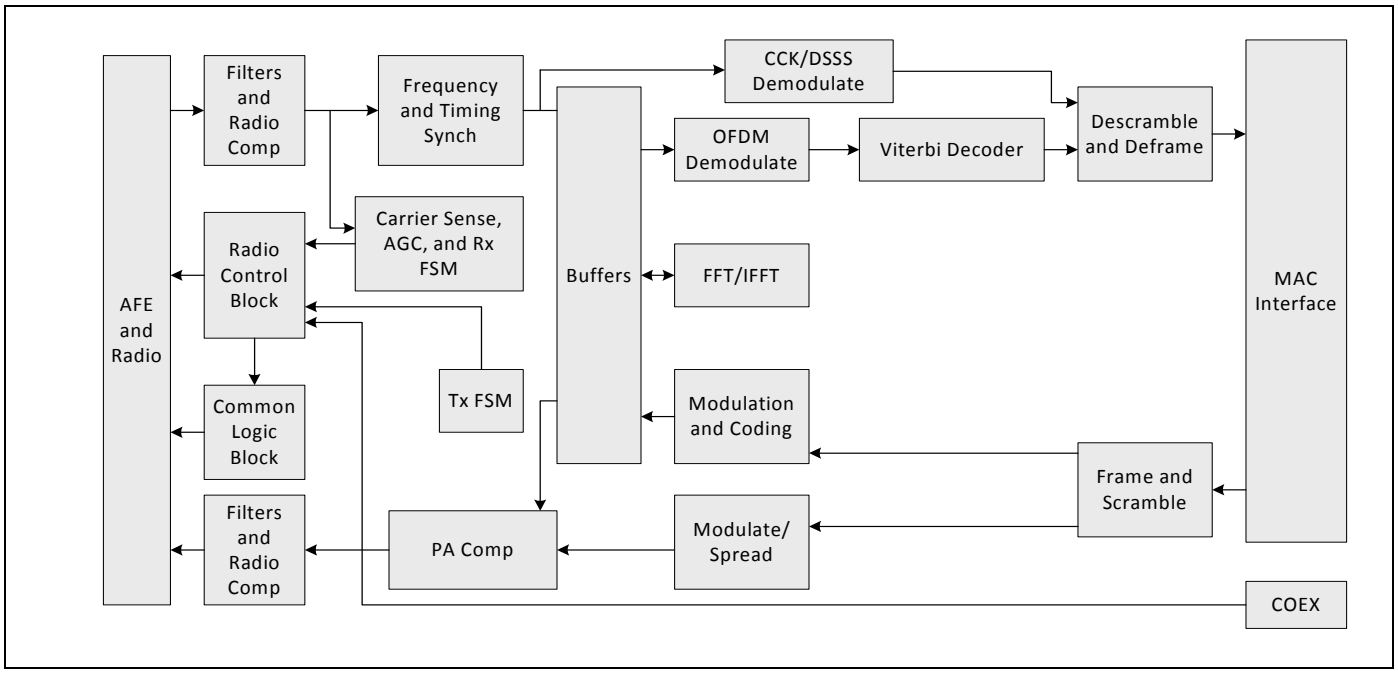
The CYW43903 WLAN digital PHY complies with IEEE 802.11a/b/g/n single-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 433.3 Mbps for low-power, high-performance, handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of filters, FFTs, and Viterbi-decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sensing and rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier-sensing algorithm provides high throughput for IEEE 802.11b/g hybrid networks with Bluetooth coexistence.

The key PHY features include:

- Programmable data rates from MCS0–7 in 20 MHz and 40 MHz channels.
- Support for Optional Short GI and Green Field modes in TX and RX.
- TX and RX LDPC for improved range and power efficiency.
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Support for IEEE 802.11h/k for worldwide operation.
- Advanced algorithms for low power consumption and enhanced sensitivity, range, and reliability.
- Algorithms to improve performance in the presence of externally received Bluetooth signals.
- An automatic gain control scheme for blocking and nonblocking cellular applications.
- Closed loop transmit power control.
- Digital RF chip calibration algorithms to handle CMOS RF chip process, voltage, and temperature (PVT) variations.
- On-the-fly channel frequency and transmit power selection.
- Per-packet RX antenna diversity.
- Available per-packet channel quality and signal-strength measurements.
- Compliance with FCC and other worldwide regulatory requirements.

Figure 13. WLAN PHY Block Diagram



8. WLAN Radio Subsystem

The CYW43903 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Ten RF control signals are available to drive external RF switches. In addition, these control signals can be used to support optional external 5 GHz band power and low-noise amplifiers. See the reference board schematics for more information.

A block diagram of the radio subsystem is shown in Figure 14. Note that integrated on-chip baluns (not shown) convert the fully differential transmit and receive paths to single-ended signal pins.

8.1 Receiver Path

The CYW43903 has a wide dynamic range, direct conversion receiver that employs high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. The 2.4 GHz and 5 GHz paths each have a dedicated on-chip low-noise amplifier (LNA).

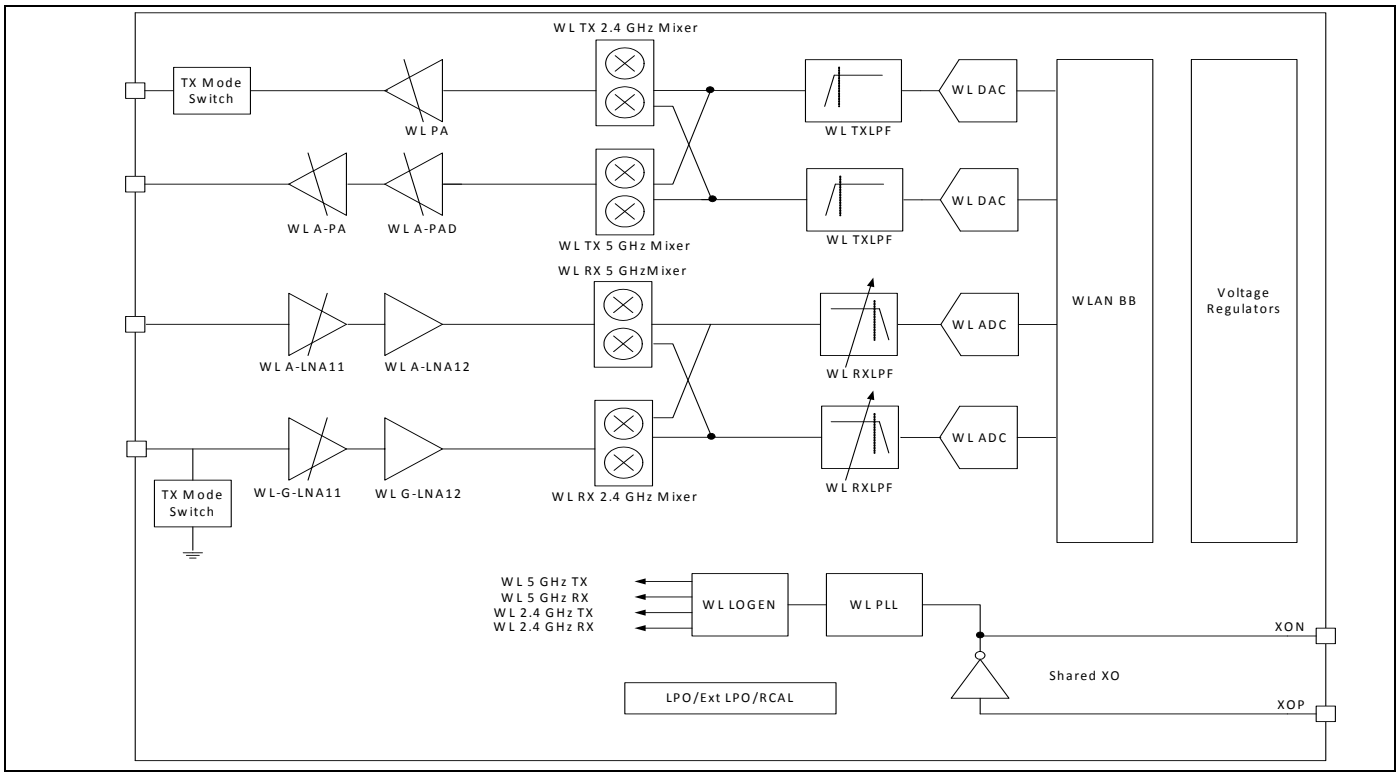
8.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively. Linear on-chip power amplifiers deliver high output powers while meeting IEEE 802.11a/b/g/n specifications without the need for external PAs. When using the internal PA, which is required in the 2.4 GHz band and optional in the 5 GHz band, closed-loop output power control is completely integrated.

8.3 Calibration

The CYW43903 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically during the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for carrier leakage reduction. In addition, I/Q calibration and VCO calibration are performed on-chip. No per-board calibration is required during manufacturing testing. This helps to minimize the test time and cost in large-volume production environments.

Figure 14. Radio Functional Block Diagram

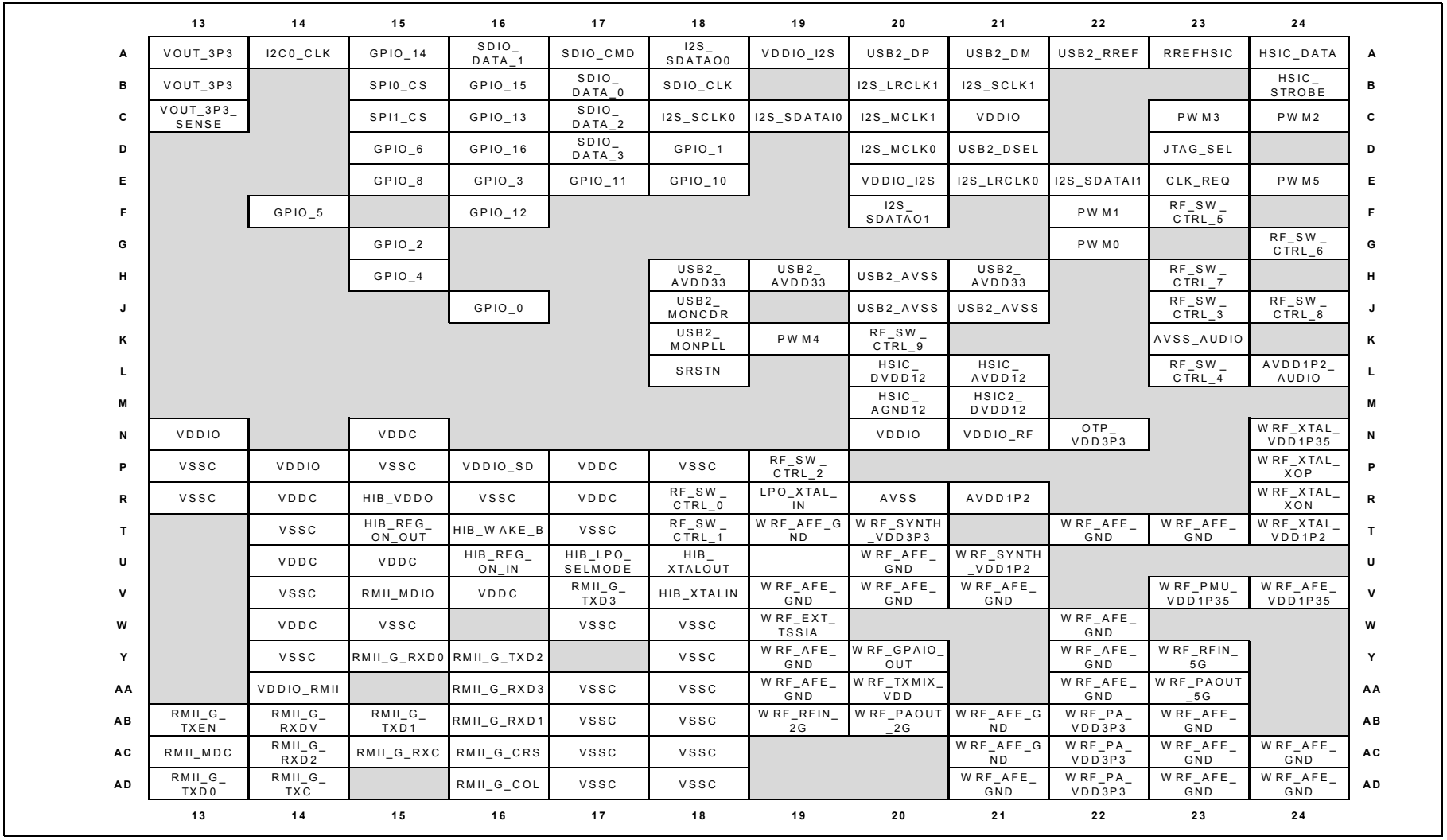


9. Pinout and Signal Descriptions

Figure 15. 338-Ball FCFBGA Map—Top View with Balls Facing Down (Page 1 of 2)

	1	2	3	4	5	6	7	8	9	10	11	12	
A	LDO_VDD1P5	LDO_VDD1P5	LDO_VDD1P5	VOUT_CLDO_SENSE	VOUT_CLDO	VOUT_CLDO		VOUT_HSICLDO	VOUT_LNLDO			LDO_VDDBAT5V	A
B	LDO_VDD1P5	LDO_VDD1P5	LDO_VDD1P5		VOUT_CLDO	VOUT_CLDO		VOUT_HSICLDO	VOUT_LNLDO			LDO_VDDBAT5V	B
C	NC	NC	NC		VOUT_CLDO	VOUT_CLDO		VOUT_HSICLDO				LDO_VDDBAT5V	C
D	NC	NC	NC							VOUT_LNLDO		LDO_VDDBAT5V	D
E							VOUT_CLDO		VOUT_HSICLDO		VOUT_LNLDO		E
F	SR_VDDBAT5V	SR_VDDBAT5V	SR_VDDBAT5V					VOUT_CLDO					F
G	SR_VLX	SR_VLX	SR_VLX						VOUT_CLDO				G
H	I2C0_SDATA			SR_VLX	SR_VLX						VOUT_HSICLDO		H
J	I2C1_CLK	GPIO_9	GPIO_7	REG_ON	UART0_TXD					VOUT_CLDO			J
K	UART0_CTS				SPI1_MISO	SR_PVSS	SR_PVSS	SR_PVSS					K
L	SFL_CS	SPI1_SISO	I2C1_SDATA	UART0_RXD		UART0_RTS		SR_PVSS					L
M			SPI0_CLK	SPI1_CLK	SFL_CLK		SPI0_SISO				PMU_AVSS	VDDIO	M
N	SFL_IO0	SFL_IO1	SFL_IO3	SFL_IO2		VSSC		SPI0_MISO					N
P	DDR_DDRV	DDR_WE_N	DDR_BANK_2		DDR_BANK_1		VDDIO_DDR		VDDIO_DDR				P
R	DDR_RESET_N	VSSC	VSSC	DDR_A_3		VSSC		VSSC					R
T	DDR_ODT	DDR_CS_N	DDR_CAS_N		DDR_A_1		DDR_A_2		VDDIO_DDR				T
U	DDR_CKE	VSSC	VSSC	DDR_A_9		DDR_A_8		VSSC					U
V	DDR_BANK_0	DDR_A_0	DDR_A_7		VSSC				VDDIO_DDR				V
W	DDR_RAS_N	VSSC	VSSC	DDR_COMP		DDR_A_10		VSSC					W
Y	DDR_A_5	DDR_A_4	DDR_A_6	VSSC	DDR_D_8		VDDIO_DDR						Y
AA	DDR_A_11	VSSC	VSSC	DDR_D_9		DDR_D_2		VDDIO_DDR		DDR_D_1		VDDIO_DDR	AA
AB	DDR_A_14	VSSC	DDR_A_13	VSSC	DDR_D_11	VSSC	DDR_D_13	VSSC	DDR_D_4	VSSC	DDR_D_3	VSSC	AB
AC	DDR_A_12	VSSC	DDR_D_10	VSSC	DDR_D_12	VSSC	DDR_DM_1	VSSC	DDR_D_14	VSSC	DDR_D_7	VSSC	AC
AD	DDR_A_15	DDR_CLK	DDR_CLK_N	DDR_DQSP_1	DDR_DQSM_1	DDR_D_15	DDR_D_6	DDR_D_0	DDR_DQSP_0	DDR_DQSM_0	DDR_D_5	DDR_DM_0	AD
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 16. 338-Ball FCFBGA Map—Top View with Balls Facing Down (Page 2 of 2)



	13	14	15	16	17	18	19	20	21	22	23	24	
A	VOUT_3P3	I2C0_CLK	GPIO_14	SDIO_DATA_1	SDIO_CMD	I2S_SDATAO0	VDDIO_I2S	USB2_DP	USB2_DM	USB2_RREF	RREFHSIC	HSIC_DATA	A
B	VOUT_3P3		SPI0_CS	GPIO_15	SDIO_DATA_0	SDIO_CLK		I2S_LRCLK1	I2S_SCLK1			HSIC_STROBE	B
C	VOUT_3P3_SENSE		SPI1_CS	GPIO_13	SDIO_DATA_2	I2S_SCLK0	I2S_SDATAI0	I2S_MCLK1	VDDIO		PWM3	PWM2	C
D			GPIO_6	GPIO_16	SDIO_DATA_3	GPIO_1		I2S_MCLK0	USB2_DSEL		JTAG_SEL		D
E			GPIO_8	GPIO_3	GPIO_11	GPIO_10		VDDIO_I2S	I2S_LRCLK0	I2S_SDATAI1	CLK_REQ	PWM5	E
F		GPIO_5		GPIO_12				I2S_SDATAO1		PWM1	RF_SW_CTRL_5		F
G			GPIO_2							PWM0		RF_SW_CTRL_6	G
H			GPIO_4			USB2_AVDD33	USB2_AVDD33	USB2_AVSS	USB2_AVDD33		RF_SW_CTRL_7		H
J				GPIO_0		USB2_MONCDR		USB2_AVSS	USB2_AVSS		RF_SW_CTRL_3	RF_SW_CTRL_8	J
K						USB2_MONPLL	PWM4	RF_SW_CTRL_9			AVSS_AUDIO		K
L						SRSTN		HSIC_DVDD12	HSIC_AVDD12		RF_SW_CTRL_4	AVDD1P2_AUDIO	L
M								HSIC_AGND12	HSIC2_DVDD12				M
N	VDDIO		VDDC					VDDIO	VDDIO_RF	OTP_VDD3P3		WRF_XTAL_VDD1P35	N
P	VSSC	VDDIO	VSSC	VDDIO_SD	VDDC	VSSC	RF_SW_CTRL_2					WRF_XTAL_XOP	P
R	VSSC	VDDC	HIB_VDDO	VSSC	VDDC	RF_SW_CTRL_0	LPO_XTAL_IN	AVSS	AVDD1P2			WRF_XTAL_XON	R
T		VSSC	HIB_REG_ON_OUT	HIB_WAKE_B	VSSC	RF_SW_CTRL_1	WRF_AFE_GND	WRF_SYNTH_VDD3P3		WRF_AFE_GND	WRF_AFE_GND	WRF_XTAL_VDD1P2	T
U		VDDC	VDDC	HIB_REG_ON_IN	HIB_LPO_SELMODE	HIB_XTALOUT		WRF_AFE_GND	WRF_SYNTH_VDD1P2				U
V		VSSC	RMII_MDIO	VDDC	RMII_G_TXD3	HIB_XTALIN	WRF_AFE_GND	WRF_AFE_GND	WRF_AFE_GND		WRF_PMU_VDD1P35	WRF_AFE_VDD1P35	V
W		VDDC	VSSC		VSSC	VSSC	WRF_EXT_TSSIA			WRF_AFE_GND			W
Y		VSSC	RMII_G_RXD0	RMII_G_TXD2		VSSC	WRF_AFE_GND	WRF_GPAIO_OUT		WRF_AFE_GND	WRF_RFIN_5G		Y
AA		VDDIO_RMII		RMII_G_RXD3	VSSC	VSSC	WRF_AFE_GND	WRF_TXMIX_VDD		WRF_AFE_GND	WRF_PAOUT_5G		AA
AB	RMII_G_TXEN	RMII_G_RXDV	RMII_G_TXD1	RMII_G_RXD1	VSSC	VSSC	WRF_RFIN_2G	WRF_PAOUT_2G	WRF_AFE_GND	WRF_PA_VDD3P3	WRF_AFE_GND		AB
AC	RMII_MDC	RMII_G_RXD2	RMII_G_RXC	RMII_G_CRS	VSSC	VSSC			WRF_AFE_GND	WRF_PA_VDD3P3	WRF_AFE_GND	WRF_AFE_GND	AC
AD	RMII_G_TXD0	RMII_G_TXC		RMII_G_COL	VSSC	VSSC			WRF_AFE_GND	WRF_PA_VDD3P3	WRF_AFE_GND	WRF_AFE_GND	AD
	13	14	15	16	17	18	19	20	21	22	23	24	

9.1 Ball List

Table 11 contains the 338-ball FCFBGA net names.

Table 11. FCFBGA Net Names

Ball	Net Name
A1	LDO_VDD1P5
A2	LDO_VDD1P5
A3	LDO_VDD1P5
A4	VOUT_CLDO_SENSE
A5	VOUT_CLDO
A6	VOUT_CLDO
A8	VOUT_HSICLDO
A9	VOUT_LNLDO
A12	LDO_VDDBAT5V
A13	VOUT_3P3
A14	I2C0_CLK
A15	GPIO_14
A16	SDIO_DATA_1
A17	SDIO_CMD
A18	I2S_SDATAO0
A19	VDDIO_I2S
A20	USB2_DP
A21	USB2_DM
A22	USB2_RREF
A23	RREFHSIC
A24	HSIC_DATA
B1	LDO_VDD1P5
B2	LDO_VDD1P5
B3	LDO_VDD1P5
B5	VOUT_CLDO
B6	VOUT_CLDO
B8	VOUT_HSICLDO
B9	VOUT_LNLDO
B12	LDO_VDDBAT5V
B13	VOUT_3P3
B15	SPI0_CS
B16	GPIO_15
B17	SDIO_DATA_0
B18	SDIO_CLK
B20	I2S_LRCLK1
B21	I2S_SCLK1
B24	HSIC_STROBE
C1	NC
C2	NC
C3	NC
C5	VOUT_CLDO
C6	VOUT_CLDO
C8	VOUT_HSICLDO
C12	LDO_VDDBAT5V
C13	VOUT_3P3_SENSE
C15	SPI1_CS
C16	GPIO_13
C17	SDIO_DATA_2
C18	I2S_SCLK0
C19	I2S_SDATAI0
C20	I2S_MCLK1
C21	VDDIO
C23	PWM3
C24	PWM2
D1	NC
D2	NC
D3	NC
D10	VOUT_LNLDO
D12	LDO_VDDBAT5V
D15	GPIO_6
D16	GPIO_16
D17	SDIO_DATA_3
D18	GPIO_1
D20	I2S_MCLK0
D21	USB2_DSEL
D23	JTAG_SEL
E7	VOUT_CLDO
E9	VOUT_HSICLDO
E11	VOUT_LNLDO
E15	GPIO_8
E16	GPIO_3
E17	GPIO_11
E18	GPIO_10
E20	VDDIO_I2S
E21	I2S_LRCLK0
E22	I2S_SDATAI1
E23	CLK_REQ
E24	PWM5
F1	SR_VDDBAT5V
F2	SR_VDDBAT5V
F3	SR_VDDBAT5V
F8	VOUT_CLDO
F14	GPIO_5
F16	GPIO_12
F20	I2S_SDATAO1
F22	PWM1

Ball	Net Name
F23	RF_SW_CTRL_5
G1	SR_VLX
G2	SR_VLX
G3	SR_VLX
G9	VOUT_CLDO
G15	GPIO_2
G22	PWM0
G24	RF_SW_CTRL_6
H1	I2C0_SDATA
H4	SR_VLX
H5	SR_VLX
H11	VOUT_HSICLDO
H15	GPIO_4
H18	USB2_AVDD33
H19	USB2_AVDD33
H20	USB2_AVSS
H21	USB2_AVDD33
H23	RF_SW_CTRL_7
J1	I2C1_CLK
J2	GPIO_9
J3	GPIO_7
J4	REG_ON
J5	UART0_TXD
J10	VOUT_CLDO
J16	GPIO_0
J18	USB2_MONCDR
J20	USB2_AVSS
J21	USB2_AVSS
J23	RF_SW_CTRL_3
J24	RF_SW_CTRL_8
K1	UART0_CTS
K5	SPI1_MISO
K6	SR_PVSS
K7	SR_PVSS
K8	SR_PVSS
K18	USB2_MONPLL
K19	PWM4
K20	RF_SW_CTRL_9
K23	AVSS_AUDIO
L1	SFL_CS
L2	SPI1_SISO
L3	I2C1_SDATA
L4	UART0_RXD
L6	UART0_RTS
L8	SR_PVSS
L18	SRSTN
L20	HSIC_DVDD12

Ball	Net Name
L21	HSIC_AVDD12
L23	RF_SW_CTRL_4
L24	AVDD1P2_AUDIO
M3	SPI0_CLK
M4	SPI1_CLK
M5	SFL_CLK
M7	SPI0_SISO
M11	PMU_AVSS
M12	VDDIO
M20	HSIC_AGND12
M21	HSIC2_DVDD12
N1	SFL_IO0
N2	SFL_IO1
N3	SFL_IO3
N4	SFL_IO2
N6	VSSC
N8	SPI0_MISO
N13	VDDIO
N15	VDDC
N20	VDDIO
N21	VDDIO_RF
N22	OTP_VDD3P3
N24	WRF_XTAL_VDD1P35
P1	DDR_DDRV
P2	DDR_WE_N
P3	DDR_BANK_2
P5	DDR_BANK_1
P7	VDDIO_DDR
P9	VDDIO_DDR
P13	VSSC
P14	VDDIO
P15	VSSC
P16	VDDIO_SD
P17	VDDC
P18	VSSC
P19	RF_SW_CTRL_2
P24	WRF_XTAL_XOP
R1	DDR_RESET_N
R2	VSSC
R3	VSSC
R4	DDR_A_3
R6	VSSC
R8	VSSC
R13	VSSC
R14	VDDC
R15	HIB_VDDO
R16	VSSC

Ball	Net Name
R17	VDDC
R18	RF_SW_CTRL_0
R19	LPO_XTAL_IN
R20	AVSS
R21	AVDD1P2
R24	WRF_XTAL_XON
T1	DDR_ODT
T2	DDR_CS_N
T3	DDR_CAS_N
T5	DDR_A_1
T7	DDR_A_2
T9	VDDIO_DDR
T14	VSSC
T15	HIB_REG_ON_OUT
T16	HIB_WAKE_B
T17	VSSC
T18	RF_SW_CTRL_1
T19	WRF_AFE_GND
T20	WRF_SYNTH_VDD3P3
T22	WRF_AFE_GND
T23	WRF_AFE_GND
T24	WRF_XTAL_VDD1P2
U1	DDR_CKE
U2	VSSC
U3	VSSC
U4	DDR_A_9
U6	DDR_A_8
U8	VSSC
U14	VDDC
U15	VDDC
U16	HIB_REG_ON_IN
U17	HIB_LPO_SELMODE
U18	HIB_XTALOUT
U20	WRF_AFE_GND
U21	WRF_SYNTH_VDD1P2
V1	DDR_BANK_0
V2	DDR_A_0
V3	DDR_A_7
V5	VSSC
V9	VDDIO_DDR
V14	VSSC
V15	RMII_MDIO
V16	VDDC
V17	RMII_G_TXD3
V18	HIB_XTALIN
V19	WRF_AFE_GND
V20	WRF_AFE_GND

Ball	Net Name
V21	WRF_AFE_GND
V23	WRF_PMU_VDD1P35
V24	WRF_AFE_VDD1P35
W1	DDR_RAS_N
W2	VSSC
W3	VSSC
W4	DDR_COMP
W6	DDR_A_10
W8	VSSC
W14	VDDC
W15	VSSC
W17	VSSC
W18	VSSC
W19	WRF_EXT_TSSIA
W22	WRF_AFE_GND
Y1	DDR_A_5
Y2	DDR_A_4
Y3	DDR_A_6
Y4	VSSC
Y5	DDR_D_8
Y7	VDDIO_DDR
Y14	VSSC
Y15	RMII_G_RXD0
Y16	RMII_G_TXD2
Y18	VSSC
Y19	WRF_AFE_GND
Y20	WRF_GPAIO_OUT
Y22	WRF_AFE_GND
Y23	WRF_RFIN_5G
AA1	DDR_A_11
AA2	VSSC
AA3	VSSC
AA4	DDR_D_9
AA6	DDR_D_2
AA8	VDDIO_DDR
AA10	DDR_D_1
AA12	VDDIO_DDR
AA14	VDDIO_RMII
AA16	RMII_G_RXD3
AA17	VSSC
AA18	VSSC
AA19	WRF_AFE_GND
AA20	WRF_TXMIX_VDD
AA22	WRF_AFE_GND
AA23	WRF_PAOUT_5G
AB1	DDR_A_14
AB2	VSSC

Ball	Net Name
AB3	DDR_A_13
AB4	VSSC
AB5	DDR_D_11
AB6	VSSC
AB7	DDR_D_13
AB8	VSSC
AB9	DDR_D_4
AB10	VSSC
AB11	DDR_D_3
AB12	VSSC
AB13	RMII_G_TXEN
AB14	RMII_G_RXDV
AB15	RMII_G_TXD1
AB16	RMII_G_RXD1
AB17	VSSC
AB18	VSSC
AB19	WRF_RFIN_2G
AB20	WRF_PAOUT_2G
AB21	WRF_AFE_GND
AB22	WRF_PA_VDD3P3
AB23	WRF_AFE_GND
AC1	DDR_A_12
AC2	VSSC
AC3	DDR_D_10
AC4	VSSC
AC5	DDR_D_12
AC6	VSSC
AC7	DDR_DM_1
AC8	VSSC
AC9	DDR_D_14
AC10	VSSC
AC11	DDR_D_7
AC12	VSSC
AC13	RMII_MDC
AC14	RMII_G_RXD2
AC15	RMII_G_RXC
AC16	RMII_G_CRS
AC17	VSSC
AC18	VSSC
AC21	WRF_AFE_GND
AC22	WRF_PA_VDD3P3
AC23	WRF_AFE_GND
AC24	WRF_AFE_GND
AD1	DDR_A_15
AD2	DDR_CLK
AD3	DDR_CLK_N
AD4	DDR_DQSP_1

Ball	Net Name
AD5	DDR_DQSM_1
AD6	DDR_D_15
AD7	DDR_D_6
AD8	DDR_D_0
AD9	DDR_DQSP_0
AD10	DDR_DQSM_0
AD11	DDR_D_5
AD12	DDR_DM_0
AD13	RMII_G_TXD0
AD14	RMII_G_TXC
AD16	RMII_G_COL
AD17	VSSC
AD18	VSSC
AD21	WRF_AFE_GND
AD22	WRF_PA_VDD3P3
AD23	WRF_AFE_GND
AD24	WRF_AFE_GND

9.2 Signal Descriptions

Table 12 provides the signal name, type, and description for each CYW43903 ball. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, and O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 12. Signal Descriptions

Ball Number	Signal Name	Type	Description
Broadcom Serial Control (BSC) Interfaces			
A14	I2C0_CLK	O	BSC master clock.
H1	I2C0_SDATA	I/O	BSC serial data
J1	I2C1_CLK	O	BSC master clock
L3	I2C1_SDATA	I/O	BSC serial data
Clocks			
P24	WRF_XTAL_XOP	I	XTAL oscillator input.
R24	WRF_XTAL_XON	O	XTAL oscillator output.
R19	LPO_XTAL_IN	I	External sleep clock input (32.768 kHz).
V18	HIB_XTALIN	I	3.3V 32 kHz crystal input
U18	HIB_XTALOUT	O	3.3V 32 kHz crystal output
E23	CLK_REQ	O	Reference clock request
DDR Interface			
AD12	DDR_DM_0	O	DDR data slice mask 0
AC7	DDR_DM_1	O	DDR data slice mask 1
AD4	DDR_DQSP_1	I/O	DDR data strobe for slice 1, plus polarity
AD5	DDR_DQSM_1	I/O	DDR data strobe for slice 1, minus polarity
AD9	DDR_DQSP_0	I/O	DDR data strobe for slice 0, plus polarity
AD10	DDR_DQSM_0	I/O	DDR data strobe for slice 0, minus polarity
AD8	DDR_D_0	I/O	DDR data signal
AA10	DDR_D_1	I/O	DDR data signal
AA6	DDR_D_2	I/O	DDR data signal
AB11	DDR_D_3	I/O	DDR data signal
AB9	DDR_D_4	I/O	DDR data signal
AD11	DDR_D_5	I/O	DDR data signal
AD7	DDR_D_6	I/O	DDR data signal
AC11	DDR_D_7	I/O	DDR data signal
Y5	DDR_D_8	I/O	DDR data signal
AA4	DDR_D_9	I/O	DDR data signal
AC3	DDR_D_10	I/O	DDR data signal
AB5	DDR_D_11	I/O	DDR data signal
AC5	DDR_D_12	I/O	DDR data signal
AB7	DDR_D_13	I/O	DDR data signal
AC9	DDR_D_14	I/O	DDR data signal
AD6	DDR_D_15	I/O	DDR data signal
V2	DDR_A_0	O	DDR address signal
T5	DDR_A_1	O	DDR address signal
T7	DDR_A_2	O	DDR address signal
R4	DDR_A_3	O	DDR address signal
Y2	DDR_A_4	O	DDR address signal

Table 12. Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Y1	DDR_A_5	O	DDR address signal
Y3	DDR_A_6	O	DDR address signal
V3	DDR_A_7	O	DDR address signal
U6	DDR_A_8	O	DDR address signal
U4	DDR_A_9	O	DDR address signal
W6	DDR_A_10	O	DDR address signal
AA1	DDR_A_11	O	DDR address signal
AC1	DDR_A_12	O	DDR address signal
AB3	DDR_A_13	O	DDR address signal
AB1	DDR_A_14	O	DDR address signal
AD1	DDR_A_15	O	DDR address signal
AD2	DDR_CLK	O	DDR clock, plus polarity
AD3	DDR_CLK_N	O	DDR clock, minus polarity
W4	DDR_COMP	I	DDR compensation pad
W1	DDR_RAS_N	O	DDR row address strobe, active low
T3	DDR_CAS_N	O	DDR column address strobe, active low
V1	DDR_BANK_0	O	DRAM memory bank selection
P5	DDR_BANK_1	O	DRAM memory bank selection
P3	DDR_BANK_2	O	DRAM memory bank selection
U1	DDR_CKE	O	DDR clock enable
T2	DDR_CS_N	O	DDR chip selection, active low
T1	DDR_ODT	O	DDR on die termination
R1	DDR_RESET_N	O	DRAM reset, active low signal
P2	DDR_WE_N	O	DDR write enable, active low
P1	DDR_DDRV	I	DDR input reference voltage

Table 12. Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Ethernet MAC Interface (MII/RMII)			
AC15	RMII_G_RXC	I	MII receive clock
AD16	RMII_G_COL	I	MII collision detection
AC16	RMII_G_CRS	I	MII carrier sense
AD14	RMII_G_TXC	I	MII/RMII transmit clock
AD13	RMII_G_TXD0	O	MII/RMII transmit signal
AB15	RMII_G_TXD1	O	MII/RMII transmit signal
Y16	RMII_G_TXD2	O	MII transmit signal
V17	RMII_G_TXD3	O	MII transmit signal
Y15	RMII_G_RXD0	I	MII/RMII receive signal
AB16	RMII_G_RXD1	I	MII/RMII receive signal
AC14	RMII_G_RXD2	I	MII receive signal
AA16	RMII_G_RXD3	I	MII receive signal
V15	RMII_MDIO	I/O	MII/RMII management data
AC13	RMII_MDC	O	MII/RMII management clock
AB13	RMII_G_TXEN	O	MII/RMII transmit enable
AB14	RMII_G_RXDV	I	MII/RMII receive data valid
GPIO Interface (WLAN)			
J16	GPIO_0	I/O	Programmable GPIO pins.
D18	GPIO_1	I/O	
G15	GPIO_2	I/O	
E16	GPIO_3	I/O	
H15	GPIO_4	I/O	
F14	GPIO_5	I/O	
D15	GPIO_6	I/O	
J3	GPIO_7	I/O	
E15	GPIO_8	I/O	
J2	GPIO_9	I/O	
E18	GPIO_10	I/O	
E17	GPIO_11	I/O	
F16	GPIO_12	I/O	
C16	GPIO_13	I/O	
A15	GPIO_14	I/O	
B16	GPIO_15	I/O	
D16	GPIO_16	I/O	

Table 12. Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Ground			
V19, v20, V21, W22, Y19, Y22, AA19. AA22, AB21, AB23, T19, T22, T23, U20, AC21, AC23, AC24, AD21, AD23, AD24	WRF_AFE_GND	GND	AFE ground
W2, W3, W8, W15, W17, W18, Y4, Y14, Y18, AA2, AA3,. N6, P13, P15, AA17, AA18, AB2, AB4, AB6, AB8, AB10, P18, R2, R3, R6, R8, R13, R16, AB12, AB17, AB18, AC2, AC4, AC6, AC8, AC10, AC12, AC17, AC18, T14, T17, U2, U3, U8, V5, V14, AD17, AD18	VSSC	GND	Core ground for WLAN and APP sections
K6, K7, K8, L8	SR_PVSS	GND	Power ground
M11	PMU_AVSS	GND	Quiet ground
R20	AVSS	GND	Baseband PLL ground
K23	AVSS_AUDIO	GND	AUDIO PLL ground
J20, J21, H20	USB2_AVSS	GND	USB 2.0 analog ground
M20	HSIC_AGND12	GND	HSIC analog ground
Hibernation Block, Power-Down/Power-Up, and Reset			
J4	REG_ON	I	Used by PMU to power up or power down the internal CYW43903 regulators used by the WLAN and APP sections. Also, when deasserted, this pin holds the WLAN and APP sections in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
U16	HIB_REG_ON_IN	I	Used by the hibernation block to power up or power down the internal CYW43903 regulators. For applications that use the hibernation block, HIB_REG_ON_OUT must connect to REG_ON. Also, when deasserted, this pin holds the WLAN and APP sections in reset.
T15	HIB_REG_ON_OUT	O	REG_ON output signal generated by the hibernation block.
T16	HIB_WAKE_B	I	Wake up chip from hibernation mode.
U17	HIB_LPO_SELMODE	I	Select precise or coarse 32 kHz clock.
L18	SRSTN	I	System reset. This active-low signal resets the backplanes.
I^2S Interface			
D20	I2S_MCLK0	I/O	M clock
C18	I2S_SCLK0	I/O	S clock
E21	I2S_LRCLK0	I/O	LR clock
C19	I2S_SDATAI0	I	I^2S data input
A18	I2S_SDATAO0	O	I^2S data output
C20	I2S_MCLK1	I/O	M clock
B21	I2S_SCLK1	I/O	S clock
B20	I2S_LRCLK1	I/O	LR clock
E22	I2S_SDATAI1	I	I^2S data input
F20	I2S_SDATAO1	O	I^2S data output
JTAG Interface			
D23	JTAG_SEL	I	JTAG select. This pin must be connected to ground if the JTAG interface is not used.
No Connects			
C1, C2, C3, D1, D2, D3	NC	–	No connect

Table 12. Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Power Supplies (Miscellaneous)			
N22	OTP_VDD3P3	PWR	OTP 3.3V supply
W14, N15, P17, R14, R17, U14, U15, V16	VDDC	PWR	1.2V core supply for WLAN
C21, M12, N13, N20, P14	VDDIO	PWR	I/O supply
N21	VDDIO_RF	PWR	I/O supply for RF switch control pads (3.3V).
A19, E20	VDDIO_I2S	PWR	I/O supply for I^2S
AA14	VDDIO_RMII	PWR	I/O supply for RMII
Y7, P7, P9, T9, V9, AA8, AA12	VDDIO_DDR	PWR	I/O supply for DDR
P16	VDDIO_SD	PWR	I/O supply for SDIO
R15	HIB_VDDO	PWR	I/O supply for hibernation block
R21	AVDD1P2	PWR	1.2V supply for baseband PLL
L24	AVDD1P2_AUDIO	PWR	1.2V supply for audio PLL
L20	HSIC_DVDD12	PWR	1.2V supply for HSIC digital circuit
L21	HSIC_AVDD12	PWR	1.2V supply for HSIC analog circuit
M21	HSIC2_DVDD12	PWR	1.2V supply for HSIC digital circuit
H18, H19, H21	USB2_AVDD33	PWR	3.3V supply for USB 2.0
Power Supplies (WLAN)			
T20	WRF_SYNTH_VDD3P3	PWR	Synthesizer VDD 3.3V supply
AB22, AC22, AD22	WRF_PA_VDD3P3	PWR	2.4 GHz and 5 GHz PA 3.3V VBAT supply
V23	WRF_PMU_VDD1P35	PWR	PMU 1.35V supply
AA20	WRF_TXMIX_VDD	PWR	3.3V supply for TX mixer
U21	WRF_SYNTH_VDD1P2	PWR	1.2V supply for synthesizer
V24	WRF_AFE_VDD1P35	PWR	1.35V supply for the analog front end (AFE)
PWM Interface			
G22	PWM0	O	Pulse width modulation bit 0.
F22	PWM1	O	Pulse width modulation bit 1
C24	PWM2	O	Pulse width modulation bit 2
C23	PWM3	O	Pulse width modulation bit 3
K19	PWM4	O	Pulse width modulation bit 4
E24	PWM5	O	Pulse width modulation bit 5

Table 12. Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
RF Signal Interface (WLAN)			
AB19	WRF_RFIN_2G	I	2.4 GHz WLAN receiver input
Y23	WRF_RFIN_5G	I	5 GHz WLAN receiver input
AB20	WRF_PAOUT_2G	O	2.4 GHz WLAN PA output
AA23	WRF_PAOUT_5G	O	5 GHz WLAN PA output
W19	WRF_EXT_TSSIA	I	5 GHz TSSI input from an optional external power amplifier/power detector
Y20	WRF_GPAIO_OUT	I/O	Analog GPIO
RF Switch Control Lines			
R18	RF_SW_CTRL_0	O	Programmable RF switch control lines. The control lines are programmable via the driver and nvram.txt file.
T18	RF_SW_CTRL_1	O	
P19	RF_SW_CTRL_2	O	
J23	RF_SW_CTRL_3	O	
L23	RF_SW_CTRL_4	O	
F23	RF_SW_CTRL_5	I/O	
G24	RF_SW_CTRL_6	I/O	
H23	RF_SW_CTRL_7	I/O	
J24	RF_SW_CTRL_8	I/O	
K20	RF_SW_CTRL_9	I/O	
SDIO Interface			
B18	SDIO_CLK	I/O	SDIO cock
A17	SDIO_CMD	I/O	SDIO command line
B17	SDIO_DATA_0	I/O	SDIO data line 0
A16	SDIO_DATA_1	I/O	SDIO data line 1
C17	SDIO_DATA_2	I/O	SDIO data line 2
D17	SDIO_DATA_3	I/O	SDIO data line 3
S/PDIF Interface			
Note: Supported via the A18 (I2S_SDATAO0) and F20 (I2S_SDATAO1) pins.			
SPI Flash Interface			
M5	SFL_CLK	O	Flash clock
N1	SFL_IO0	I/O	Flash data
N2	SFL_IO1	I/O	Flash data
N4	SFL_IO2	I/O	Flash data
N3	SFL_IO3	I/O	Flash data
L1	SFL_CS	O	Flash slave select

Table 12. Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
SPI Interfaces			
Note: Each SPI interface can alternatively be configured and used as a BSC interface.			
M3	SPI0_CLK	O	SPI clock
N8	SPI0_MISO	I	SPI data master in
M7	SPI0_SISO	O	SPI data master out
B15	SPI0_CS	O	SPI slave select
M4	SPI1_CLK	O	SPI clock
K5	SPI1_MISO	I	SPI data master in
L2	SPI1_SISO	O	SPI data master out
C15	SPI1_CS	O	SPI slave select
UART Interface			
K1	UART0_CTS	I	UART clear-to-send
L6	UART0_RTS	O	UART request-to-send
L4	UART0_RXD	I	UART serial input
J5	UART0_TXD	O	UART serial output
USB 2.0 and HSIC			
A21	USB2_DM	I/O	USB 2.0 data
A20	USB2_DP	I/O	USB 2.0 data
A22	USB2_RREF	I	USB 2.0 reference resistor connection
J18	USB2_MONCDR	O	USB 2.0 CDR monitor
K18	USB2_MONPLL	O	USB 2.0 PLL monitor
B24	HSIC_STROBE	I/O	HSIC strobe
A24	HSIC_DATA	I/O	HSIC data
A23	RREFHSIC	I	HSIC reference resistor connection
D21	USB2_DSEL	I	USB 2.0 host and device mode selection
Voltage Regulators (Integrated)			
F1, F2, F3	SR_VDDBAT5V	I	VBAT.
G1, G2, G3, H4, H5	SR_VLX	O	CBUCK switching regulator output
A1, A2, A3, B1, B2, B3	LDO_VDD1P5	I	LNLDO input
A12, B12, C12, D12	LDO_VDDBAT5V	I	LDO VBAT
N24	WRF_XTAL_VDD1P35	I	XTAL LDO input (1.35V)
T24	WRF_XTAL_VDD1P2	O	XTAL LDO output (1.2V)
A9, B9, D10, E11	VOUT_LNLDO	O	Output of LNLDO
A5, A6, B5, B6, C5, C6, E7,F8, G9, J10	VOUT_CLDO	O	Output of core LDO
A13, B13	VOUT_3P3	O	LDO 3.3V output
C13	VOUT_3P3_SENSE	O	Voltage sense pin for LDO 3.3V output
A4	VOUT_CLDO_SENSE	O	Voltage sense pin for core LDO
A8, B8, C8, E9, H11	VOUT_HSICLDO	O	Output of HSIC LDO

10. GPIO Signals and Strapping Options

10.1 Overview

This section describes GPIO signals and strapping options. The pins are sampled at power-on reset (POR) to determine various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in Table 14. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to ground, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

10.2 Weak Pull-Down and Pull-Up Resistances

At VDDO = 3.3V ±10%, the minimum, typical, and maximum weak pull-down resistances (for a pin voltage of VDDO) are 37.99 kΩ, 44.57 kΩ, and 51.56 kΩ, respectively. At VDDO = 3.3V ±10%, the minimum, typical, and maximum weak pull-up resistances (for a pin voltage of 0V) are 34.73 kΩ, 39.58 kΩ, and 44.51 kΩ, respectively.

10.3 Strapping Options

Table 13 provides the strapping options.

Table 13. Strapping Options

Pin Name	Strap	Ball #	Default Internal Pull During Strap	Description
GPIO_1	GSPI_MODE	D18	PD	Enable gSPI interface
GPIO_7	WCPU_BOOT_MODE	J7	PD	Boot from SoC SROM or SoC SRAM
GPIO_9	USB_HSIC_PHY_SEL	J2	PD	Select either USB or HSIC PHY (see USB 2.0/HSIC on page 23)
GPIO_11	ACPU_BOOT_MODE	E17	PD	Boot from tightly coupled memory (TCM) ROM or TCM RAM
GPIO_13	SDIO_MODE	C16	PD	Select either SDIO host mode or SDIO device mode
GPIO_15	VTRIM_EN	B16	PD	Enable PMU voltage trimming
RF_SW_CTRL_5	DAP_CLK_SEL	F23	PD	Select XTAL clock or the test clock (tck) for the debug access port (DAP)
RF_SW_CTRL_7	RSRC_INIT_MODE	H23	PD	PMU resource initialization mode selection

10.4 Alternate GPIO Signal Functions

Table 14 provides the alternate signal functions of the GPIO signals.

Table 14. Alternate GPIO Signal Functions

GPIO	Default	JTAG_SEL	Default Pull	HOLD/PDLOW/ PDHIGH	Strap	Comments
GPIO_0	USB20H_CTL	–	No pull	HOLD	–	8 mA
GPIO_1	–	–	Down	HOLD	GSPI_MODE	8 mA
GPIO_2	GCI_GPIO(0)	JTAG_TCK	No pull	HOLD	–	8 mA
GPIO_3	GCI_GPIO(1)	JTAG_TMS	No pull	HOLD	–	8 mA
GPIO_4	GCI_GPIO(2)	JTAG_TDI	No pull	HOLD	–	8 mA
GPIO_5	GCI_GPIO(3)	JTAG_TDO	No pull	HOLD	–	8 mA
GPIO_6	GCI_GPIO(4)	JTAG_TRST	No pull	HOLD	–	8 mA
GPIO_7	–	–	Down	HOLD	WCPU_BOOT_MODE	8 mA
GPIO_8	GPIO_8	–	No pull	HOLD	–	8 mA
GPIO_9	–	–	Down	HOLD	USB_HSIC_PHY_SEL	8 mA
GPIO_10	GPIO_10	–	No pull	HOLD	–	8 mA
GPIO_11	–	–	Down	HOLD	ACPU_BOOT_MODE	8 mA
GPIO_12	GPIO_12	–	No pull	HOLD	–	8 mA
GPIO_13	–	–	Down	HOLD	SDIO_MODE	8 mA
GPIO_14	GPIO_14	–	No pull	HOLD	–	8 mA
GPIO_15	–	–	Down	HOLD	VTRIM_EN	8 mA
GPIO_16	–	–	No pull	HOLD	–	8 mA

11. Pin Multiplexing

Table 15 shows the pin multiplexing functions.

Table 15. Pin Multiplexing

Pin	Function										
	1	2	3	4	5	6	7	8	9	10	11
GPIO_0	GPIO_0	UART0_RXD	I2C1_SDATA	PWM0	SPI1_MISO	PWM2	GPIO_12	GPIO_8	–	PWM4	USB20H_CTL
GPIO_1	GPIO_1	UART0_TXD	I2C1_CLK	PWM1	SPI1_CLK	PWM3	GPIO_13	GPIO_9	–	PWM5	–
GPIO_2	GPIO_2	–	–	GCI_GPIO_0	–	–	–	–	TCK	–	–
GPIO_3	GPIO_3	–	–	GCI_GPIO_1	–	–	–	–	TMS	–	–
GPIO_4	GPIO_4	–	–	GCI_GPIO_2	–	–	–	–	TDI	–	–
GPIO_5	GPIO_5	–	–	GCI_GPIO_3	–	–	–	–	TDO	–	–
GPIO_6	GPIO_6	–	–	GCI_GPIO_4	–	–	–	–	TRST_L	–	–
GPIO_7	GPIO_7	UART0_ RTS_OUT	PWM1	PWM3	SPI1_CS	I2C1_CLK	GPIO_15	GPIO_11	PMU_TEST_ O	–	PWM5
GPIO_8	GPIO_8	SPI1_MISO	PWM2	PWM4	UART0_RXD	–	GPIO_16	GPIO_12	TAP_SEL_P	I2C1_SDATA	PWM0
GPIO_9	GPIO_9	SPI1_CLK	PWM3	PWM5	UART0_TXD	–	GPIO_0	GPIO_13	–	I2C1_CLK	PWM1
GPIO_10	GPIO_10	SPI1_MOSI	PWM4	I2C1_SDATA	UART0_ CTS_IN	PWM0	GPIO_1	GPIO_14	PWM2	SDIO_SEP_ INT	SDIO_SEP_ INT_0D
GPIO_11	GPIO_11	SPI1_CS	PWM5	I2C1_CLK	UART0_ RTS_OUT	PWM1	GPIO_7	GPIO_15	PWM3	–	–
GPIO_12	GPIO_12	I2C1_SDATA	UART0_RXD	SPI1_MISO	PWM2	PWM4	GPIO_8	GPIO_16	PWM0	SDIO_SEP_ INT_0D	SDIO_SEP_ INT
GPIO_13	GPIO_13	I2C1_CLK	UART0_TXD	SPI1_CLK	PWM3	PWM5	GPIO_9	GPIO_0	PWM1	–	–
GPIO_14	GPIO_14	PWM0	UART0_ CTS_IN	SPI1_MOSI	I2C1_SDATA	–	GPIO_10	–	PWM4	–	PWM2
GPIO_15	GPIO_15	PWM1	UART0_ RTS_OUT	SPI1_CS	I2C1_CLK	–	GPIO_11	GPIO_7	PWM5	–	PWM3
GPIO_16	GPIO_16	UART0_ CTS_IN	PWM0	PWM2	SPI1_MOSI	I2C1_SDATA	GPIO_14	GPIO_10	RF_ DISABLE_L	–	PWM4
SDIO_CLK	SDIO_CLK	–	–	–	–	–	–	–	SDIO_AOS_ CLK	–	–
SDIO_CMD	SDIO_CMD	–	–	–	–	–	–	–	SDIO_AOS_ CMD	–	–
SDIO_ DATA_0	SDIO_D0	–	–	–	–	–	–	–	SDIO_AOS_ D0	–	–
SDIO_ DATA_1	SDIO_D1	–	–	–	–	–	–	–	SDIO_AOS_ D1	–	–

Table 15. Pin Multiplexing

Pin	Function										
	1	2	3	4	5	6	7	8	9	10	11
SDIO_ DATA_2	SDIO_D2	–	–	–	–	–	–	–	SDIO_AOS_ D2	–	–
SDIO_ DATA_3	SDIO_D3	–	–	–	–	–	–	–	SDIO_AOS_ D3	–	–
RF_SW_ CTRL_5	RF_SW_ CTRL_5	GCI_GPIO_5	–	–	–	–	–	–	–	–	–
RF_SW_ CTRL_6	RF_SW_ CTRL_6	UART_ DBG_RX	SECI_IN	–	–	–	–	–	–	–	–
RF_SW_ CTRL_7	RF_SW_ CTRL_7	UART_ DBG_TX	SECI_OUT	–	–	–	–	–	–	–	–
RF_SW_ CTRL_8	RF_SW_ CTRL_8	SECI_IN	UART_ DBG_RX	–	–	–	–	–	–	–	–
RF_SW_ CTRL_9	RF_SW_ CTRL_9	SECI_OUT	UART_ DBG_TX	–	–	–	–	–	–	–	–
PWM0	PWM0	GPIO_2	GPIO_18	–	–	–	–	–	–	–	–
PWM1	PWM1	GPIO_3	GPIO_19	–	–	–	–	–	–	–	–
PWM2	PWM2	GPIO_4	GPIO_20	–	–	–	–	–	–	–	–
PWM3	PWM3	GPIO_5	GPIO_21	–	–	–	–	–	–	–	–
PWM4	PWM4	GPIO_6	GPIO_22	–	–	–	–	–	–	–	–
PWM5	PWM5	GPIO_8	GPIO_23	–	–	–	–	–	–	–	–
SPI0_MISO	SPI0_MISO	GPIO_17	GPIO_24	–	–	–	–	–	–	–	–
SPI0_CLK	SPI0_CLK	GPIO_18	GPIO_25	–	–	–	–	–	–	–	–
SPI0_MOSI	SPI0_MOSI	GPIO_19	GPIO_26	–	–	–	–	–	–	–	–
SPI0_CS	SPI0_CS	GPIO_20	GPIO_27	–	–	–	–	–	–	–	–
I2C0_SDATA	I2C0_SDATA	GPIO_21	GPIO_28	–	–	–	–	–	–	–	–
I2C0_CLK	I2C0_CLK	GPIO_22	GPIO_29	–	–	–	–	–	–	–	–
I2S_MCLK0	I2S_MCLK0	GPIO_23	GPIO_0	–	–	–	–	–	–	–	–
I2S_SCLK0	I2S_SCLK0	GPIO_24	GPIO_2	–	–	–	–	–	–	–	–
I2S_LRCLK0	I2S_LRCLK0	GPIO_25	GPIO_3	–	–	–	–	–	–	–	–
I2S_S DATAI0	I2S_ SDATAI0	GPIO_26	GPIO_4	–	–	–	–	–	–	–	–
I2S_ SDATAO0	I2S_ SDATAO0	GPIO_27	GPIO_5	–	–	–	–	–	–	–	–
I2S_ SDATAO1	I2S_ SDATAO1	GPIO_28	GPIO_6	–	–	–	–	–	–	–	–

Table 15. Pin Multiplexing

Pin	Function										
	1	2	3	4	5	6	7	8	9	10	11
I2S_SDATAI1	I2S_SDATAI1	GPIO_29	GPIO_8	–	–	–	–	–	–	–	–
I2S_MCLK1	I2S_MCLK1	GPIO_30	GPIO_17	–	–	–	–	–	–	–	–
I2S_SCLK1	I2S_SCLK1	GPIO_31	GPIO_30	–	–	–	–	–	–	–	–
I2S_LRCLK1	I2S_LRCLK1	GPIO_0	GPIO_31	–	–	–	–	–	–	–	–

12. I/O States

Table 16 provides I/O state information for the signals listed.

The following notations are used in Table 16:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 16. I/O States

Ball Name	I/O	Keeper[1]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[2] (REG_ON Held Low)	Out-of-Reset; Before Software Download (REG_ON High)	Power Rail
HIB_REG_ON_IN	I	N	Input; PD (Pull-down can be disabled.)	Input; PD (Pull-down can be disabled.)	Input	Input	–
REG_ON	I	N	Input; PD (Pull-down can be disabled.)	Input; PD (Pull-down can be disabled.)	Input; PD (of 200 kΩ)	Input; PD (of 200 kΩ)	–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high.	High-Z, NoPull	Open drain; active high	VDDO
GPIO_0	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_1	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_2	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_3	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_4	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_5	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO

Table 16. I/O States

Ball Name	I/O	Keeper[1]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[2] (REG_ON Held Low)	Out-of-Reset; Before Software Download (REG_ON High)	Power Rail
GPIO_6	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_7	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_8	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_9	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_10	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_11	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_12	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_13	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_14	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_15	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_16	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
RF_SW_CTRL (0 to 9)	I/O	Y	Output; NoPull	Output; NoPull	High-Z	Output; NoPull	VDDIO_RF

1. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in power-down state. If there is no keeper, and it is an input and there is NoPull, then the pad should be driven to prevent leakage due to floating pad (WL_REG_ON, for example).

2. In the power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.

13. Electrical Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

13.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 17 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 17. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC supply for VBAT and PA driver supply [1]	VBAT	–0.5 to +5.5	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for DDR I/O	VDDIO_DDR	–0.5 to 1.8	V
DC supply voltage for I^2S I/O	VDDIO_I2S	–0.5 to 3.9	V
DC supply voltage for RF switch I/O	VDDIO_RF	–0.5 to 3.9	V
DC supply voltage for Ethernet I/O	VDDIO_RMII	–0.5 to 3.9	V
DC supply voltage for SDIO I/O	VDDIO_SD	–0.5 to 3.9	V
DC input supply voltage for CLDO, LNLDO, and HSIC LDO[2]	–	–0.5 to 1.575	V
3.3V DC supply for USB	USB2_AVDD33	–0.5 to 3.9	V
3.3V DC supply voltage for RF analog[3]	VDD3P3RF	–0.5 to 3.6	V
1.35V DC supply voltage for RF analog[4]	VDD1P35RF	–0.5 to 1.5	V
1.2V DC supply voltage for RF analog[5]	VDD1P2RF	–0.5 to 1.26	V
1.2V DC supply voltage for analog circuits[6]	VDD1P2A	–0.5 to 1.26	V
DC supply voltage for the core[7]	VDDC	–0.5 to 1.32	V
DC supply voltage for OTP memory	OTP_VDD3P3	–0.5 to 3.9	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum junction temperature	T_j	125	°C

1. For the SR_VDDBAT5V and LDO_VDDBAT5V supplies.
2. For the LDO_VDD1P5 and WRF_XTAL_VDD1P35 supplies.
3. For the WRF_SYNTH_VDD3P3, WRF_PA_VDD3P3, and WRF_TXMIX_VDD supplies.
4. For WRF_PMU_VDD1P35 and WRF_AFE_VDD1P35 supplies.
5. For the WRF_SYNTH_VDD1P2 supply.
6. For the AVDD1P2_AUDIO, AVDD1P2, and HSIC_AVDD12 supplies.
7. For the VDD, HSIC_DVDD12, and HSIC2_DVDD2 supplies.

13.2 Environmental Ratings

The environmental ratings are shown in Table 18.

Table 18. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient temperature (T_A)	–30 to +85	°C	Functional operation
Storage temperature	–40 to +125	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

13.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 19. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/ JESD22-A114	1.5 kΩ	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/ JESD22-C101	250	V

13.4 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 20. Operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 20. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	2.3[1]	3.6	4.8	V
DC supply voltage for digital I/O	VDDIO	1.71	–	3.63	V
DC supply voltage for DDR I/O	VDDIO_DDR	1.35	1.5	1.65	V
DC supply voltage for I^2S I/O	VDDIO_I2S	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF[2]	3.13	3.3	3.6	V
DC supply voltage for Ethernet I/O	VDDIO_RMII	1.71	–	3.63	V
DC supply voltage for SDIO I/O	VDDIO_SD	1.71	–	3.63	V
DC input supply voltage for CLDO, LNLDO, and HSIC LDO	–	1.3	1.35	1.5	V
3.3V DC supply for USB	USB2_AVDD33	2.97	3.3	3.63	V
3.3V DC supply voltage for RF analog	VDD3P3RF[3]	3	3.3	3.45	V
1.35V DC supply voltage for RF analog	VDD1P35RF[3]	1.3	1.35	1.5	V
1.2V DC supply voltage for RF analog	VDD1P2RF[3]	1.1	1.2	1.26	V
1.2V DC supply voltage for analog	VDD1P2A[3]	1.1	1.2	1.26	V
DC supply voltage for core	VDDC	1.14	1.2	1.26	V
DC supply voltage for OTP memory	OTP_VDD3P3[2]	2.97	3.3	3.63	V

Table 20. Recommended Operating Conditions and DC Characteristics (Cont.)

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD[3]	1.62	1.8	1.98	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[4]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

1. The CYW43903 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3V < VBAT < 4.8V.
2. VDD3P3RF, which is an internally generated supply, can drive this node. There is sufficient current and the appropriate state is maintained during hibernation and sleep cycles.
3. Internally generated supply.
4. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

13.5 Power Supply Segments

The digital I/O's are placed in physical segments. The supply voltage for each segment can be independently selected.

Table 21 shows the power supply segments and the I/O pins associated with each segment.

Table 21. Power Supply Segments

Power Supply Segment	Pins
VDDIO	CLK_REQ, GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_6, GPIO_7, GPIO_8, GPIO_9, GPIO_10, GPIO_11, GPIO_12, GPIO_13, GPIO_14, GPIO_15, GPIO_16, I2C0_CLK, I2C0_SDATA, I2C1_CLK, I2C1_SDATA, JTAG_SEL, PWM0, PWM1, PWM2, PWM3, PWM4, PWM5, SFL_CLK, SFL_CS, SFL_IO0, SFL_IO1, SFL_IO2, SFL_IO3, SPI0_CLK, SPI0_CS, SPI0_MISO, SPI0_SISO, SPI1_CLK, SPI1_CS, SPI1_MISO, SPI1_SISO, SRSTN, UART0_CTS, UART0_RTS, UART0_RXD, UART0_TXD, USB2_DSEL
VDDIO_DDR	DDR_A_0, DDR_A_1, DDR_A_2, DDR_A_3, DDR_A_4, DDR_A_5, DDR_A_6, DDR_A_7, DDR_A_8, DDR_A_9, DDR_A_10, DDR_A_11, DDR_A_12, DDR_A_13, DDR_A_14, DDR_A_15, DDR_BANK_0, DDR_BANK_1, DDR_BANK_2, DDR_CAS_N, DDR_CKE, DDR_CLK, DDR_CS_N, DDR_D_0, DDR_D_1, DDR_D_2, DDR_D_3, DDR_D_4, DDR_D_5, DDR_D_6, DDR_D_7, DDR_D_8, DDR_D_9, DDR_D_10, DDR_D_11, DDR_D_12, DDR_D_13, DDR_D_14, DDR_D_15, DDR_DM_0, DDR_DM_1, DDR_DQS_0, DDR_DQS_1, DDR_ODT, DDR_RAS_N, DDR_RESET_N, DDR_WE_N
VDDIO_I2S	I2S_LRCLK0, I2S_LRCLK1, I2S_MCLK0, I2S_MCLK1, I2S_SCLK0, I2S_SCLK1, I2S_SDATAI0, I2S_SDATAI1, I2S_SDATAO0, I2S_SDATAO1
VDDIO_RF	RF_SW_CTRL_0, RF_SW_CTRL_1, RF_SW_CTRL_2, RF_SW_CTRL_3, RF_SW_CTRL_4, RF_SW_CTRL_5, RF_SW_CTRL_6, RF_SW_CTRL_7, RF_SW_CTRL_8, RF_SW_CTRL_9
VDDIO_RMII	RMII_G_COL, RMII_G_CRS, RMII_G_RXC, RMII_G_RXD0, RMII_G_RXD1, RMII_G_RXD2, RMII_G_RXD3, RMII_G_RXDV, RMII_G_TXC, RMII_G_TXD0, RMII_G_TXD1, RMII_G_TXD2, RMII_G_TXD3, RMII_G_TXEN, RMII_MDC, RMII_MDIO

13.6 DDR3 SDRAM Memory Interface AC and DC Characteristics

Table 22 provides the AC and DC characteristics of the DDR3 SDRAM interface.

Table 22. AC and DC Characteristics of the DDR3 SDRAM Interface

Parameter	Symbol	Min	Max	Units
Input logic high (DC)	V_{IHDC}	DDR_VREF + 0.1	DDR_OVDD	V
Input logic low (DC)	V_{ILDC}	DVSS	DDR_VREF – 0.1	V
Input logic high (AC reference only)	V_{IHAC}	DDR_VREF + 0.15	–	V
Input logic low (AC reference only)	V_{ILAC}	–	DDR_VREF – 0.15	V
Output logic high (at IOH min.)	V_{OH}	DDR_OVDD – 0.4	–	V
Output logic low (at IOL min.)	V_{OL}	–	0.4	V
Output source current (at VOH min.)	I_{OH}	7	–	mA
Output sink current (at VOL max.)	I_{OL}	7.5	–	mA
Differential DQS input low (AC)	VIL..DIFF(AC)	–	0.30	V
Differential DQS input high (AC)	VIH..DIFF(AC)	0.30	–	V

13.7 Ethernet MAC Controller (MII/RMII) DC Characteristics

Table 23. MII Recommended Operating Condition

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	GMAC_VDDIO (MII/RMII)	3.14	3.47	V

13.8 GPIO, UART, and JTAG Interfaces DC Characteristics

Table 24. GPIO, UART, and JTAG Interfaces

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Logic input high voltage	V_{IH}	2.0	VDDIO + 0.5	V	–
Logic input low voltage	V_{IL}	–0.5	0.8	V	–
Logic output high voltage	V_{OH}	2.4	–	V	–
Logic output low voltage	V_{OL}	–	0.4	V	–

14. WLAN RF Specifications

14.1 Introduction

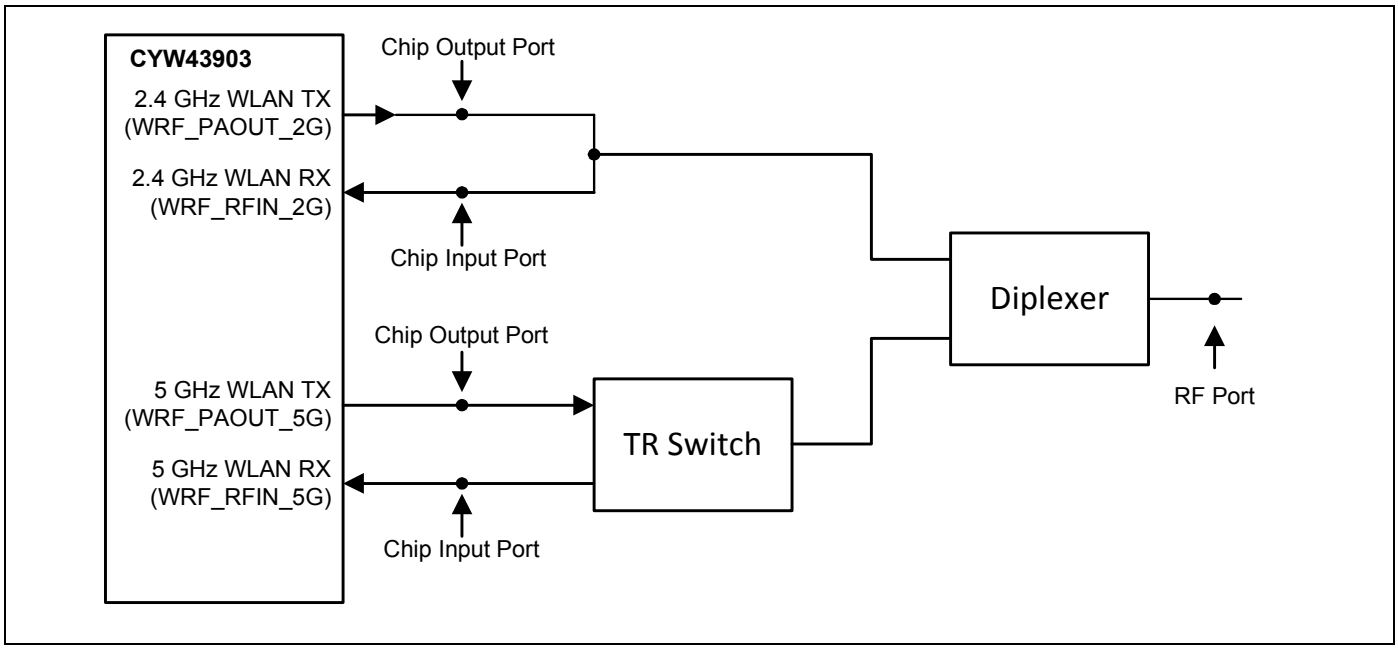
The CYW43903 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radio.

Note: Values in this section of the data sheet are design goals and are subject to change based on device characterization results.

Unless otherwise stated, limit values apply for the conditions specified in Table 18, “Environmental Ratings,” and Table 20, “Recommended Operating Conditions and DC Characteristics,”. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 17. Port Locations for WLAN Testing



14.2 2.4 GHz Band General RF Specifications

Table 25. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

14.3 WLAN 2.4 GHz Receiver Performance Specifications

Note: he specifications shown in Table 26 apply at the chip ports, unless otherwise defined.

Table 26. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS		–	–98.9	–	dBm
	2 Mbps DSSS		–	–96.0	–	dBm
	5.5 Mbps DSSS		–	–93.9	–	dBm
	11 Mbps DSSS		–	–90.4	–	dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM		–	–95.0	–	dBm
	9 Mbps OFDM		–	–93.8	–	dBm
	12 Mbps OFDM		–	–92.7	–	dBm
	18 Mbps OFDM		–	–90.3	–	dBm
	24 Mbps OFDM		–	–87.1	–	dBm
	36 Mbps OFDM		–	–83.6	–	dBm
	48 Mbps OFDM		–	–79.3	–	dBm
	54 Mbps OFDM		–	–78.0	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) [1] Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS0		–	–94.6	–	dBm
	MCS1		–	–92.1	–	dBm
	MCS2		–	–89.8	–	dBm
	MCS3		–	–86.6	–	dBm
	MCS4		–	–83.0	–	dBm
	MCS5		–	–78.3	–	dBm
	MCS6		–	–76.6	–	dBm
	MCS7		–	–75.0	–	dBm
Input in-band IP3	Maximum LNA gain		–	–8	–	dBm
	Minimum LNA gain		–	+9	–	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6, 9, 12 Mbps (10% PER, 1024 octets)		–9.5	–	–	dBm
	@ MCS0–2 rates (10% PER, 4095 octets)		–9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps (10% PER, 1024 octets)		–14.5	–	–	dBm
	@ MCS3–7 rates (10% PER, 4095 octets)		–14.5	–	–	dBm
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes.)	**Desired and interfering signal 30 MHz apart**					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB

Table 26. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/ Notes.)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/ Notes.)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
Maximum receiver gain	–	–	–	66	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[2]	Range –95[3] dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		10	11.5	13	dB
Receiver cascaded noise figure	At maximum gain		–	4	–	dB

1. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.
2. The minimum and maximum values shown have a 95% confidence level.
3. –95 dBm with calibration at time of manufacture, –92 dBm without calibration.

14.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note: Unless otherwise noted, the values shown in Table 27 apply at the chip ports.

Table 27. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
RF port TX power EVM[1] (highest power setting, 25°C, and VBAT = 3.6)	DSS/CCK	–9 dB	–	20.5	–	dBm
	OFDM, BPSK	–8 dB	–	20	–	dBm
	OFDM, QPSK	–13 dB	–	20	–	dBm
	OFDM, 16-QAM	–19 dB	–	19	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	–	19	–	dBm
	OFDM, 64-QAM (MCS7, HT20)	–27 dB	–	18.5	–	dBm
OFDM EVM[2] (25°C, VBAT = 3.6V)	OFDM, BPSK	5 dBm	–29	–31	–	dB
	OFDM, 64-QAM	5 dBm	–31	–33	–	dB
	MCS7	5 dBm	–33	–35	–	dB
Phase noise	37.4 MHz crystal, integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies to 10 dBm to 20 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port TX	Z_o = 50Ω		–	6	–	dB

1. This specification row indicates the linear power specification as measured from the chip output port. The requirement is in dBm (TX power). The ratio (dB) in the Conditions/Notes column is the EVM.

2. This specification row indicates the EVM floor. The requirement is in dB (EVM). The power in the Conditions/Notes column is the TX power specification in dBm.

14.5 WLAN 5 GHz Receiver Performance Specifications

Note: Unless otherwise noted, the values shown in Table 28 apply at the chip ports.

Table 28. WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
RX sensitivity [1] IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps OFDM		–	–93.6	–	dBm
	9 Mbps OFDM		–	–92.4	–	dBm
	12 Mbps OFDM		–	–91.3	–	dBm
	18 Mbps OFDM		–	–88.9	–	dBm
	24 Mbps OFDM		–	–85.7	–	dBm
	36 Mbps OFDM		–	–82.3	–	dBm
	48 Mbps OFDM		–	–77.9	–	dBm
	54 Mbps OFDM		–	–76.6	–	dBm
RX sensitivity [1] IEEE 802.11n (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS0		–	–93.2	–	dBm
	MCS1		–	–90.7	–	dBm
	MCS2		–	–88.4	–	dBm
	MCS3		–	–85.2	–	dBm
	MCS4		–	–81.6	–	dBm
	MCS5		–	–76.9	–	dBm
	MCS6		–	–75.2	–	dBm
	MCS7		–	–73.6	–	dBm
RX sensitivity [1] IEEE 802.11n (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates					
	MCS0		–	–90.3	–	dBm
	MCS1		–	–87.5	–	dBm
	MCS2		–	–84.9	–	dBm
	MCS3		–	–81.8	–	dBm
	MCS4		–	–78.3	–	dBm
	MCS5		–	–73.9	–	dBm
	MCS6		–	–72.7	–	dBm
	MCS7		–	–71.2	–	dBm
Input in-band IP3	Maximum LNA gain		–	–12	–	dBm
	Minimum LNA gain		–	+4	–	dBm
Maximum receive level @ 5 GHz	@ 6, 9, 12 Mbps (10% PER, 1024 octets)		–9.5	–	–	dBm
	@ MCS0–2 rates (10% PER, 4095 octets)		–9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps (10% PER, 1024 octets)		–14.5	–	–	dBm
	@ MCS3–7 rates (10% PER, 4095 octets)		–14.5	–	–	dBm
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/ Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB

Table 28. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[2] octet PSDU with desired signal level as specified in Condition/ Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	66	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[3]	Range –92 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		10	–	13	dB
Receiver cascaded noise figure	At maximum gain		–	5	–	dB

1. For PCIE derate the 5 GHz RX sensitivity by 1.5 dB
2. For 65 Mbps, the size is 4096.
3. The minimum and maximum values shown have a 95% confidence level.

14.6 WLAN 5 GHz Transmitter Performance Specifications

Note: Unless otherwise noted, the values shown in Table 29 apply at the chip ports.

Table 29. WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
RF port TX power EVM[1] (highest power setting, 25°C, and VBAT = 3.6)	OFDM, QPSK	–13 dB	–	20	–	dBm
	OFDM, 16-QAM	–19 dB	–	18.5	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	–	17	–	dBm
	OFDM, 64-QAM (MCS7, HT20)	–27 dB	–	16.5	–	dBm
OFDM EVM[2] (25°C, VBAT = 3.6V)	OFDM, BPSK	0 dBm	–	–30	–	dB
	OFDM,64-QAM	0 dBm	–	–33	–	dB
	MCS7	0 dBm	–	–34	–	dB
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Closed loop TX power variation at highest power level setting	Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range.		–	–	±2.0	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Z_o = 50Ω		–	6	–	dB

1. This specification row indicates the linear power specification as measured from the chip output port. The requirement is in dBm (TX power). The ratio (dB) in the Conditions/Notes column is the EVM.

2. This specification row indicates the EVM floor. The requirement is in dB (EVM). The power in the Conditions/Notes column is the TX power specification in dBm.

14.7 General Spurious Emissions Specifications

This section provides the TX and RX spurious emissions specifications for the WLAN 2.4 GHz and 5 GHz bands. The recommended spectrum analyzer settings for the spurious emissions specifications are provided in Table 30.

Table 30. Recommended Spectrum Analyzer Settings

Parameter	Setting
Resolution bandwidth (RBW)	1 MHz
Video bandwidth (VBW)	1 MHz
Sweep	Auto
Span	100 MHz
Detector	Maximum peak
Trace	Maximum hold
Modulation	OFDM

14.7.1 Transmitter Spurious Emissions Specifications

2.4 GHz Band Spurious Emissions

20-MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/18 specifications for channel 2442 are listed in Table 31.

- AFE=VCO/18
- AFE=VCO/16
- AFE=VCO/8
- AFE=VCO/6

Table 31. 2.4 GHz Band, 20-MHz Channel Spacing TX Spurious Emissions Specifications [1]

Spurious Frequency	Power (dBm)	Frequency (Fch; MHz) Channel 2442	
		Typical (dBm)	Maximum (dBm)
HD2	–5	–58.7	–56.6
HD3	–5	–71.7	–68.9
HD4	–5	–57.2	–50.2
VCO	–5	–45.7	–43.7
VCOx2	–5	–71.5	–69.0
VCOx3	–5	–85.2	–74.1
AFEx3	–5	–	–
AFEx4	–5	–	–
AFEx5	–5	–	–
AFEx6	–5	–78.4	–73.5
AFEx7	–5	–77.3	–76.1
AFEx8	–5	–73.6	–73.4
AFEx9	–5	–70.9	–69.9
AFEx10	–5	–81.1	–78.8
AFEx11	–5	–70.3	–69.1
AFEx13	–5	–72.0	–71.0
AFEx14	–5	–76.2	–73.8
AFEx15	–5	–79.3	–73.6
AFEx16	–5	–82.5	–77.9
AFEx17	–5	–85.3	–77.7
AFEx19	–5	–83.4	–77.6
AFEx20	–5	–83.9	–76.5
AFEx21	–5	–78.7	–74.9
AFEx22	–5	–82.1	–76.2
AFEx23	–5	–87.1	–77.6

1. VCO = 1.5 × Fch, where Fch is the center frequency of the channel.

5 GHz Band Spurious Emissions

20-MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/18 specifications for channels 5180, 5500, and 5825 are listed in Table 32.

- AFE=VCO/18
- AFE=VCO/16
- AFE=VCO/8
- AFE=VCO/6

Table 32. 5 GHz Band, 20-MHz Channel Spacing TX Spurious Emissions Specifications

Spurious Frequency	Power (dBm)	Frequency (Fch; MHz)					
		5180 [1]		5500 [1]		5825 [1]	
		Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)
HD2	–5	–57.1	–56.3	–58.0	–56.9	–59.6	–58.3
HD3	–5	–71.8	–71.0	–70.8	–70.1	–69.6	–69.1
VCO	–5	–62.6	–54.2	–54.3	–54.0	–50.7	–50.3
VCOx2	–5	–74.7	–72.4	–76.2	–69.9	–71.2	–67.0
VCOx3	–5	–57.1	–56.3	–58.0	–56.9	–59.6	–58.3
AFEx2	–5	–81.6	–80.5	–81.5	–80.6	–81.0	–80.0
AFEx4	–5	–81.2	–80.1	–81.3	–80.4	–80.8	–80.0
AFEx6	–5	–80.9	–80.0	–80.7	–80.0	–80.5	–80.0
AFEx12	–5	–	–	–	–	–	–
AFEx15	–5	–	–	–	–	–	–
Fch + AFE	–5	–75.6	–74.7	–76.4	–75.5	–76.1	–75.0
Fch + AFEx2	–5	–77.1	–76.2	–77.1	–76.2	–76.5	–75.6
Fch + AFEx3	–5	–76.8	–74.5	–77.1	–74.9	–76.4	–75.9
Fch – AFE	–5	–76.6	–75.6	–76.4	–75.5	–75.5	–75.5
Fch – AFEx2	–5	–77.3	–76.1	–76.8	–75.5	–76.8	–76.3
Fch – AFEx3	–5	–77.9	–76.5	–77.2	–76.5	–76.0	–75.9

1. VCO = (2/3) × Fch, where Fch is the center frequency of the channel.

40-MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/9 specifications for channels 5190, 5510, and 5795 are listed in Table 33.

- AFE=VCO/18
- AFE=VCO/16
- AFE=VCO/8
- AFE=VCO/6

Table 33. 5 GHz Band, 40-MHz Channel Spacing TX Spurious Emissions Specifications

Spurious Frequency	Power (dBm)	Frequency (Fch; MHz)					
		5190 [1]		5510 [2]		5795 [2]	
		Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)
HD2	–5	–56.9	–56.4	–58.5	–57.3	–58.7	–57.3
HD3	–5	–72.2	–71.7	–72.3	–71.7	–71.7	–71.2
VCO	–5	–50.6	–50.0	–53.7	–53.4	–51.4	–50.7
VCOx2	–5	–71.1	–69.8	–76.9	–70.0	–74.5	–67.9
VCOx3	–5	–75.9	–75.1	–58.5	–57.3	–58.7	–57.3
AFEx2	–5	–81.0	–79.8	–81.2	–79.8	–81.4	–80.2
AFEx4	–5	–79.0	–77.7	–80.0	–78.9	–78.3	–77.5
AFEx6	–5	–76.8	–75.3	–78.5	–76.2	–80.8	–75.2
AFEx12	–5	–	–	–74.5	–73.6	–79.0	–77.8
AFEx15	–5	–76.1	–72.9	–73.9	–71.1	–70.6	–70.5
Fch + AFE	–5	–78.7	–76.1	–78.6	–77.7	–77.5	–75.9
Fch + AFEx2	–5	–78.5	–76.2	–78.0	–77.2	–76.3	–73.4
Fch + AFEx3	–5	–	–	–78.6	–78.0	–78.2	–77.6
Fch – AFE	–5	–79.0	–77.3	–78.6	–77.3	–79.1	–78.3
Fch – AFEx2	–5	–79.0	–78.0	–79.2	–78.6	–79.2	–78.6
Fch – AFEx3	–5	–	–	–79.7	–79.0	–79.6	–79.0

1. VCO = (3/4) x Fch, where Fch is the center frequency of the channel.
2. VCO = (2/3) × Fch, where Fch is the center frequency of the channel.

14.7.2 Receiver Spurious Emissions Specifications

Table 34. 2G and 5G General Receiver Spurious Emissions

Band	Frequency Range	Typical	Maximum	Unit
2G	2.4 GHz < f < 2.5 GHz	–75.5	–74.1	dBm
	3.6 GHz < f < 3.8 GHz	–52.8	–50.9	dBm
5G	5150 MHz < f < 5850 MHz	–57.7	–56.1	dBm
	3.45 GHz < f < 3.9 GHz	–48.6	–47.6	dBm

15. Internal Regulator Electrical Specifications

15.1 Core Buck Switching Regulator

Note: Values in this data sheet are design goals and are subject to change based on device characterization results.

Note: Functional operation is not guaranteed outside of the specification limits provided in this section.

Table 35. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Unit
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.6	4.8[1]	V
PWM mode switching frequency	CCM, load > 100 mA VBAT = 3.6V.	–	4	–	MHz
PWM output current	–	–	–	550	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V.	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static load. Max. ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor with min. effective L > 1.05 µH, cap. + board total – ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak efficiency at 200 mA load.	78	86	–	%
PFM mode efficiency	10 mA load current.	70	81	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V.	–	400	500	µs
External inductor	0806 size, 2.2 µH, DCR = 0.11Ω, ACR = 1.18Ω @ 4 MHz.	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, 4.7 µF ±20%, 6.3V.	2.0[2]	4.7	10[3]	µF
External input capacitor	For SR_VDDBAT5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±4.7 µF ±20%, 6.3V.	0.67[2]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V.	40	–	–	µs

1. The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
2. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
3. Total capacitance includes those connected at the far end of the active load.

15.2 3.3V LDO (LDO3P3)

Table 36. LDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = V_o + 0.2V = 3.5V dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.6	4.8[1]	V
Output current	–	0.001	–	450	mA
Nominal output voltage, V_o	Default = 3.3V.	–	3.3	–	V
Dropout voltage	At max. load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load.	–	–	85	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max. load.	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 450 mA.	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 3.3V, C_o = 4.7 µF, Max load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402,(ESR: 5 mΩ–240 mΩ), ± 10%, 10V.	1.0[2]	4.7	10	µF
External input capacitor	For LDO_VDDBAT5V pin (shared with band gap) ceramic, X5R, 0402, (ESR: 30mΩ–200 mΩ), ± 10%, 10V. Not needed if sharing 4.7 µF VBAT capacitor with SR_VDDBAT5V.	–	4.7	–	µF

1. The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.

2. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

15.3 CLDO

Table 37. CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	350	mA
Output voltage, V_o	Programmable in 10 mV steps. Default = 1.2.V.	0.95	1.2	1.26	V
Dropout voltage	At max. load.	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation.	–4	–	+4	%
Quiescent current	No load.	–	26	–	µA
	200 mA load.	–	2.48	–	mA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load.	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA.	–	0.02	0.05	mV/mA
Leakage current	Power down.	–	10	40	µA
	Bypass mode.	–	2	6	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF.	20	–		dB
Start-up time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO turn-on time	LDO turn-on time when the rest of the chip is up.	–	140	180	µs
External output capacitor, C_o	Total ESR: 5 mΩ–240 mΩ.	3.76[1]	4.7	–	µF
External input capacitor	Only use an external input capacitor at the LDO_VDD1P5 pin if it is not supplied from the CBUCK output.	–	1	2.2	µF

1. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

15.4 LNLDO

Table 38. LNLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. $V_{IN} = V_O + 0.15V = 1.35V$ (where $V_O = 1.2V$)dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V.	1.1	1.2	1.275	V
Dropout voltage	At maximum load.	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation.	–4	–	+4	%
Quiescent current	No load.	–	44	–	µA
	Max. load.	–	970	990	µA
Line regulation	V_{in} from (V_o + 0.1V) to 1.5V, 150 mA load.	–	–	5	mV/V
Load regulation	Load from 1 mA to 150 mA.	–	0.02	0.05	mV/mA
Leakage current	Power-down.	–	–	10	µA
Output noise	@30 kHz, 60–150 mA load C_o = 2.2 µF. @100 kHz, 60–150 mA load C_o = 2.2 µF.	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V.	20	–	–	dB
LDO turn-on time	LDO turn-on time when the rest of the chip is up.	–	140	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ.	0.5[1]	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at the LDO_VDD1P5 pin if it is not supplied from the CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ.	–	1	2.2	µF

1. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

15.5 HSIC LDO

Table 39. HSIC LDO Specifications

Parameter	Conditions and Comments	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. V_{in}= V_o + 0.15V = 1.35V (for V_o = 1.2V). The dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V.	1.1	1.2	1.275	V
Dropout voltage	At max. load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation.	–4	–	+4	%
Output current	Peak load = 80 mA, average = 35 mA	0.1	–	55	mA
Quiescent current	No load	–	10	12	µA
	55 mA load	–	550	570	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V; 200 mA load	–	–	5	mV/V
Load regulation	load from 1mA to 200 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Leakage current	Powered down. Junction temperature is 85°C.	–	5	20	µA
	Bypass mode	–	0.2	1.5	µA
PSRR	@1 kHz, $V_{in} \geq V_o$ + 0.15V, Co = 4.7 µF	20	–	–	dB
Start-up time of PMU	VIO up and steady. Time from REG_ON rising edge to CLDO reaching 99% of V_o.	–	530	700	us
LDO turn-on time	The LDO turn-on time when the rest of the chip is up.	–	140	180	us
Inrush current	Vin=Vo+0.15V to 1.5V, Co=0.47uF, no load	–	60	70	mA
External output capacitor, C_o	Ceramic, X5R, size 0201, max. 6.3V, 20% tolerance	0.27	0.47	–	µF
External input capacitor	Only use an external input capacitor at the LDO_VDD1P5 pin if it is not supplied from the CBUCK output.	–	1	–	µF

16. System Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Note: Unless otherwise stated, these values apply for the conditions specified in Table 20, “Recommended Operating Conditions and DC Characteristics,”.

16.1 WLAN Current Consumption

The tables in this subsection show the typical, total current used by the CYW43903. Current values may be measured with the APPS core powered off. The first column of the table, the mode description, will state the power condition of the APPS core.

16.1.1 2.4 GHz Mode

Table 40. 2.4 GHz Mode WLAN Current Consumption

Mode	V_{BAT} = 3.6V [1] (µA)	VDDIO = VDDIO_HIB = 3.3V [1, 2, 3] (µA)
Sleep Modes		
Radio off [4]	3	3
Sleep [5, 6]	6	160
IEEE Power Save, DTIM=1, single RX, APPS powered down [7]	2180	160
IEEE Power Save, DTIM=3, single RX, APPS powered down [8]	680	160
IEEE Power Save, DTIM=9, single RX, APPS powered down	233	160
Active Modes		
Continuous RX mode MCS7, HT20, 1SS, APPS powered up [9, 10]	57,200	60
CRS-HT20, APPS powered up [11]	55,200	60
Continuous TX mode 1 Mbps, APPS powered up [12]	336,000	60
Continuous TX mode MCS7, HT20, 1SS, 1 TX, APPS powered up [12]	337,900	60
Ping Modes		
Ping to associated access point [12]	336,000	60
Sleep	6	160

1. Typical silicon.
2. VIO is specified with all pins idle (not switching) and not driving any loads.
3. Excludes VDDIO_USB, VDDIO_RMII, VDDIO_I2S, VDDIO_DDR, and VDDIO_SD.
4. REG_ON is low or the device is in hibernation, and all supplies are present.
5. REG_ON is high. APPS domain is powered down. WLAN domain is in low-power state retention mode. Top level is powered up.
6. Inter-beacon current.
7. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3× DTIM intervals.
8. Beacon interval = 307.2 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3× DTIM intervals.
9. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
10. Measured using packet engine test mode.
11. Carrier sense (CCA) when no carrier present.
12. Duty cycle is 100%.

16.1.2 5 GHz Mode

Table 41. 5 GHz Mode WLAN Current Consumption

Mode	V_{BAT} = 3.6V [1] (µA)	VDDIO = VDDIO_HIB = 3.3V [1, 2, 3] (µA)
Sleep Modes		
Radio off [4]	3	3
Sleep [5, 6]	6	160
IEEE Power Save, DTIM=1, single RX, APPS powered down [7]	1390	160
IEEE Power Save, DTIM=3, single RX, APPS powered down [8]	470	160
IEEE Power Save, DTIM=9, single RX, APPS powered down	160	160
Active Modes		
Continuous RX mode MCS7, HT20, 1SS, APPS powered up [9, 10]	72,400	60
Continuous RX mode MCS7, HT40, 1SS, APPS powered up [9, 10]	84,700	60
CRS-HT20, APPS powered up [11]	70,200	60
CRS-HT40, APPS powered up [11]	79,500	60
Continuous TX mode MCS7, HT20, 1SS, 1 TX, APPS powered up [12]	326,000	60
Continuous TX mode MCS7, HT40, 1SS, 1 TX, APPS powered up [12]	311,000	60
Ping Modes		
Ping to associated access point [12]	327,000	60
Sleep	6	160

1. Typical silicon.
2. VIO is specified with all pins idle (not switching) and not driving any loads.
3. Excludes VDDIO_USB, VDDIO_RMII, VDDIO_I2S, VDDIO_DDR, and VDDIO_SD.
4. REG_ON is low or the device is in hibernation, and all supplies are present.
5. REG_ON is high. APPS domain is powered down. WLAN domain is in low-power state retention mode. Top level is powered up.
6. Inter-beacon current.
7. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3× DTIM intervals.
8. Beacon interval = 307.2 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3× DTIM intervals.
9. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
10. Measured using packet engine test mode.
11. Carrier sense (CCA) when no carrier present.
12. Duty cycle is 100%.

17. Interface Timing and AC Characteristics

17.1 DDR3 SDRAM AC Timing Characteristics

Figure 18. DDR3 DRAM Address and Control Timing

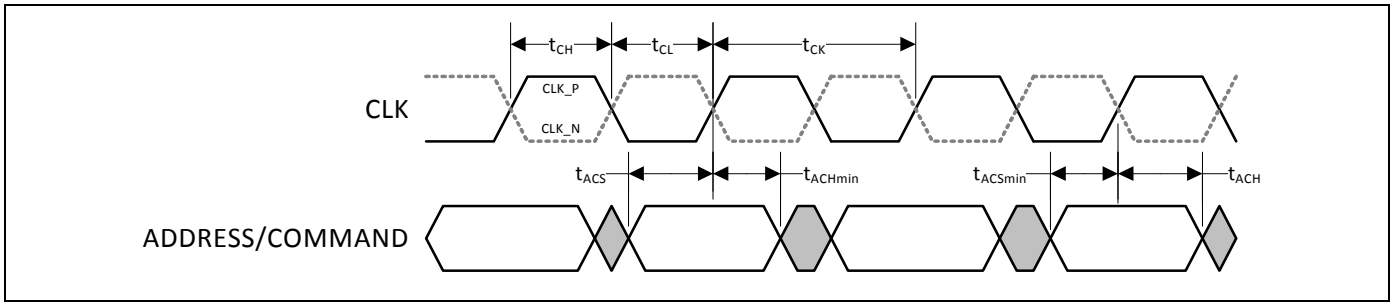


Figure 19. DDR3 DRAM Read Timing

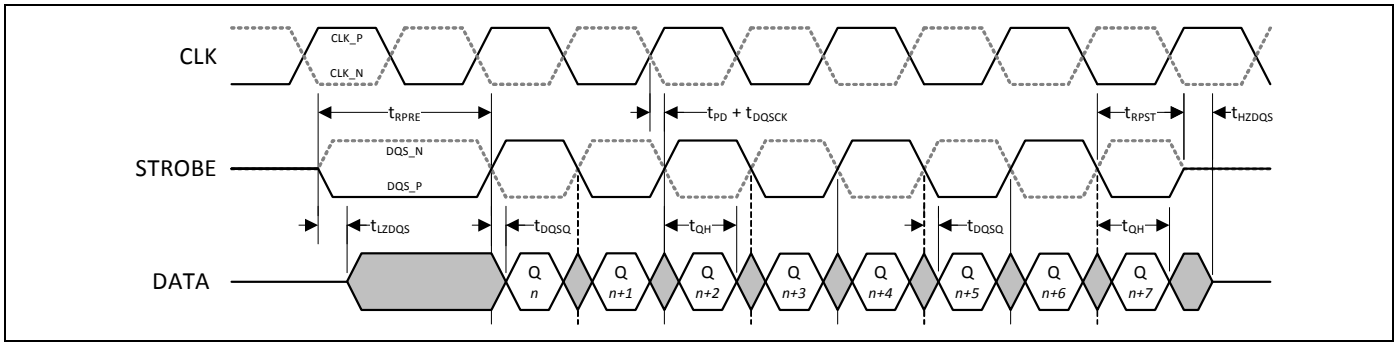


Figure 20. DDR3 DRAM Write Timing

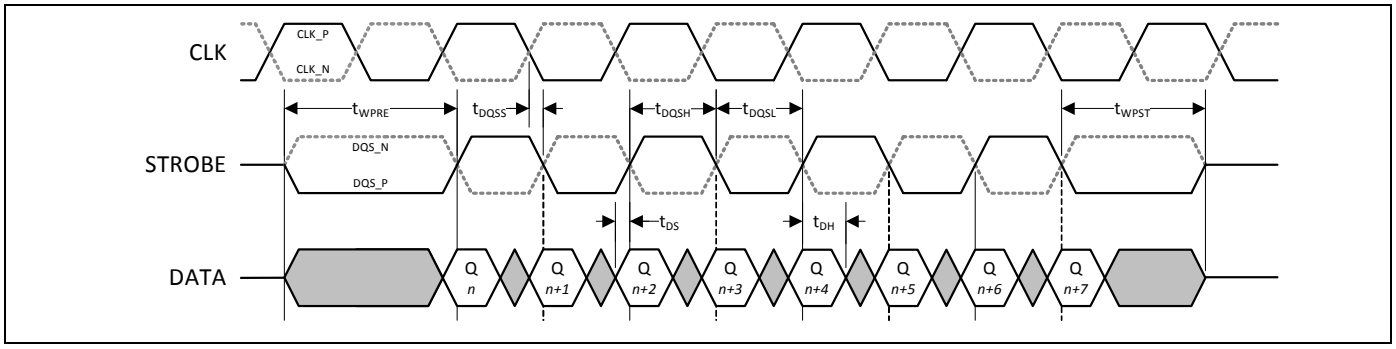


Table 42. DDR3 DRAM Interface Timing

Parameter	Symbol	Minimum	Maximum	Unit
Address and Control Timing				
CLK period	t_{CK}	3.125	–	ns
CLK pulse width (high)	t_{CH}	1.42	1.49	t_{ck}
CLK pulse width (low)	t_{CL}	1.42	1.49	t_{ck}
CLK periodic jitter	$t_{JIT(per)}$	–70	70	ps
ADDRESS/COMMAND output setup time	t_{ACS}	170	–	ps
ADDRESS/COMMAND output hold time	t_{ACH}	120	–	ps
Write timing				
WRITE preamble	t_{WPRE}	0.9	–	t_{ck}
WRITE post-amble	t_{WPST}	0.3	–	t_{ck}
DQS pulse width (high)	t_{DQSH}	0.45	0.55	t_{ck}
Positive DQS latching edge to associated CLK edge	t_{DQSS}	–0.25	0.25	t_{ck}
DQ-DQS output setup time	t_{DS}	125	–	ps
DQ-DQS output hold time	t_{DH}	150	–	ps
DQS falling edge to CLK rising edge—setup time	t_{DSS}	0.2	–	t_{ck}
DQS falling edge from CLK rising edge—hold time	t_{DSH}	0.2	–	t_{ck}
Read timing				
DQS output access time from CLK	t_{DQSCK}	–400	400	ps
READ preamble	t_{RPRE}	0.9	–	t_{ck}
READ post-amble	t_{RPST}	0.3		t_{ck}
DQS low-Z time	t_{LZDQS}	–800	400	ps
DQS high-Z time	t_{HZDQS}	–	400	ps
DQ-DQS input setup time (per group, per access)	t_{DQSQ}	–	200	ps
DQ-DQS input hold time	t_{QH}	0.38	–	t_{ck}

Note: These DDR3 parameter values are subject to change based on final characterization results.

17.2 Ethernet MAC (MII/RMII) Interface Timing

17.2.1 MII Receive Packet Timing

Figure 21 and Table 43 provide the MII receive packet timing.

Figure 21. MII Receive Packet Timing

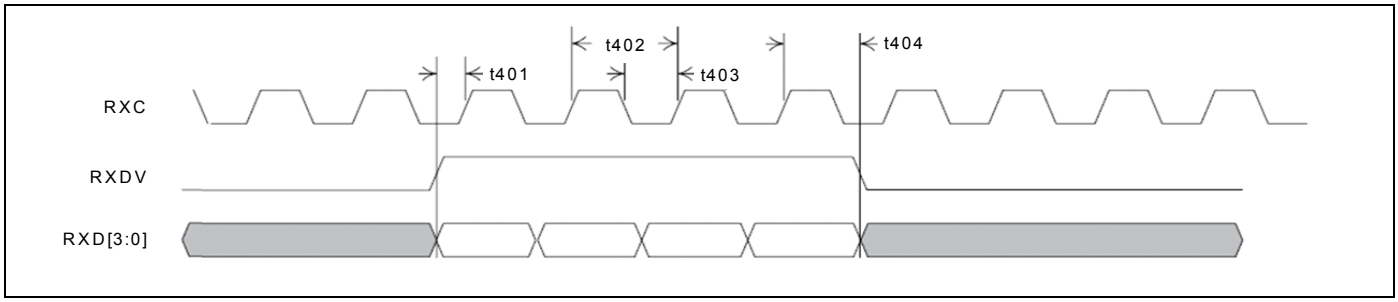


Table 43. MII Receive Packet Timing Parameters

Parameter	Description	Minimum	Typical	Maximum	Units
t401	RXDV and RXD[3:0] to RXC rising setup time	10	–	–	ns
t402	RXC clock period (10BASE-T mode)	–	400	–	ns
	RXC clock period (100BASE-TX mode)	–	40	–	ns
t403	RXC low/high time (10BASE-T mode)	160	–	240	ns
	RXC low/high time (100BASE-TX mode)	16	–	24	ns
t404	RXDV and RXD[3:0] to RXC rising hold time	10	–	–	ns
–	Duty cycle	40	50	60	%

17.3 MII Transmit Packet Timing

Figure 22 and Table 44 provide the MII transmit packet timing.

Figure 22. MII Transmit Packet Timing

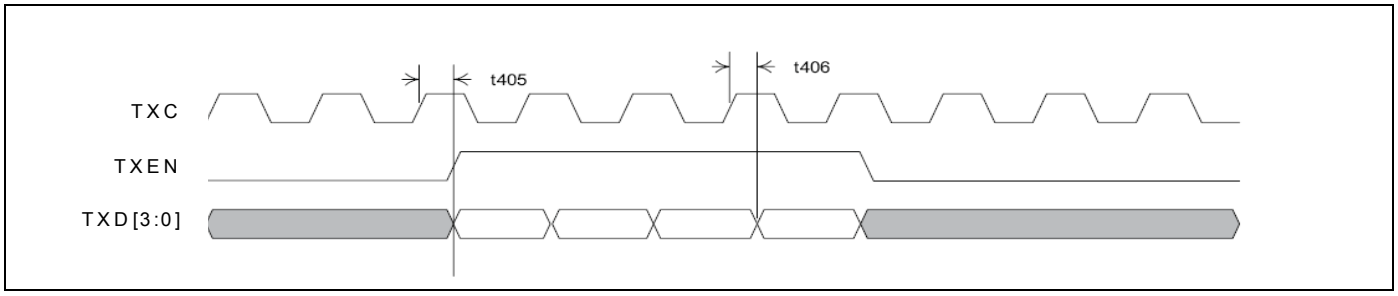


Table 44. MII Transmit Packet Timing Parameters

Parameter	Description	Minimum	Typical	Maximum	Units
t405	TXC high to TXEN and TXD[3:0] valid	0	–	25	ns
t406	TXC high to TXEN and TXD[3:0] invalid (hold)	0	–	–	ns

17.4 RMII Receive Packet Timing

Figure 23 and Table 45 provide the RMII receive packet timing.

Figure 23. RMII Receive Packet Timing

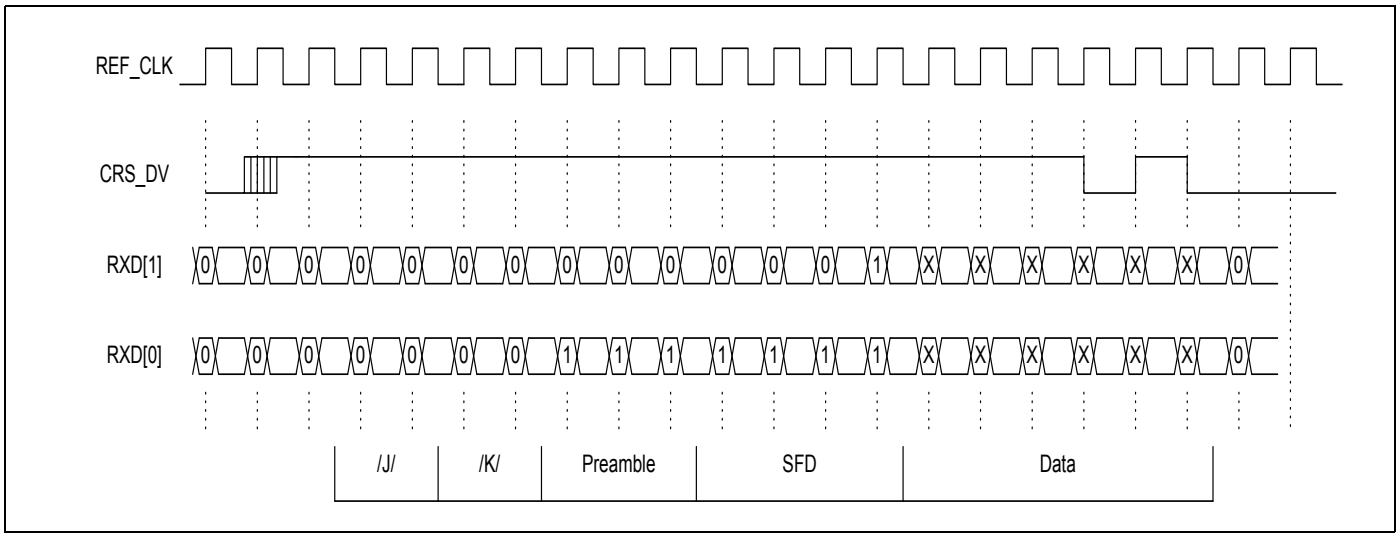


Table 45. RMII Receive Packet Timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
REF_CLK Cycle Time	–	–	20	–	ns
RXD[1:0], RXER, CRS_DV Output delay from REF_CLK rising	–	2	–	10	ns

Notes:

1. In 10 Mbps mode, there are ten REF_CLK periods per data period.
2. The receiver accounts for differences between the local REF_CLK and the recovered clock through use of sufficient elasticity buffering.

17.5 RMII Transmit Packet Timing

Figure 24 and Table 46 provide the RMII transmit packet timing.

Figure 24. RMII Transmit Packet Timing

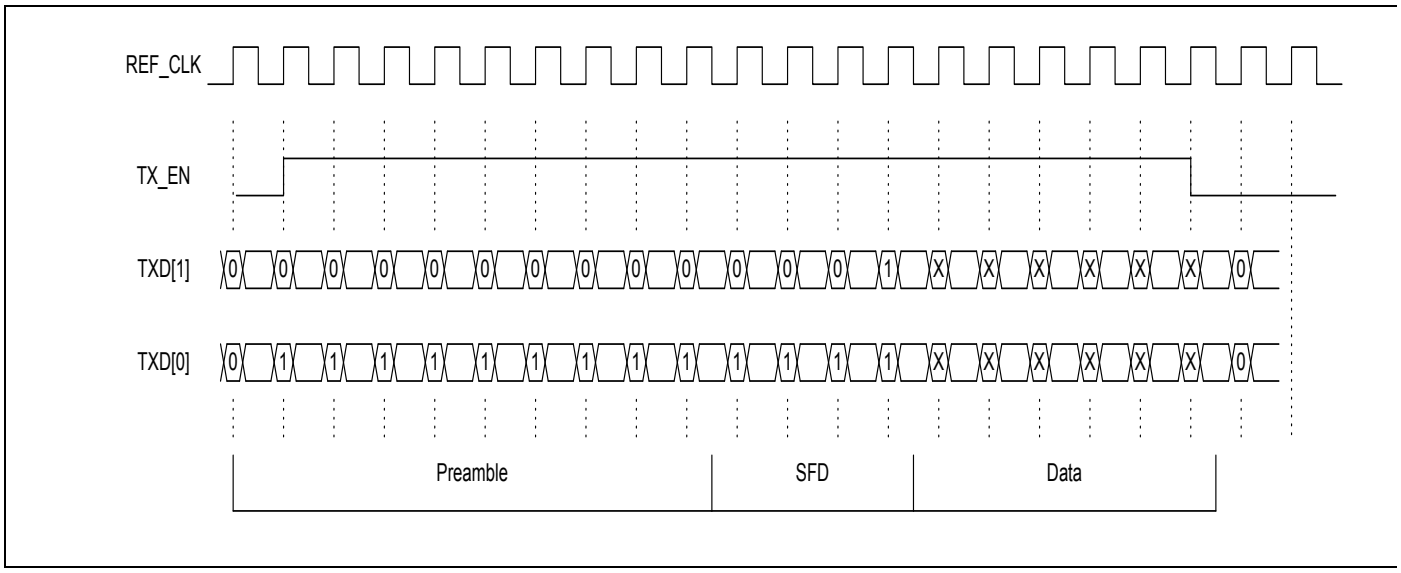


Table 46. RMII Transmit Packet Timing Parameters

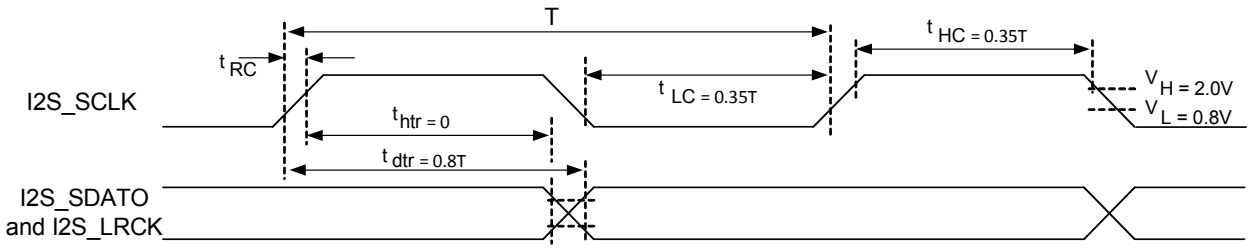
Parameter	Symbol	Minimum	Typical	Maximum	Unit
REF_CLK Cycle Time	–	–	20	–	ns
TXEN, TXER, TXD[1:0] setup time to REF_CLK rising	TXEN_SETUP	4	–	–	ns
TXEN, TXER, TXD[1:0] hold time from REF_CLK rising	TXEN_HOLD	2	–	–	ns

Notes:
1. TXD[1:0] provides valid data for each REF_CLK period while TX_EN is asserted.
2. In 10 Mbps mode, there are ten REF_CLK periods per data period.

17.6 I²S Master and Slave Mode TX Timing

Figure 25 and Table 47 provide the I²S Master mode transmitter timing.

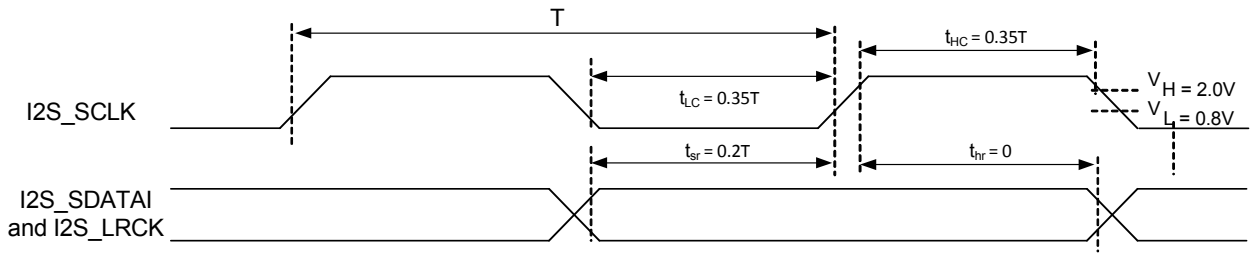
Figure 25. I²S Master Mode Transmitter Timing



T = Clock period.
T_{tr} = Minimum allowed clock period for transmitter.
T > T_{tr}.
t_{RC} is only relevant for transmitters in Slave mode.

Figure 26 and Table 47 provide the I²S Slave mode receiver timing.

Figure 26. I²S Slave Mode Receiver Timing



T = Clock period.
T_r = Minimum allowed clock period for the transmitter.
T > T_r.

Table 47. Timing for I²S Transmitters and Receivers

Parameter	Transmitter				Receiver	
	Lower Limit		Upper Limit		Lower Limit	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
Clock period T	T_{tr}	–	–	–	T_{tr}	–
Slave mode:						
Clock HIGH, t_{HC}	–	$0.35T_r$	–	–	–	$0.35T_r$
Clock LOW, t_{LC}	–	$0.35T_r$	–	–	–	$0.35T_r$
Clock rise time, t_{RC}	–	–	$0.15T_{tr}$	–	–	–
Transmitter delay, t_{dtr}	–	–	–	0.8T	–	–
Transmitter hold time, t_{htr}	0	–	–	–	–	–
Receiver setup time, t_{sr}	–	–	–	–	–	$0.2T_r$
Receiver hold time, t_{hr}	–	–	–	–	–	0

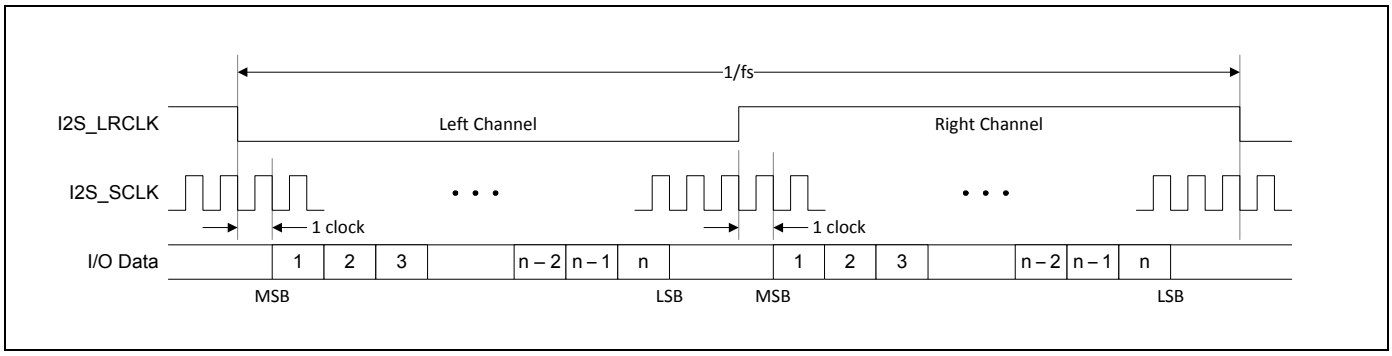
Table 48 provides the I2S_MCLK specification.

Table 48. I2S_MCLK Specification

Parameter	Minimum	Typical	Maximum	Unit
Frequency range	1	–	40	MHz
Frequency accuracy (with respect to the XTAL frequency)	–	1	–	ppb
Tuning resolution	–	50	–	ppb
Tuning range	–	1000	–	ppm
Tuning step size	–	–	10	ppm
Tuning rate	–	1	–	ppm/ms
Baseband jitter (100 Hz to 40 kHz)	–	–	100	ps rms
Wideband jitter (100 Hz to 1 MHz)	–	–	200	ps rms

Figure 27 shows the I²S frame-level timing.

Figure 27. I²S Frame-Level Timing



17.7 SDIO Interface Timing

17.7.1 SDIO Default-Speed Mode Timing

SDIO default-speed (DS) mode timing is shown by the combination of Figure 28 and Table 49.

Figure 28. SDIO Bus Timing (Default-Speed Mode)

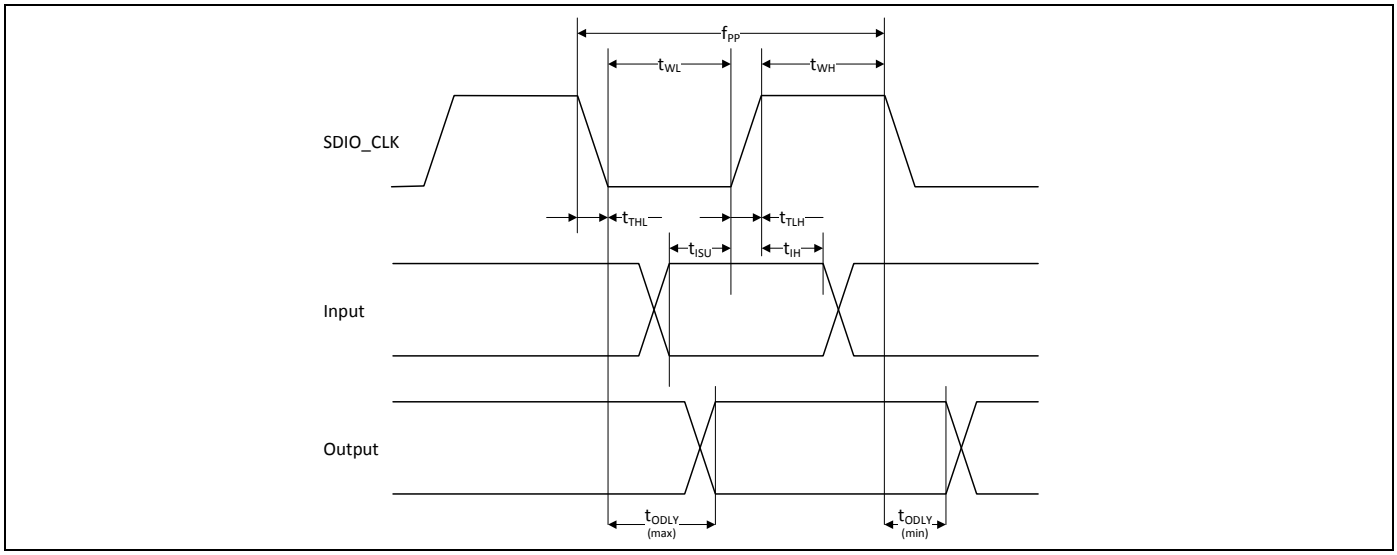


Table 49. SDIO Bus Timing[1] Parameters (Default-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO_CLK or CLK—All values are referred to minimum VIH and maximum VIL[2]					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

1. Timing is based on CL ≤ 40 pF load on CMD (command) and DAT (data) lines.

2. Min. (Vih) = 0.7 × VDDIO and max. (Vil) = 0.2 × VDDIO.

17.8 SDIO High-Speed Mode Timing

SDIO high-speed (HS) mode timing is shown by the combination of Figure 29 and Table 50.

Figure 29. SDIO Bus Timing (High-Speed Mode)

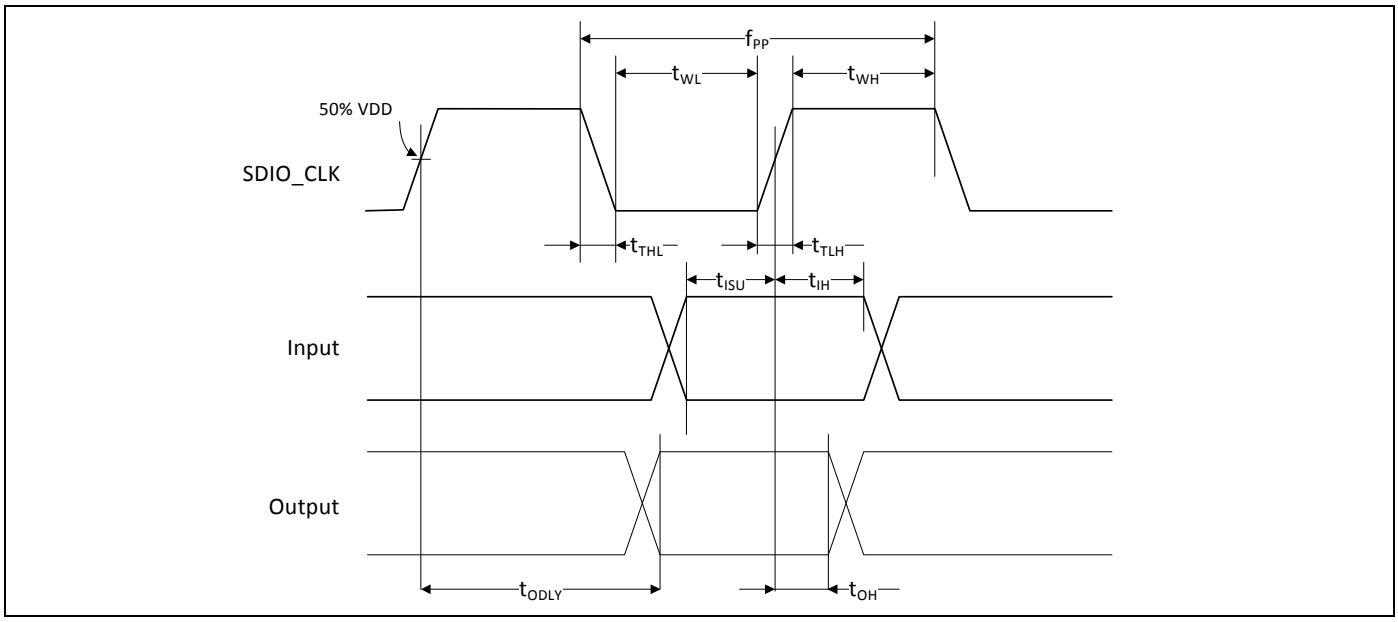


Table 50. SDIO Bus Timing[1] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO_CLK or CLK—All values are referred to minimum VIH and maximum VIL[2]					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	–	–	ns
Input hold time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

1. Timing is based on CL ≤ 40 pF load on CMD (command) and DAT (data) lines.

2. Min. (Vih) = 0.7 × VDDIO and max. (Vil) = 0.2 × VDDIO.

17.8.1 SDIO Bus Timing Specifications in SDR Modes

Clock Timing

SDIO clock timing in the SDR modes is shown by the combination of Figure 30 and Table 51.

Figure 30. SDIO Clock Timing (SDR Modes)

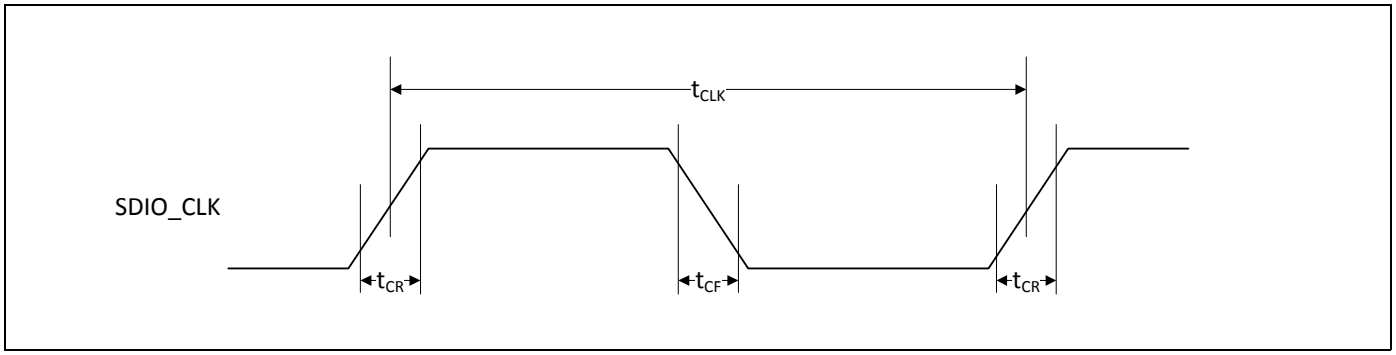


Table 51. SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

Device Input Timing

SDIO device input timing in the SDR modes is shown by the combination of Figure 31 and Table 52.

Figure 31. SDIO Bus Input Timing (SDR Modes)

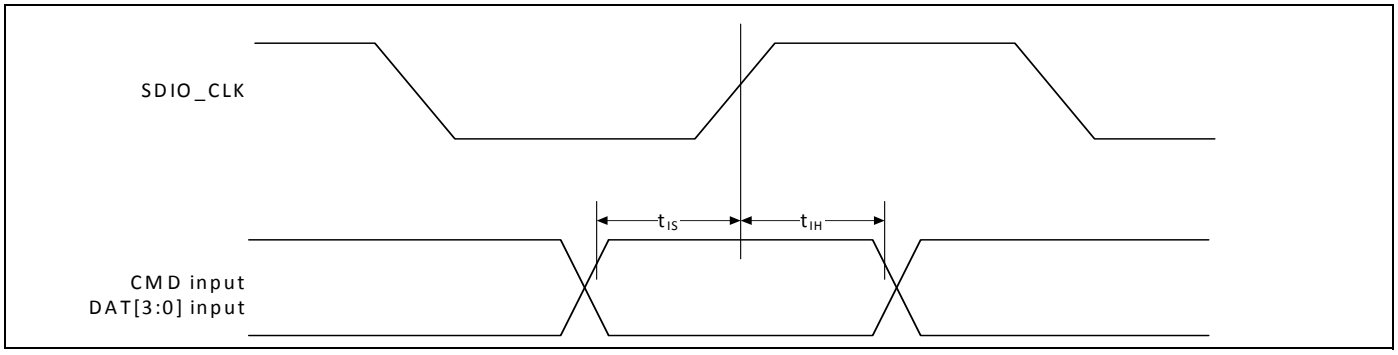


Table 52. SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Device Output Timing

SDIO device output timing in the SDR modes with clock rates up to 50 MHz is shown by the combination of Figure 32 and Table 53.

Figure 32. SDIO Bus Output Timing (SDR Modes up to 50 MHz)

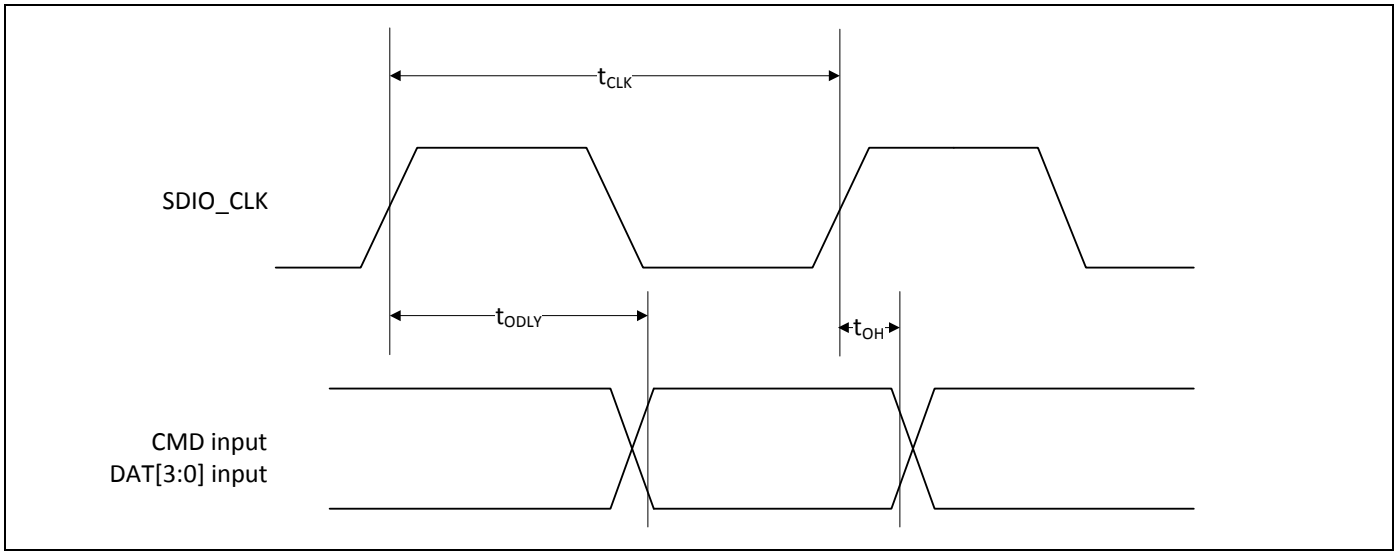


Table 53. SDIO Bus Output Timing Parameters (SDR Modes up to 50 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L= 40 pF
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min.) C_L= 15 pF

17.9 S/PDIF Interface Timing

The S/PDIF protocol embeds the clock and data within a stream of data using a Biphase Mark Code (BMC).

Figure 33 shows the S/PDIF interface timing.

Figure 33. S/PDIF Interface Timing

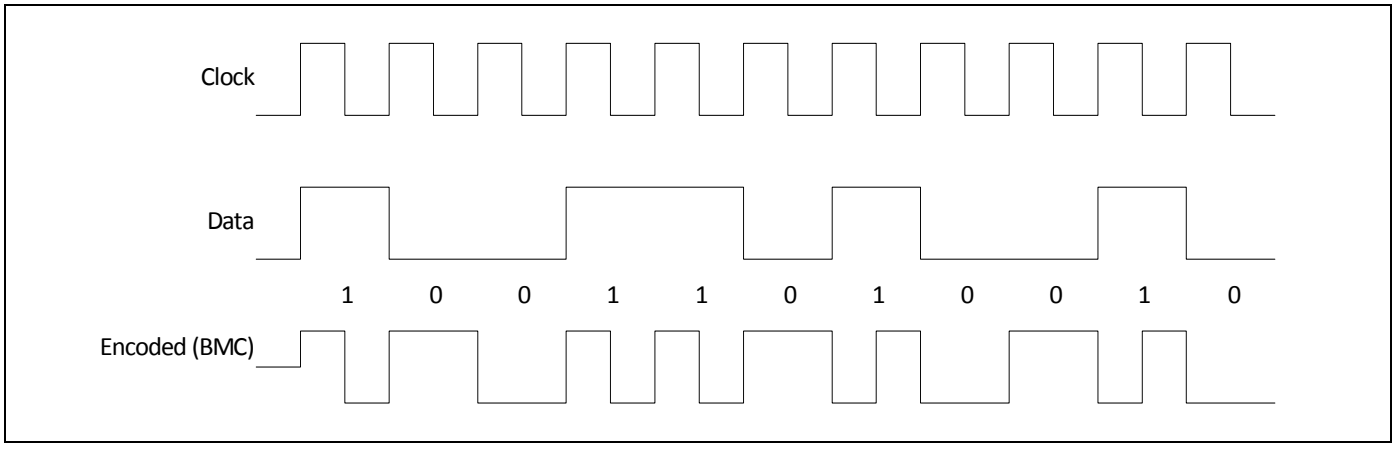


Figure 34 shows the S/PDIF data output timing.

Figure 34. S/PDIF Data Output Timing

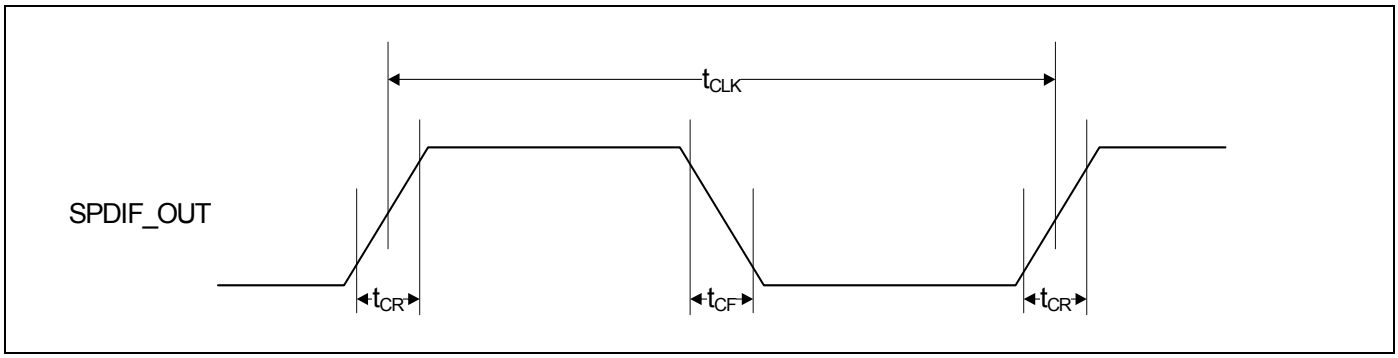


Table 54 provides the S/PDIF biphase mark code timing parameters (to be used in conjunction with Figure 34).

Table 54. SPDIF Biphase Mark Code Timing Parameters

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	192 kHz sample rate
–	t_{CR}, t_{CF}	–	0.3 × t_{CLK}	ns	–
Duty cycle	–	30	70	%	–

Table 55 provides the S/PDIF biphase mark code sample rate and receiver clock frequency.

Table 55. SPDIF Biphase Mark Code Sample Rate and Receiver Clock Frequency

Parameter	Symbol	Minimum	Maximum	Unit	Comments
Sampling frequency	f_S	–	192	kHz	192 kHz sample rate maximum.
Component clock frequency	f_{CLOCK}	–	25	MHz	Typical is 128 × f_S, max is 192 × f_S. Clock is 2× the desired data rate or 2 × 192 kHz × 64 = 24.576 MHz.

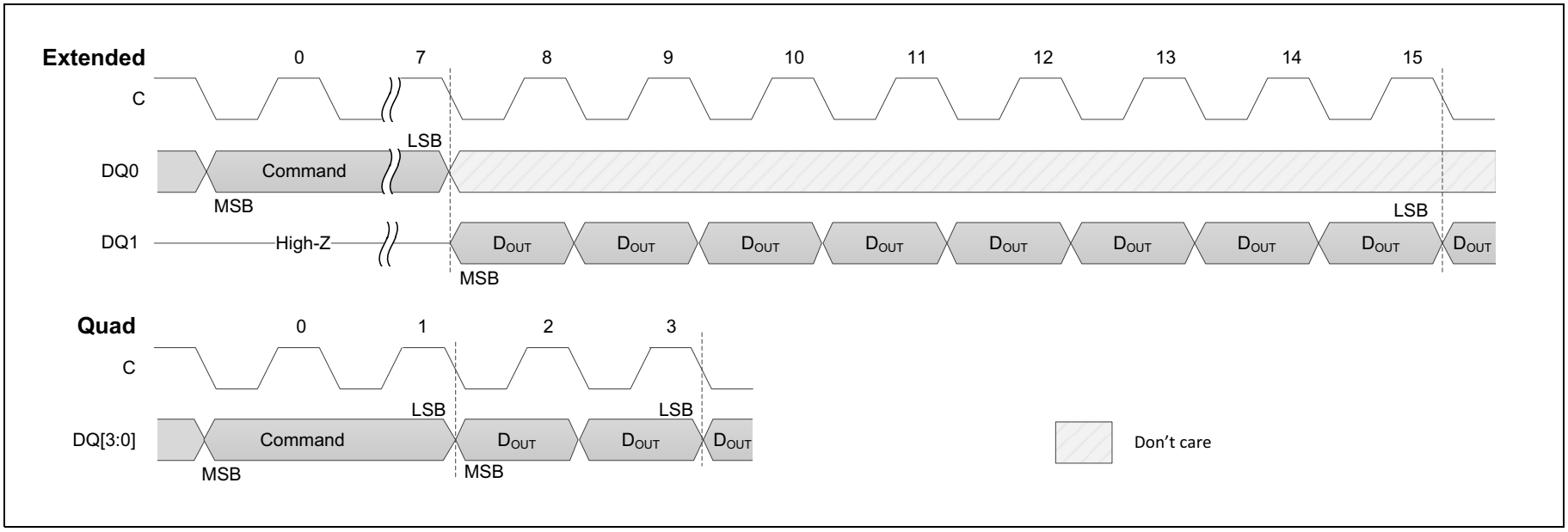
17.10 SPI Flash Timing

17.10.1 Read-Register Timing

Figure 35 shows the SPI flash extended and quad read-register timing.

Note: Regarding Figure 35: All Read Register commands except Read Lock Register are supported. A Read Nonvolatile Configuration Register operation will output data starting from the least significant byte.

Figure 35. SPI Flash Read-Register Timing



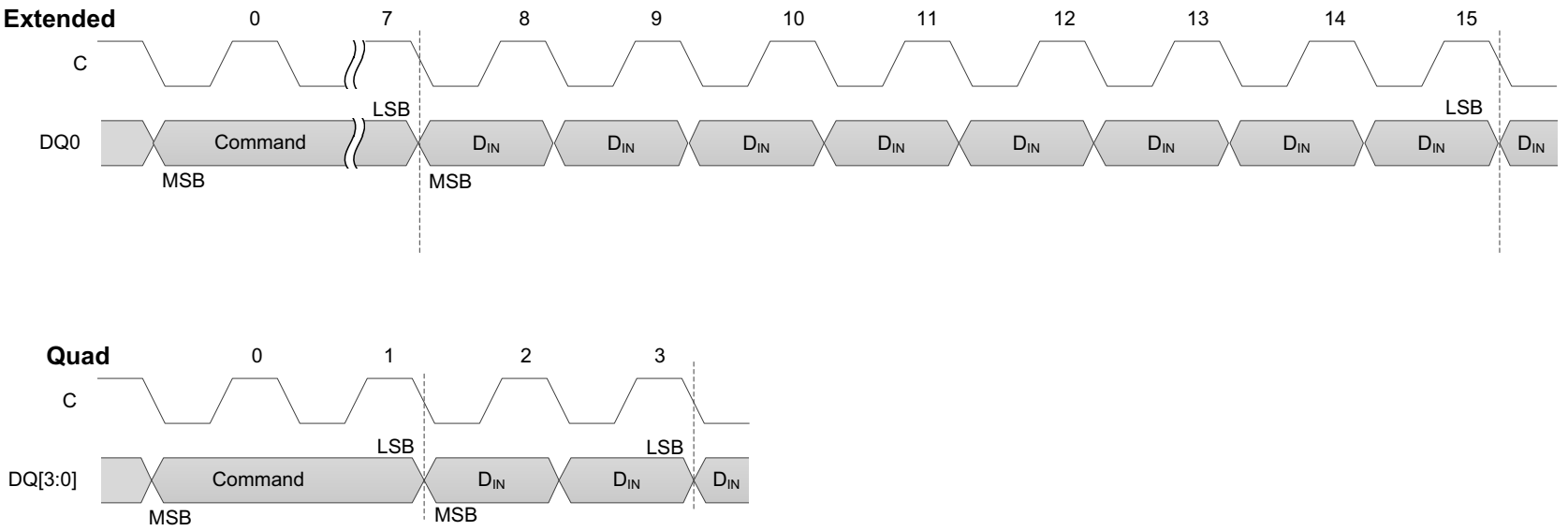
17.10.2 Write-Register Timing

Figure 36 shows the SPI flash extended and quad write-register timing.

Note: Regarding Figure 36:

1. All write-register commands except Write Lock Register are supported.
2. The waveform must be extended for each protocol: to 23 for extended and five for quad.
3. A Write Nonvolatile Configuration Register operation requires data being sent starting from the least significant byte.

Figure 36. SPI Flash Write-Register Timing



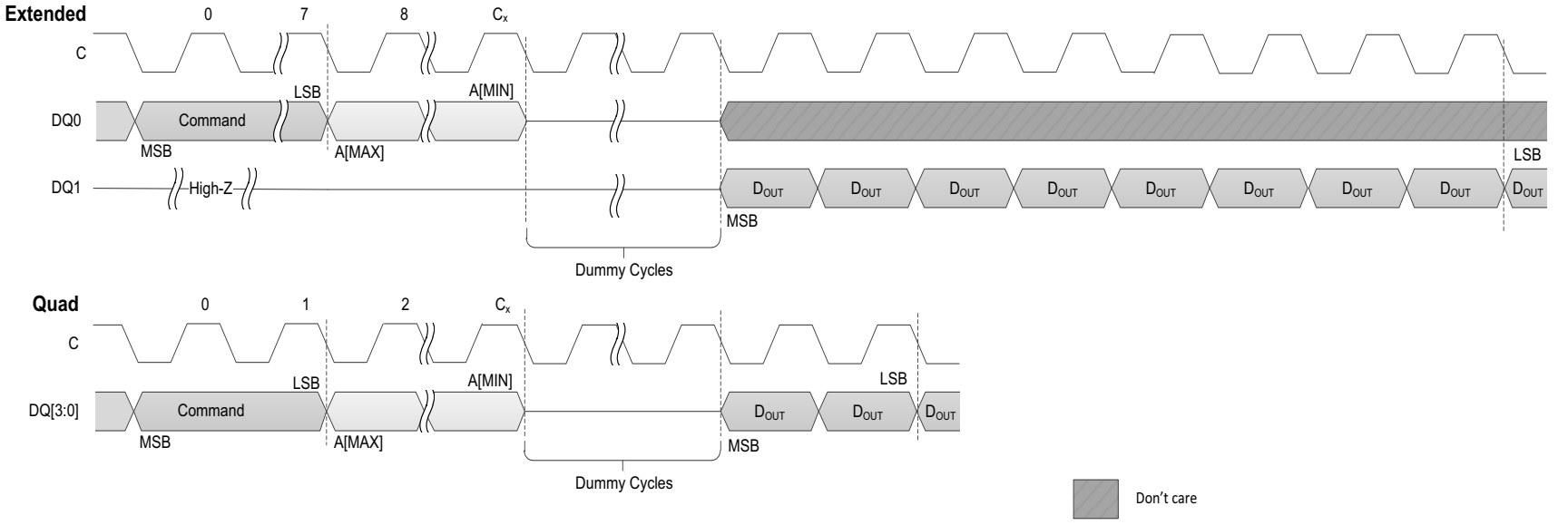
17.10.3 Memory Fast-Read Timing

Figure 37 shows the SPI flash extended and quad memory fast-read timing.

Note: Regarding Figure 37:

1. 24-bit addressing is used, so A[MAX] = A[23] and A[MIN] = A[0].
2. For an extended SPI protocol, C_x = 7 + (A[MAX] + 1).
3. For a quad SPI protocol, C_x = 1 + (A[MAX] + 1)/4.

Figure 37. Memory Fast-Read Timing



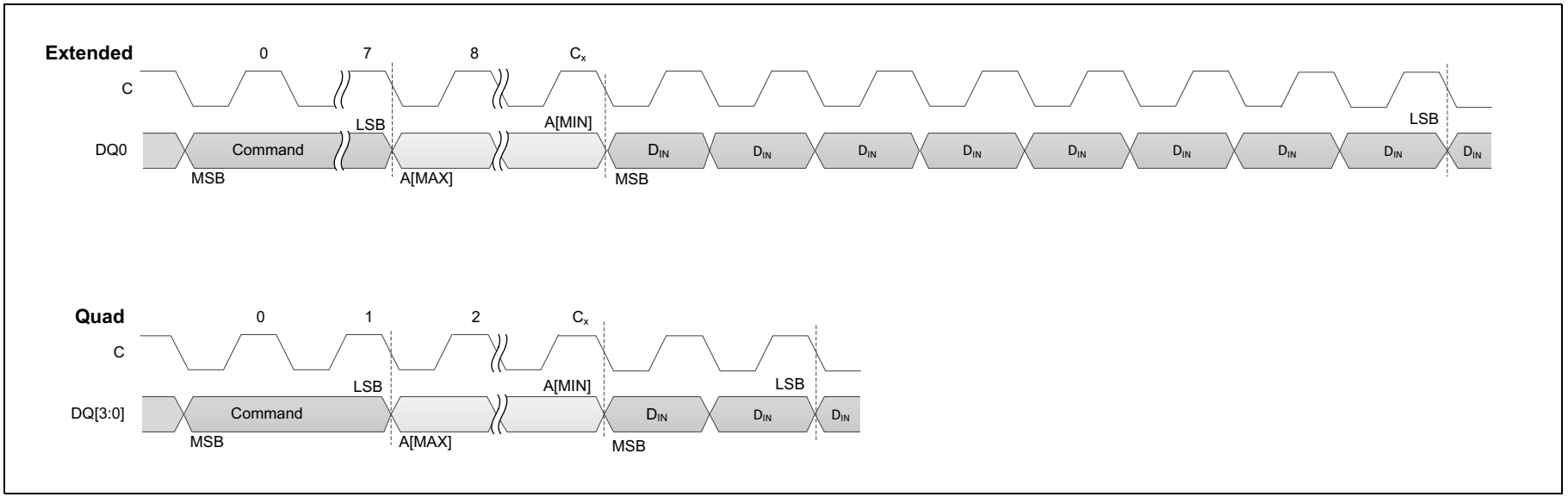
17.10.4 Memory-Write Timing

Figure 38 shows the SPI flash extended and quad memory-write (Page Program) timing.

Note: Regarding Figure 38:

1. For an extended SPI protocol, $C_x = 7 + (A[MAX] + 1)$.
2. For a quad SPI protocol, $C_x = 1 + (A[MAX] + 1)/4$.

Figure 38. Memory-Write Timing



17.10.5 SPI Flash Parameters

The combination of Figure 39 and Table 56 provide the SPI flash timing parameters.

Figure 39. SPI Flash Timing Parameters Diagram

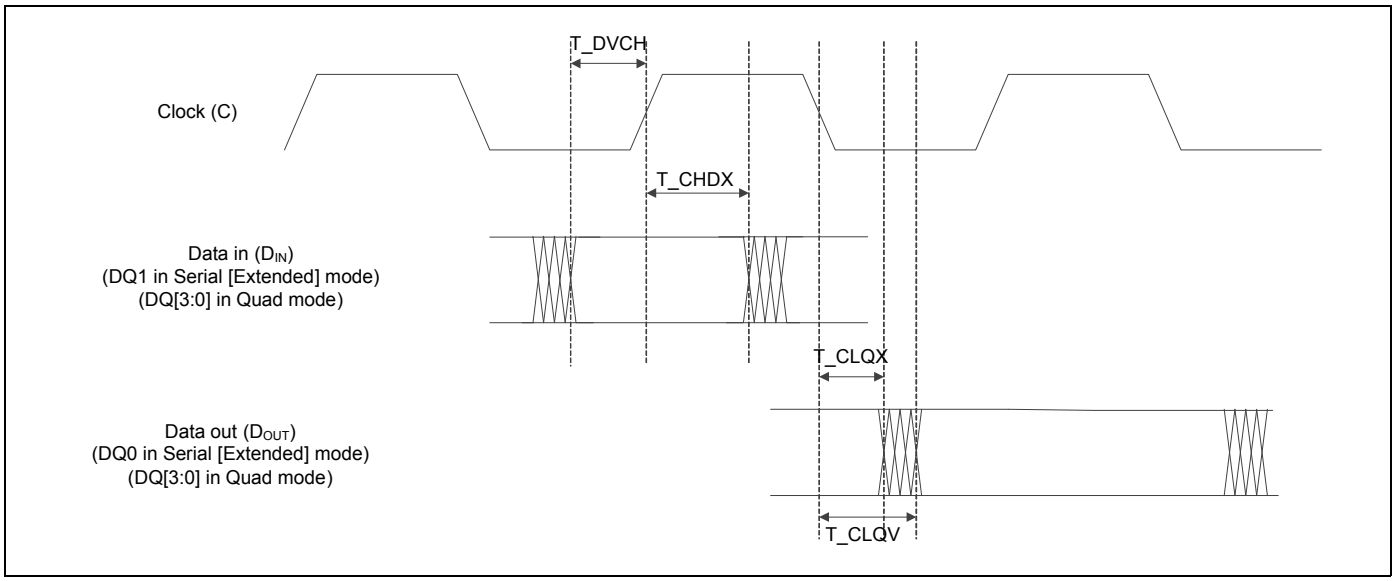


Table 56. SPI Flash Timing Parameters

Parameter	Description	Minimum	Maximum	Units
T_DVCH	Data setup time	2	–	ns
T_CHDX	Data hold time	3	–	ns
T_CLQX	Output hold time	1	–	ns
T_CLQV	Output valid time (with a 10 pF load)	–	5	ns

17.11 USB PHY and HSIC PHY Electrical Characteristics and Timing

17.11.1 USB 2.0 and USB 1.1 Electrical and Timing Parameters

Table 57 provides electrical and timing parameters for USB 2.0.

Table 57. USB 2.0 Electrical and Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units	Conditions
Baud rate	B_{PS}	–	480	–	Mbps	–
Unit interval	UI	–	2083	–	ps	–
Receiver – HS Mode						
Differential input voltage sensitivity	V_{HSDI}	300	–	–	mV	Static | $V_{IDP} - V_{IDN}$ |
Input common mode voltage range	V_{HSCM}	–50	–	500	mV	–
Receiver jitter tolerance	ΔT_{HSRX}	–0.15	–	0.15	UI	–
Input impedance	R_{IN}	40.5	45	49.5	Ω	Single ended
Transmitter – HS Mode						
Output high voltage	V_{HSOH}	360	400	440	mV	Static condition
Output low voltage	V_{HSOL}	–10	0	10	mV	Static condition
Output rise time	T_{HSR}	500	–	–	ps	10% to 90%
Output fall time	T_{HSF}	500	–	–	ps	90% to 10%
Transmitter jitter	ΔT_{HSTX}	–0.05	–	0.05	UI	Transmit output jitter
Output impedance	R_O	40.5	45	49.5	Ω	Single ended
Chirp-J output voltage (differential)	V_{CHIRPJ}	700	–	1100	mV	HS termination disabled. 1.5 kΩ ± 5% pull-up resistor connected.
Chirp-K output voltage (differential)	V_{CHIRPK}	–900	–	–500	mV	HS termination disabled. 1.5 kΩ ± 5% pull-up resistor connected.

Note: Refer to Section 7 of the USB 2.0 specification (www.usb.org) for more information on the receiver eye diagram template.

Table 58 provides electrical and timing parameters for USB 1.1.

Table 58. USB 1.1 FS/LS Electrical and Timing Parameters [1]

Parameter	Symbol	Value			Unit	Condition
		Minimum	Typical	Maximum		
Baud Rate						
FS	B_{PS}	–	12	–	Mbps	–
LS	B_{PS}	–	1.5	–	Mbps	–
Unit Interval						
FS	UI	–	83.33	–	ns	–
LS	UI	–	666.67	–	ns	–
Receiver						
Differential input sensitivity	V_{FSDI}	200	–	–	mV	Static $\|V_{IDP} – V_{IDN}\|$
Input common mode range	V_{FSCM}	0.8	–	2.5	V	–
Input impedance	Z_{IN}	300	–	–	kΩ	–
Input high voltage	V_{FSIH}	2.0	–	–	V	Static
Input low voltage	V_{FSIL}	–	–	0.8	V	Static
Transmitter						
Output high voltage	V_{FSOH}	2.8	–	–	V	Static
Output low voltage	V_{FSOL}	–	–	0.3	V	Static
Output rise/fall time for fast speed	T_R,T_F	4	–	20	ns	10 to 90%
Output rise/fall time for low speed	T_R,T_F	75	–	300	ns	10 to 90%
Fast-speed jitter	$\Delta\tau_{FSTX}$	–2	–	2	ns	–
Low-speed jitter	$\Delta\tau_{LSTX}$	–25	–	25	ns	–
Output impedance	R_O	28	–	44	Ω	Single ended

1. For more details, refer to the USB 1.1 Specification.

17.11.2 USB 2.0 Timing Diagrams

Figure 40 shows the important timing parameters associated with a post-reset transition to high-speed (HS) operation.

Figure 40. USB 2.0 Bus Reset to High-Speed Mode Operation

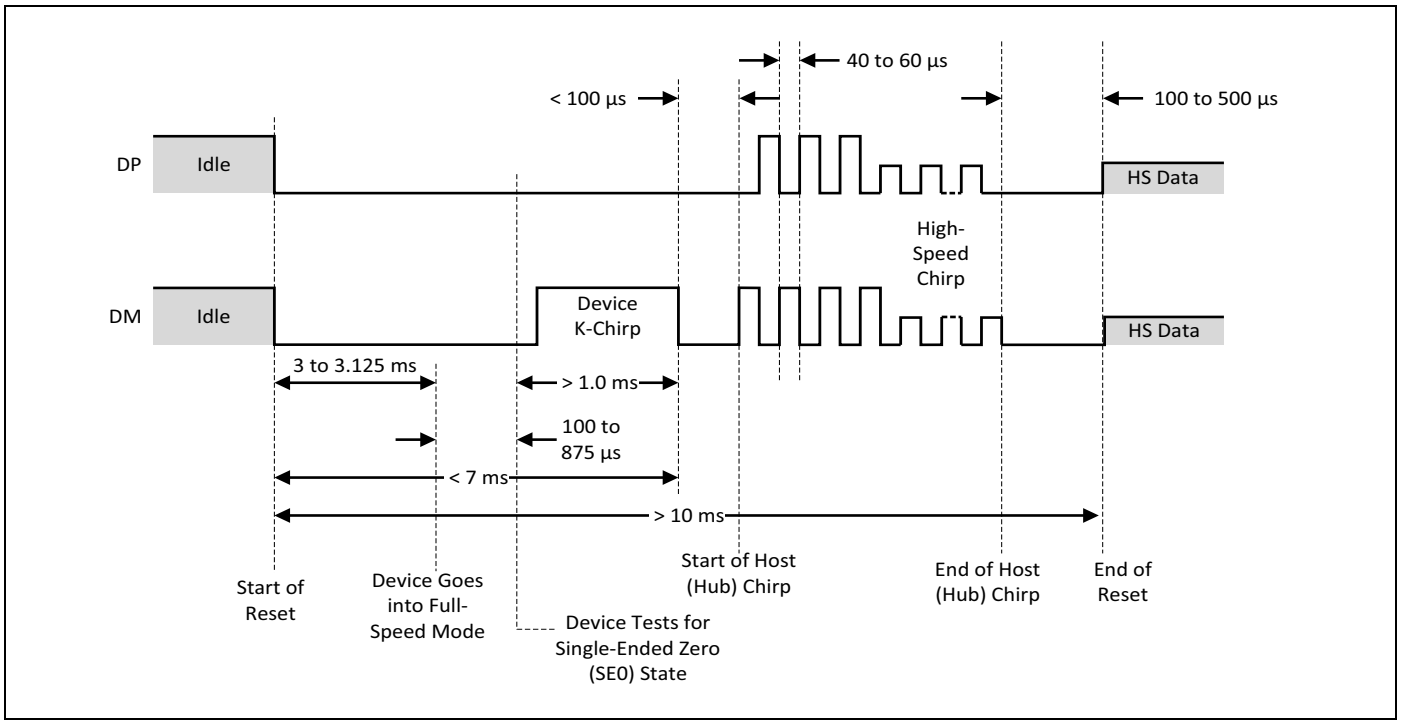


Figure 41 shows the USB 2.0 HS Mode transmit timing.

Figure 41. USB 2.0 High-Speed Mode Transmit Timing

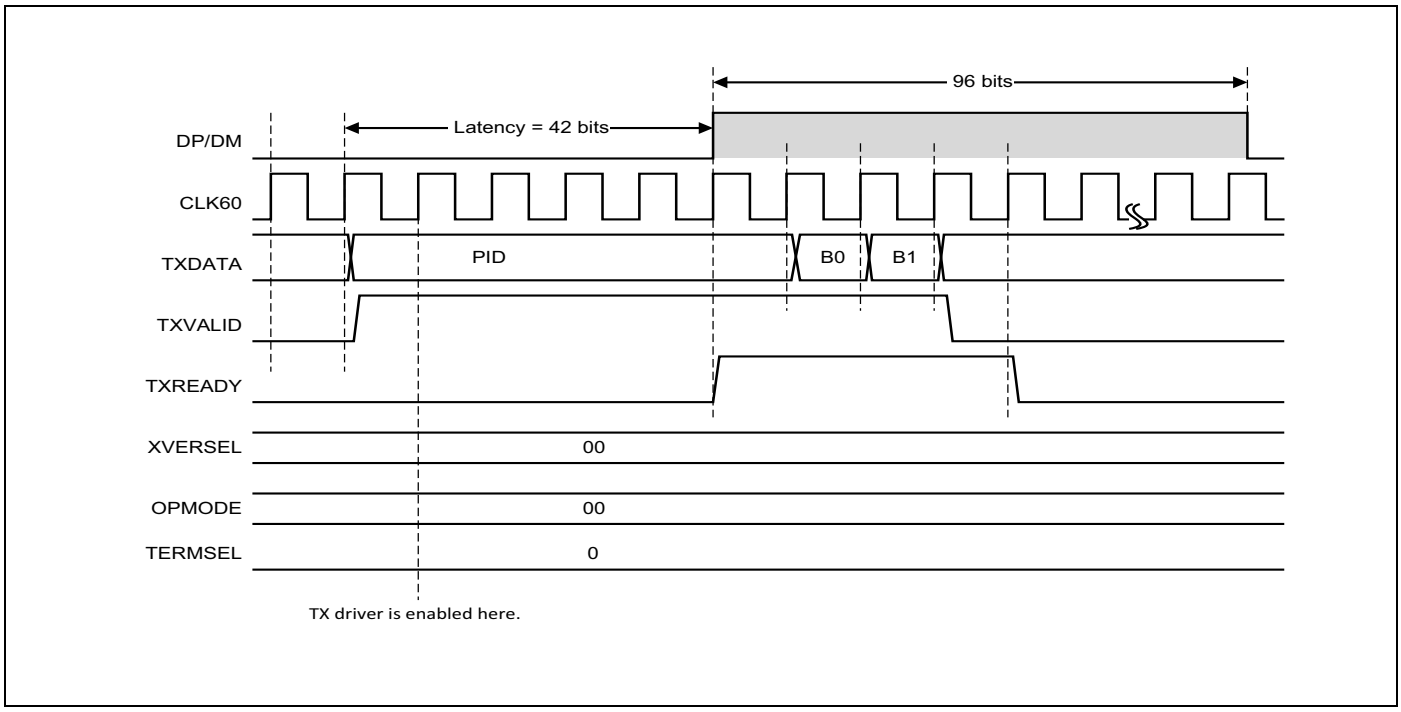
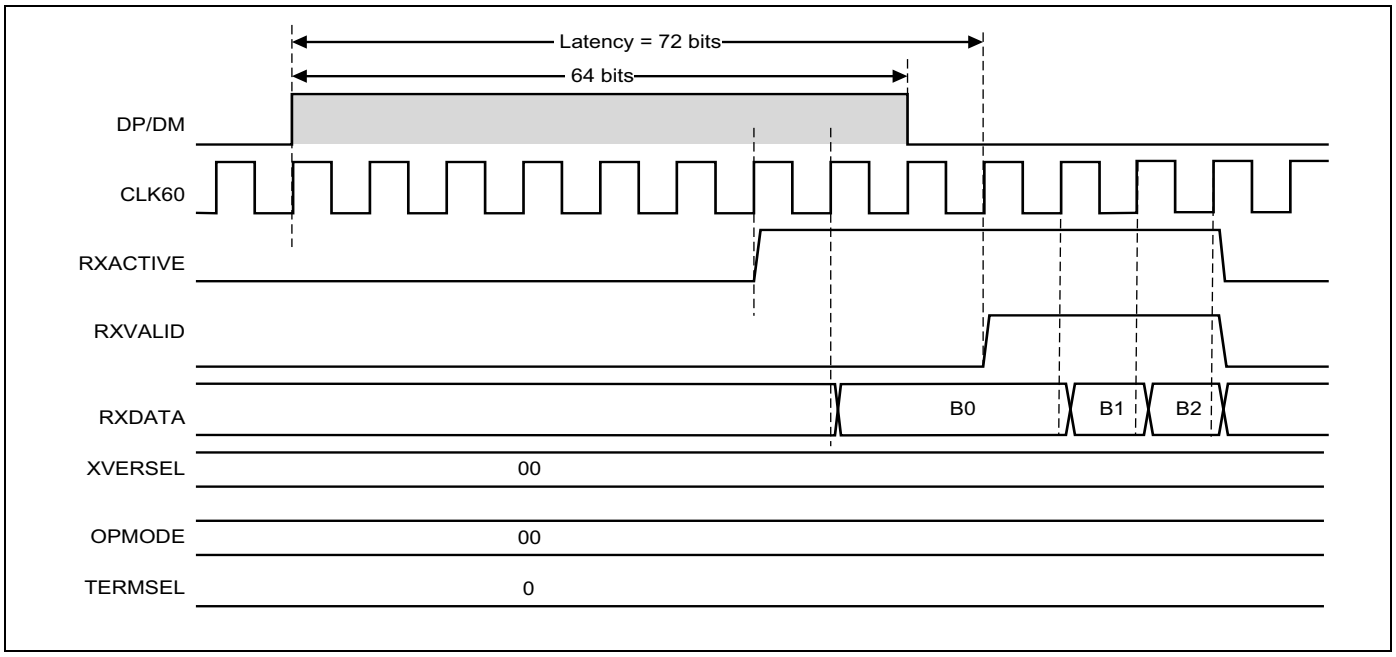


Figure 42 shows the USB 2.0 HS Mode receive timing.

Figure 42. USB 2.0 High-Speed Mode Receive Timing



17.11.3 HSIC

Table 59. HSIC Electrical and Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Comments
HSIC signaling voltage	V_{DD}	1.1	1.2	1.3	V	–
I/O voltage input low	V_{IL}	–0.3	–	0.35 × V_{DD}	V	–
I/O voltage input high	V_{IH}	0.65 × V_{DD}	–	V_{DD} + 0.3	V	–
I/O voltage output low	V_{OL}	–	–	0.25 × V_{DD}	V	–
I/O voltage output high	V_{OH}	0.75 × V_{DD}	–	–	V	–
I/O pad drive strength	O_D	40	–	60	Ω	Controlled output impedance driver
I/O weak keepers	I_L	20	–	70	mA	–
I/O input impedance	Z_I	100	–	–	kΩ	–
Total capacitive load[1]	C_L	3	–	14	pF	–
Characteristic trace impedance	T_I	45	50	55	Ω	–
Circuit board trace length	T_L	–	–	10	cm	–
Circuit board trace propagation skew[2]	T_S	–	–	15	ps	–
STROBE frequency[3]	F_{STROBE}	239.988	240	240.012	MHz	± 500 ppm
Slew rate (rise and fall) STROBE and DATA[c]	T_{slew}	0.60 × V_{DD}	1.0	1.2	V/ns	Averaged from 30% ~ 70% points
Receiver data setup time (with respect to STROBE)[c]	T_s	300	–	–	ps	Measured at the 50% point
Receiver data hold time (with respect to STROBE)[c]	T_b	300	–	–	ps	Measured at the 50% point

1. Total capacitive load (C_L), includes device Input/Output capacitance, and capacitance of a 50Ω PCB trace with a length of 10 cm.
2. Maximum propagation delay skew in STROBE or DATA with respect to each other. The trace delay should be matched between STROBE and DATA to ensure that the signal timing is within specification limits at the receiver.
3. Jitter and duty cycle are not separately specified parameters. They are incorporated into the values of this table.

18. Power-Up Sequence and Timing

18.1 Sequencing of Reset and Regulator Control Signals

The CYW43903 has two signals that allow the host to control power consumption by enabling or disabling the internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 43 and Figure 44). The timing values indicated are minimum required values; longer delays are also acceptable.

18.1.1 Description of Control Signals

- **REG_ON**: Used by the PMU to power-up the CYW43903. It controls the internal CYW43903 regulators. When this pin is high, the regulators are enabled and the device is out of reset. When this pin is low the regulators are disabled.
- **HIB_REG_ON_IN**: Used by the Hibernation (HIB) block to power up the internal CYW43903 regulators. If the HIB_REG_ON_IN pin is low, the regulators are disabled. For the HIB_REG_ON_IN pin to work as designed, HIB_REG_ON_OUT must be connected to REG_ON.

Note: The CYW43903 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold.

Note: The 10%–90% VBAT rise time should not be faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

18.1.2 Control Signal Timing Diagrams

Figure 43. REG_ON = High, No HIB_REG_ON_OUT Connection to REG_ON

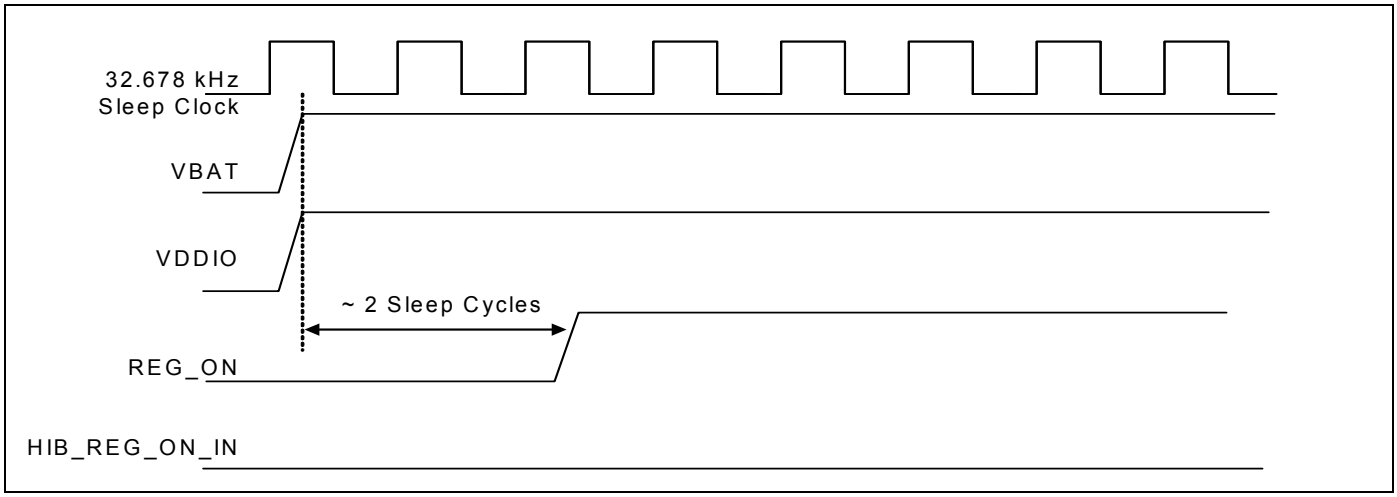
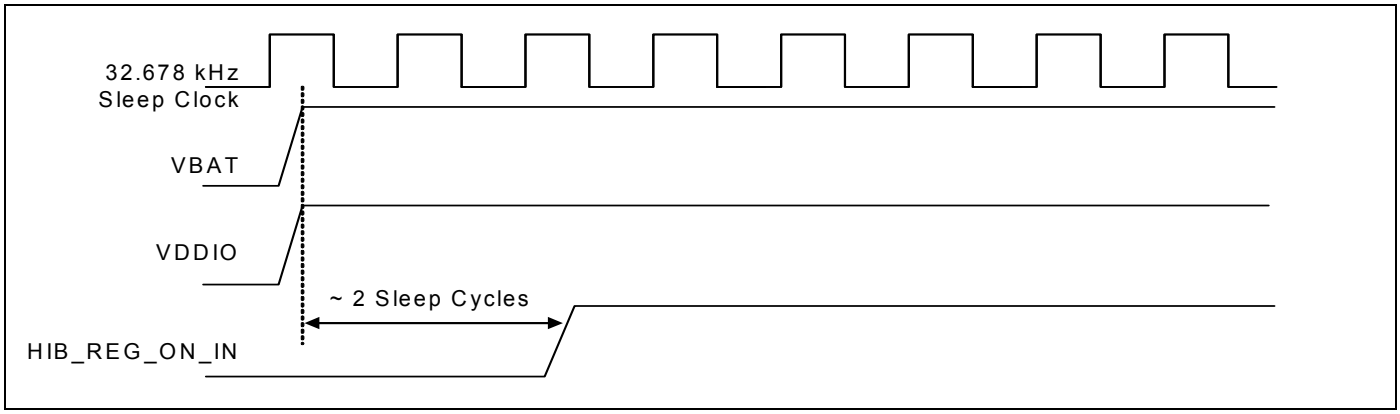


Figure 44. HIB_REG_ON_IN = High, HIB_REG_ON_OUT Connected to REG_ON



19. Thermal Information

19.1 Package Thermal Characteristics

Table 60. Package Thermal Characteristics[1]

Characteristic	FCFBGA
θ_{JA} (°C/W) (value in still air)	43.25
θ_{JB} (°C/W)	16.32
θ_{JC} (°C/W)	16.12
Ψ_{JT} (°C/W)	9.78
Ψ_{JB} (°C/W)	26.95
Maximum Junction Temperature T_j (°C)	129.9
Maximum power dissipation (W)	1.38

1. No heat sink, TA = 70°C. This is an estimate based on a 4-layer PCB that conforms to EIA/JESD51–7. Air velocity is 0 m/s.

19.2 Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

TJ = TT + P x YJT

Where:

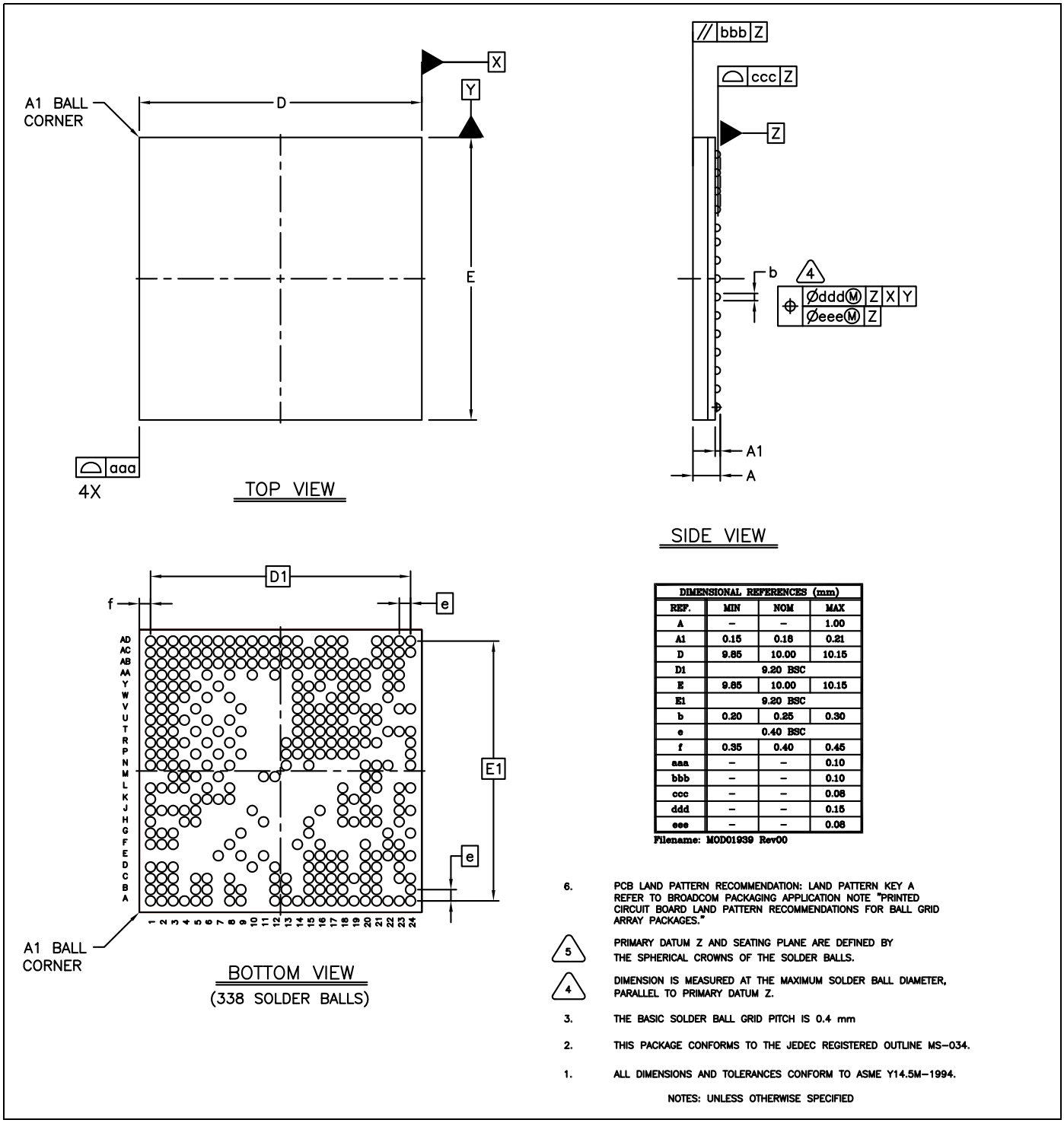
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

19.3 Environmental Characteristics

For environmental characteristics data, see Table 18, “Environmental Ratings,”.

20. Mechanical Information

Figure 45. FCFBGA Package



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.00
A1	0.15	0.18	0.21
D	9.85	10.00	10.15
D1		9.20 BSC	
E	9.85	10.00	10.15
E1		9.20 BSC	
b	0.20	0.25	0.30
e		0.40 BSC	
f	0.35	0.40	0.45
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD01939 Rev00

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.4 mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MS–034.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

21. Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
CYW43903KRFBG	10 mm x 10 mm, 338-pin FCFBGA (RoHs compliant)	–	–30°C to +85°C

22. Additional Information

22.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

22.2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (https://community.cypress.com/)

Document History Page

Document Title: CYW43903 WICED™ IEEE 802.11 a/b/g/n SoC with an Embedded Applications Processor Document Number: 002-14826				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	10/15/2015	43903-DS100-R Initial Release
*A	–	–	11/03/2015	43903-DS101-R Updated: • Table 21: “Absolute Maximum Ratings” • Table 24: “Recommended Operating Conditions and DC Characteristics” • Table 30: “WLAN 2.4 GHz Receiver Performance Specifications” • Table 31: “WLAN 2.4 GHz Transmitter Performance Specifications”
*B	–	–	03/12/2016	43903-DS102-R Updated: • General edits
*C	5445059	UTSV	11/14/2016	Added Cypress Part Numbering Scheme and Mapping Table. Updated to Cypress template.

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