

## Features

- Pin- and function-compatible with CY7C1049B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 90 \text{ mA}$  at 10 ns
- Low CMOS Standby power
  - $I_{SB2} = 10 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 36-pin (400-Mil) Molded SOJ package

## Functional Description

The CY7C1049D <sup>[1]</sup> is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is

provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

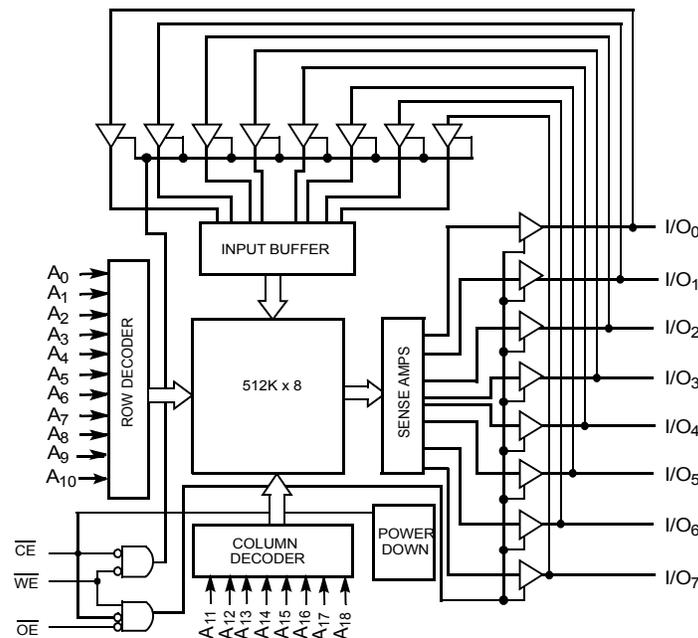
The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1049D is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

The CY7C1049D is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

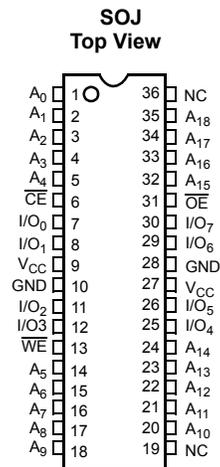
1. For guidelines on SRAM system design, refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

## Contents

<b>Pin Configuration</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>11</b>
<b>Selection Guide</b> .....	<b>3</b>	Ordering Code Definitions .....	11
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagram</b> .....	<b>12</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>13</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>13</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	13
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>14</b>
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>15</b>
<b>Data Retention Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	15
<b>Data Retention Waveform</b> .....	<b>6</b>	Products .....	15
<b>Switching Characteristics</b> .....	<b>7</b>	PSoC® Solutions .....	15
<b>Switching Waveforms</b> .....	<b>8</b>	Cypress Developer Community .....	15
<b>Truth Table</b> .....	<b>11</b>	Technical Support .....	15

## Pin Configuration

Figure 1. 36-pin SOJ pinout (Top View)



## Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	90	mA
Maximum CMOS standby current	10	mA

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage on V <sub>CC</sub> to Relative GND [2] .....	-0.5 V to +6.0 V
DC Voltage Applied to Outputs in High Z State [2] .....	-0.5 V to V <sub>CC</sub> + 0.5 V

DC Input Voltage [2] .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015) .....	>2001 V
Latch-Up Current .....	>200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	4.5 V–5.5 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit	
			Min	Max		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	V	
		V <sub>CC</sub> = Max, I <sub>OH</sub> = -0.1mA	-	3.4 [3]		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA	-	0.4	V	
V <sub>IH</sub> [2]	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.5	V	
V <sub>IL</sub> [2]	Input LOW Voltage [2]		-0.5	0.8	V	
I <sub>IX</sub>	Input Leakage Current	GND < V <sub>I</sub> < V <sub>CC</sub>	-1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND < V <sub>OUT</sub> < V <sub>CC</sub> , Output Disabled	-1	+1	μA	
I <sub>CC</sub>	VCC Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	100 MHz	-	90	mA
			83 MHz	-	80	mA
			66 MHz	-	70	mA
			40 MHz	-	60	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current – TTL Inputs	Max. V <sub>CC</sub> , CE > V <sub>IH</sub> , V <sub>IN</sub> > V <sub>IH</sub> or V <sub>IN</sub> < V <sub>IL</sub> , f = f <sub>MAX</sub>	-	20	mA	
I <sub>SB2</sub>	Automatic CE Power-Down Current – CMOS Inputs	Max. V <sub>CC</sub> , CE > V <sub>CC</sub> - 0.3 V, V <sub>IN</sub> > V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> < 0.3 V, f = 0	-	10	mA	

### Notes

- Minimum voltage is -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
- Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V<sub>IH</sub> of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

### Capacitance

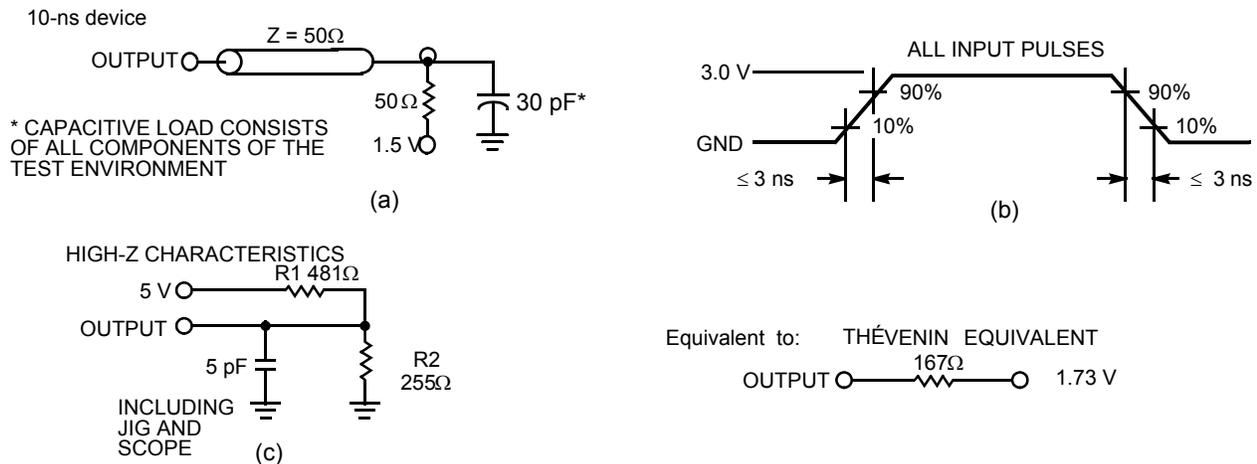
Parameter <sup>[4]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	8	pF
C <sub>OUT</sub>	I/O capacitance		8	pF

### Thermal Resistance

Parameter <sup>[4]</sup>	Description	Test Conditions	SOJ Package	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.91	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		36.73	°C/W

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[5]</sup>



**Note**

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

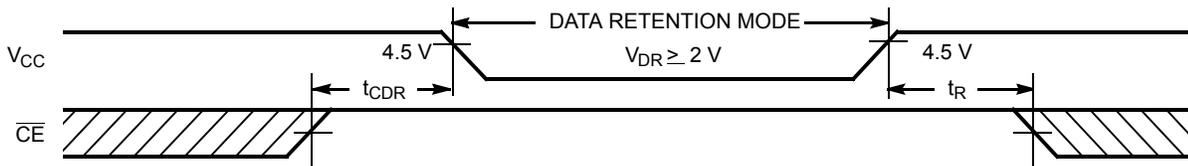
### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions <sup>[6]</sup>	Min	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0	–	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> = 2.0 V,	–	10	mA
t <sub>CDR</sub> <sup>[7]</sup>	Chip Deselect to Data Retention Time	$\overline{CE} \geq V_{CC} - 0.3 V,$	0	–	ns
t <sub>R</sub> <sup>[8]</sup>	Operation Recovery Time	V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.3 V or V <sub>IN</sub> ≤ 0.3 V	t <sub>RC</sub>	–	ns

### Data Retention Waveform

Figure 3. Data Retention Waveform



**Notes**

- 6. No input may exceed V<sub>CC</sub> + 0.5 V.
- 7. Tested initially and after any design or process changes that may affect these parameters.
- 8. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 50 μs or stable at V<sub>CC(min.)</sub> ≥ 50 μs.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[9]</sup>	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}$	$V_{CC}$ (typical) to the First Access <sup>[10]</sup>	100	–	$\mu$ s
$t_{RC}$	Read Cycle Time	10	–	ns
$t_{AA}$	Address to Data Valid	–	10	ns
$t_{OHA}$	Data Hold from Address Change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[11]</sup>	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[11, 12]</sup>	–	5	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[11]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[11, 12]</sup>	–	5	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down	–	10	ns
<b>Write Cycle <sup>[13, 14]</sup></b>				
$t_{WC}$	Write Cycle Time	10	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	7	–	ns
$t_{AW}$	Address Set-Up to Write End	7	–	ns
$t_{HA}$	Address Hold from Write End	0	–	ns
$t_{SA}$	Address Set-Up to Write Start	0	–	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7	–	ns
$t_{SD}$	Data Set-Up to Write End	6	–	ns
$t_{HD}$	Data Hold from Write End	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[11]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[11, 12]</sup>	–	5	ns

### Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
10.  $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
11. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (c) of [Figure 2](#). Transition is measured when the outputs enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
14. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 4. Read Cycle No. 1 [15, 16]

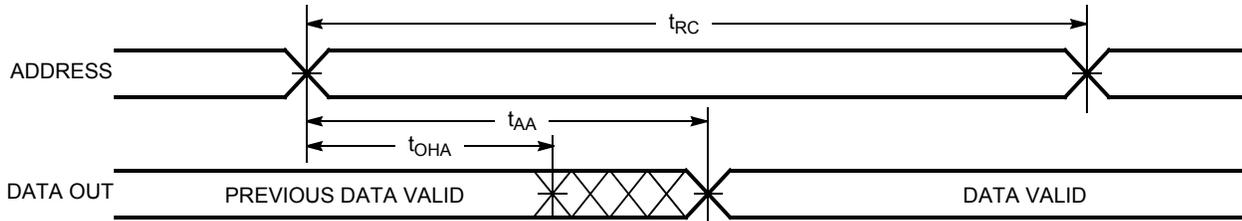
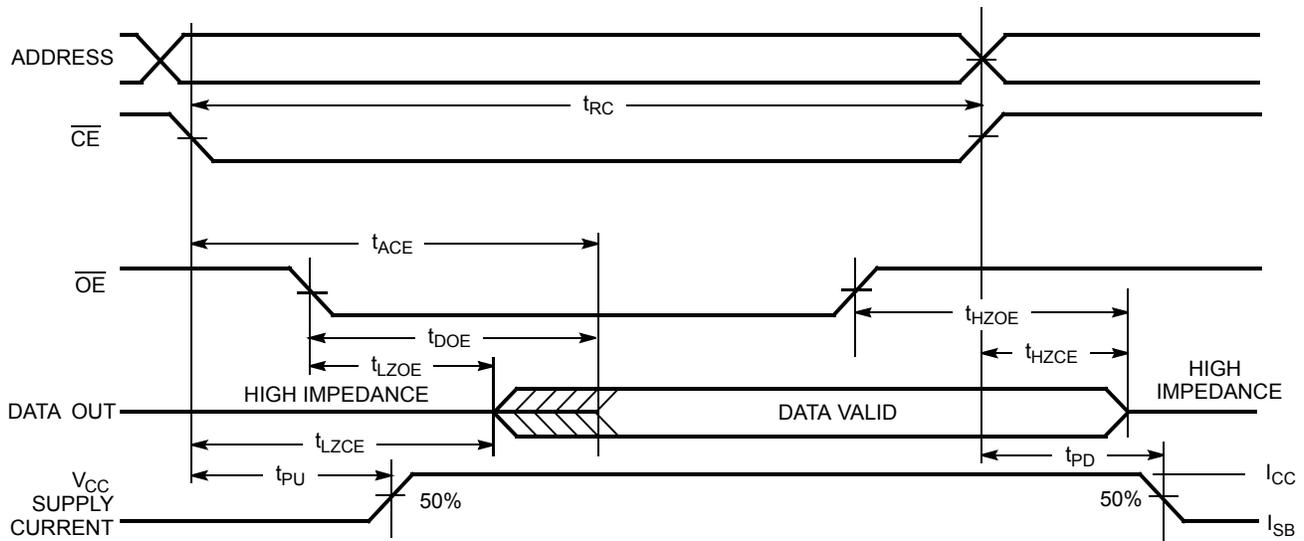


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [16, 17]



**Notes**

15. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .

16.  $\overline{WE}$  is HIGH for read cycle.

17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [18, 19]

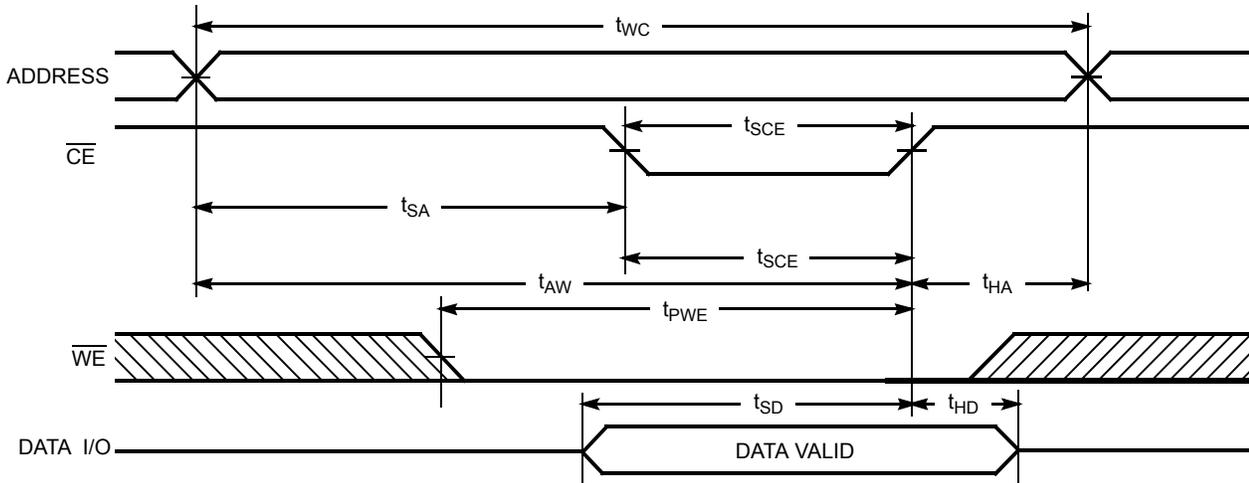
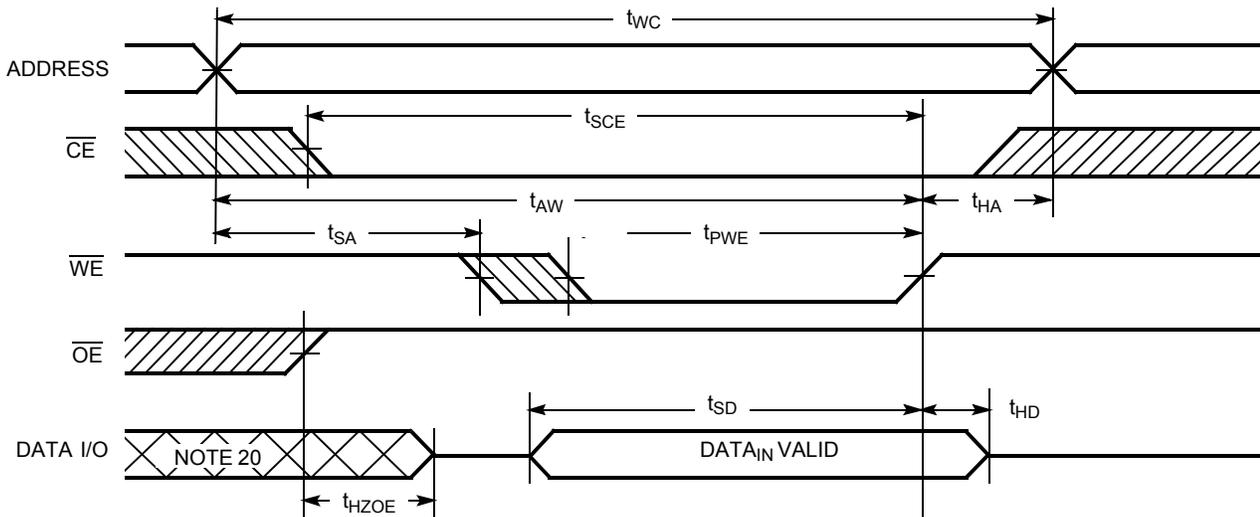


Figure 7. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write) [18, 19]

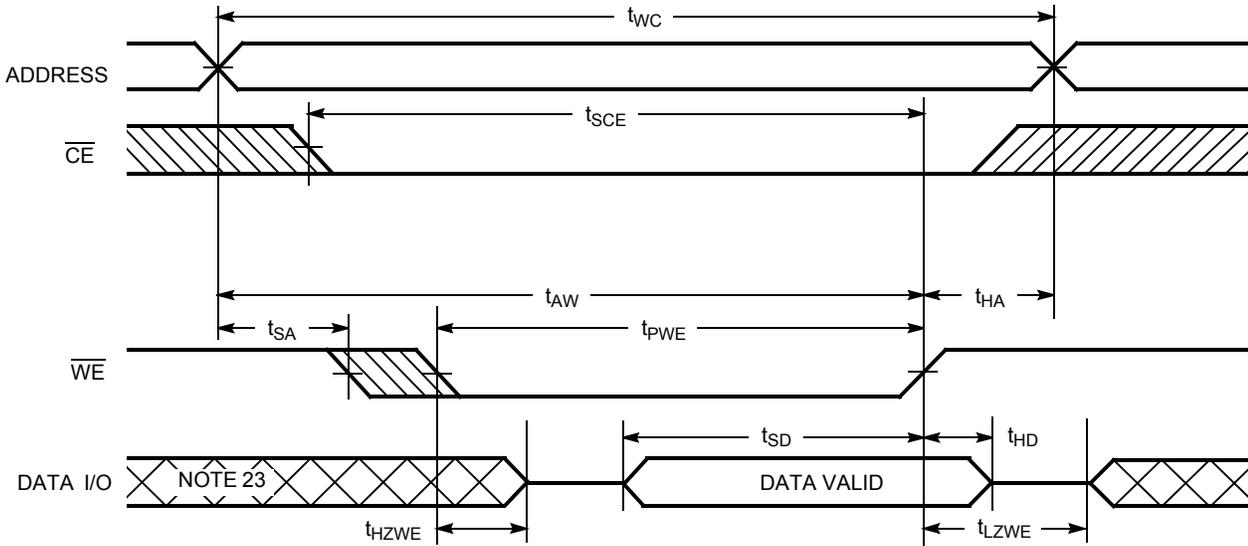


Notes

- 18. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
- 19. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
- 20. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms(continued)

Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [21, 22]



Note

- 21. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 22. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 23. During this period the I/Os are in the output state and input signals should not be applied.

### Truth Table

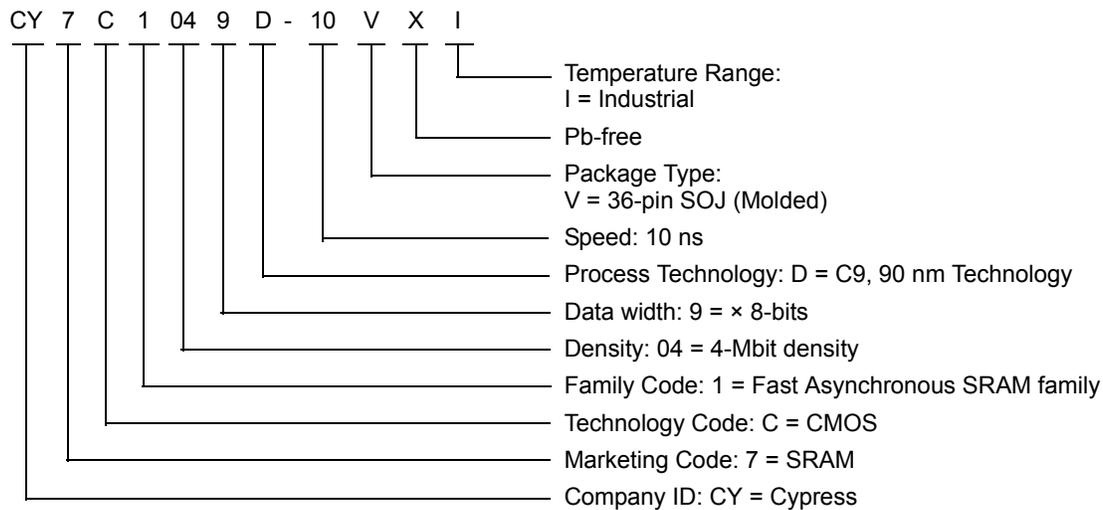
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1049D-10VXI	51-85090	36-pin SOJ (Molded) Pb-free	Industrial

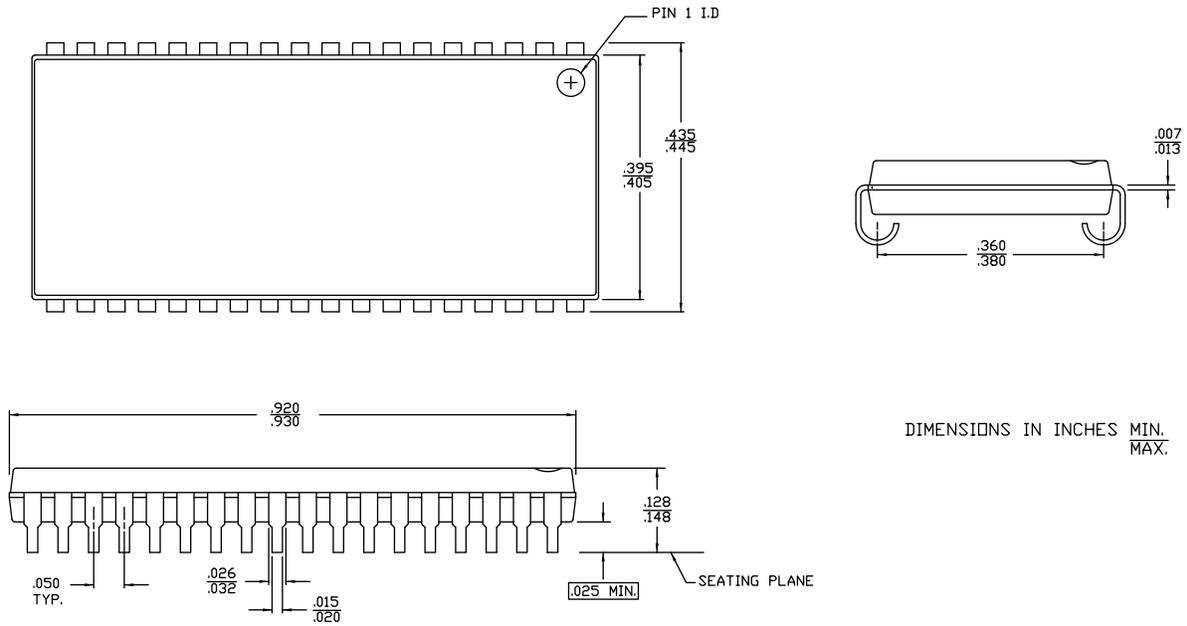
Please contact your local Cypress sales representative for availability of these parts.

### Ordering Code Definitions



Package Diagram

Figure 9. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090



51-85090 \*F

## Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
SOJ	Small Outline J-Lead
VFBGA	Very Fine-Pitch Ball Grid Array

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}C$	degree Celsius
MHz	megahertz
$\mu A$	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY7C1049D, 4-Mbit (512 K × 8) Static RAM Document Number: 38-05474				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance Datasheet for C9 IPP
*A	233729	RKF	See ECN	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	351096	PCI	See ECN	Changed from Advance to Preliminary Removed 17, 20 ns Speed bin Added footnote # 4 Redefined I <sub>CC</sub> values for Com'l and Ind'l temperature ranges I <sub>CC</sub> (Com'l): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively I <sub>CC</sub> (Ind'l): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Added V <sub>IH(max)</sub> spec in Note# 2 Modified Note# 10 on t <sub>R</sub> Changed t <sub>SCE</sub> from 8 to 7 ns for 10 ns speed bin Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Truth Table on page# 6 Removed L-Version Added 10 ns parts in the Ordering Information Table Added Lead-Free Product Information Shaded Ordering Information Table
*C	446328	NXR	See ECN	Converted from Preliminary to Final Removed -12 and -15 speed bins Removed Commercial Operating Range product information Changed Maximum Rating for supply voltage from 7 V to 6 V Updated Thermal Resistance table Changed t <sub>HZWE</sub> from 6 ns to 5 ns Updated footnote #7 on High-Z parameter measurement Replaced Package Name column with Package Diagram in the Ordering Information table
*D	3109184	AJU	12/13/2010	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> .
*E	3235742	PRAS	04/20/2011	Added Acronyms and Units of measure. Updated template.
*F	4040855	MEMJ	06/26/2013	Updated <a href="#">Functional Description</a> . Updated <a href="#">Electrical Characteristics</a> : Added one more Test Condition "V <sub>CC</sub> = Max, I <sub>OH</sub> = -0.1mA" for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition. Added Note 3 and referred the same note in maximum value for V <sub>OH</sub> parameter corresponding to Test Condition "V <sub>CC</sub> = Max, I <sub>OH</sub> = -0.1mA". Updated <a href="#">Package Diagram</a> : spec 51-85090 – Changed revision from *E to *F. Updated in new template.
*G	4391976	MEMJ	05/28/2014	Updated <a href="#">Switching Waveforms</a> : Added Note 22 and referred the same note in <a href="#">Figure 8</a> . Completing Sunset Review.
*H	4578500	MEMJ	11/24/2014	Added related documentation hyperlink in page 1.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

<a href="#">Automotive</a>	<a href="#">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="#">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="#">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="#">cypress.com/go/powerpsoc</a> <a href="#">cypress.com/go/plc</a>
<a href="#">Memory</a>	<a href="#">cypress.com/go/memory</a>
<a href="#">PSoC</a>	<a href="#">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="#">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="#">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="#">cypress.com/go/wireless</a>

#### PSoC<sup>®</sup> Solutions

[psoc.cypress.com/solutions](#)  
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/go/support](#)

---

© Cypress Semiconductor Corporation, 2004-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.