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EFM32TG232 Errata History

F32/F16/F8

This document describes known errata for all revisions of EFM32TG232 devices.

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

1 Errata History

1.1 Errata Overview

Table 1.1 (p. 2) shows which erratum is applicable for each revision. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to all revisions of this device.

Table 1.1. Errata Overview

Erratum ID	Rev. C	Rev. B	Rev. A
AES_E101	X	X	X
AES_E102	X	X	X
CMU_E108		X	X
CMU_E109		X	X
DMA_E101	X	X	X
EMU_E105		X	X
GPIO_E101		X	X
LES_E101		X	X
LES_E102		X	X
LES_E103		X	X
PRS_E101	X	X	X
TIMER_E102	X	X	X
USART_E112	X	X	X
WDOG_E103	X	X	X

1.2 EFM32TG232 Errata Descriptions

Table 1.2. EFM32TG232 Errata Descriptions

ID	Title/Problem	Effect	Fix/Workaround
AES_E101	**BYTEORDER does not work in combination with DATASTART/XORSTART** When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XORSTART.	If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order.	Do not use BYTEORDER in combination with DATASTART or XORSTART.
AES_E102	**AES_STATUS_RUNNING set one cycle late with BYTEORDER set** When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late.	If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption.	If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag.
CMU_E108	**LFxCLKEN write** First write to LFxCLKEN can be missed.	For devices with PROD_REV < 15, enabling the clock for LFA/LFB after reset and then immediately writing LFACLKEN/LFBCLKEN, may cause the write to miss its effect.	For devices with PROD_REV < 15, make sure CMU_SYNCBUSY is not set before writing LFACLKEN/LFBCLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy.
CMU_E109	**LFXO configuration incorrect** LFXO configuration incorrect.	For devices with PROD_REV < 15, the default value for LFXOBOOST in CMU_CTRL are wrong.	On devices with PROD_REV < 15, change LFXOBOOST to 0.
DMA_E101	**EM2 with WFE and DMA** WFE does not work for the DMA in EM2.	In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system.	Use WFI (Wait for Interrupt) or EM1 instead.
EMU_E105	**Debug unavailable during DMA processing from EM2** The debugger cannot access the system processing DMA request from EM2.	DMA requests from the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the DMA controller, the system will keep waiting for it while denying debug access.	Make sure DMA requests triggered from EM2 are handled.
GPIO_E101	**GPIO wakeup from EM4**	All EM4 wakeup cause bits for EM4 wakeup pins with high polarity are set on wakeup.	Use low polarity if possible. For active high, slow changing inputs, a solution is to sample the inputs on wakeup.

ID	Title/Problem	Effect	Fix/Workaround
	On GPIO wakeup from EM4 all cause bits for high-polarity wakeup pins are set.		
LES_E101	**LESENSE and Schmitt trigger** Schmitt trigger cannot be disabled on pins used for sensor excitation	When using LESENSE to excite a pin, the pin has to be configured in push-pull mode, which also enables the Schmitt trigger. If this pin has an input voltage somewhere in between 0.3*VDD and 0.7*VDD, the Schmitt trigger will consume a considerable ammount of current.	Keep the input voltage to pins configured as push-pull outside the range 0.3*VDD to 0.7*VDD when LESENSE is not interacting with the connected sensor.
LES_E102	**LESENSE and DAC CH1 configuration** LESENSE cannot control DAC CH1 if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.	LESENSE control of DAC CH1 cannot be enabled if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.	Configure DACCH0CONV in LESENSE_PERCTRL to anything but DISABLE, this enables DAC CH1 to be controlled properly. If DAC CH0 is not to be used, set DACCH0OUT in LESENSE_PERCTRL to DISABLE. This will disable LESENSE control of DAC CH0, but still allow LESENSE to control DAC CH1.
LES_E103	**AUXHFRCO and LESENSE** LESENSE will not work properly at low AUXHFRCO frequencies.	LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.	Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
PRS_E101	**Edge detect on GPIO/ACMP** Edge detect on peripherals with asynchronous edges might be missed.	When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed.	Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC.
TIMER_E102	**Timer capture and debugger** Timer capture triggered when timer is halted by debugger.	When DEBUGRUN is disabled, and the capture input is HIGH it is possible to wrongly trigger a capture event by halting the MCU and starting it again (for instance by setting a breakpoint).	Enable DEBUGRUN when using a debugger.
USART_E112	**USART AUTOTX continues to transmit even with full RX buffer** USART AUTOTX continues to transmit even with full RX buffer.	When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.	No known workaround.
WDOG_E103	**WDOG EM2 detection with LFXO digital/sine input** The WDOG will mistake EM2 for EM3 if using LFXO with digital or sine input.	When the WDOG is using LFXO with digital or sine input as a clock source, it will mistake EM2 for EM3. The EM2RUN and EM3RUN bits of WDOG_CTRL will behave accordingly.	When using LFXO with digital/sine input, EM3RUN must be set to keep the WDOG running in EM2.

2 Revision History

2.1 Revision 0.6

August 21st, 2013

Added AES_E102.

Updated disclaimer, trademark and contact information.

2.2 Revision 0.50

July 30th, 2013

Added DMA_E101.

Updated errata naming convention.

2.3 Revision 0.40

November 26th, 2012

Added AES1.

Added TIMER1.

Updated with chip revision C.

2.4 Revision 0.30

April 24th, 2012

Added LES3.

2.5 Revision 0.20

January 20th, 2012

Added GPIO1.

2.6 Revision 0.10

January 9th, 2012

Initial preliminary release.

A Disclaimer and Trademarks

A.1 Disclaimer

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B Contact Information

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