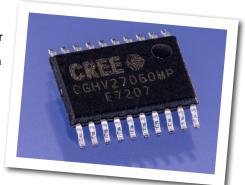


CGHV27060MP

60 W, DC - 2700 MHz, 50 V, GaN HEMT for LTE and Pulse Radar Applications

Cree's CGHV27060MP is a 60W gallium nitride (GaN) high electron mobility transistor (HEMT) housed in a small plastic SMT package 4.4mm x 6.5mm. The transistor is a broadband device with no internal input or output match which allows for the agility to apply to a wide range of frequencies from UHF thru 2.7GHz. The CGHV27060MP makes for an excellent transistor for pulsed applications at UHF, L Band or low S Band (<2.7GHz). Additionally, the transistor is well suited for LTE micro basestation amplifiers in the power class of 10 to 15W average power in high efficiency topologies such as Class A/B, F or Doherty amplifiers.



PN: CGHV27060MP

Typical Performance Over 2.5 - 2.7 GHz (T_c = 25°C) of Demonstration Amplifier

Parameter	2.5 GHz	2.6 GHz	2.7 GHz	Units
Gain @ 41.5 dBm Avg P _{OUT}	18.25	18.5	18.25	dB
ACLR @ 41.5 dBm Avg P _{out}	-34	-37	-38	dBc
Drain Efficiency @ 41.5 dBm Avg P _{out}	33	35	33	%

Note:

Measured in the CGHV27060MP-TB amplifier circuit, under WCDMA 3GPP test model 1, 64 DPCH, 45% clipping, PAR = $7.5 \, dB \, @ 0.01\%$ Probability on CCDF, V_{DD} = $50 \, V$, I_{DS} = $125 \, mA$.

Typical Performance Over 2.5 - 2.7 GHz (T_c = 25°C) of Demonstration Amplifier

Parameter	2.5 GHz	2.6 GHz	2.7 GHz	Units
Gain	16.5	16.3	16.2	dB
Output Power	84	82	79	W
Drain Efficiency	71	69	65	%

Note:

Measured in the CGHV27060MP-TB amplifier circuit, under pulse width 100 μ s, 10% duty cycle, P_{IN} = 33 dBm.

Features - WCDMA

- 2.5 2.7 GHz Reference Design Amplifier
- 18.5 dB Gain at 14 W P_{AVE}
- -35 dBc ACLR at 14 W P_{AVE}
- 35% Efficiency at 14 W P_{AVE}
- · High Degree of DPD Correction Can be Applied

Features - Pulsed

- 16.5 dB Gain at Pulsed P_{SAT}
- 70% Efficiency at Pulsed P_{SAT}
- 80W at Pulsed P_{SAT}





Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V _{DSS}	150	Volts	25°C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25°C
Storage Temperature	T _{STG}	-65, +150	°C	
Operating Junction Temperature	$T_{_{J}}$	225	°C	
Maximum Forward Gate Current	I _{GMAX}	10.4	mA	25°C
Maximum Drain Current ¹	I _{DMAX}	6.3	А	25°C
Soldering Temperature ²	T _s	245	°C	
Thermal Resistance, Junction to Case ³	R _{eJC}	2.6	°C/W	85°C, P _{DISS} = 52 W
Thermal Resistance Pulsed 10%, 100 µs, Junction to Case	$R_{_{ heta JC}}$	1.95	°C/W	85° C, P_{DISS} = 62W, 100 μ s/10%
Case Operating Temperature⁴	T _c	-40, +90	°C	cw

Note:

Electrical Characteristics (T_c = 25°C)

Characteristics	Symbol	Min.	Тур.	Max.	Units	Conditions
DC Characteristics ¹						
Gate Threshold Voltage	$V_{\rm GS(th)}$	-3.8	-3.0	-2.3	V _{DC}	V _{DS} = 10 V, I _D = 10.4 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	-	-2.7	-	V _{DC}	V _{DS} = 50 V, I _D = 125 mA
Saturated Drain Current ²	I _{DS}	8.4	10.4	-	А	$V_{DS} = 6.0 \text{ V, } V_{GS} = 2.0 \text{ V}$
Drain-Source Breakdown Voltage	$V_{_{\mathrm{BR}}}$	150	-	-	V _{DC}	V_{GS} = -8 V, I_{D} = 10.4 mA
RF Characteristics ⁵ (T _c = 25°C, F ₀ = 2.7 GH	z unless otherw	vise noted)				
Saturated Output Power ^{3,4}	P_{SAT}	-	80	-	W	V _{DD} = 50 V, I _{DQ} = 125 mA
Pulsed Drain Efficiency ^{3,4}	η	-	70	-	%	V_{DD} = 50 V, I_{DQ} = 125 mA, P_{OUT} = P_{SAT}
Gain ^{3,4}	G	-	16.5	-	dB	V_{DD} = 50 V, I_{DQ} = 125 mA, P_{OUT} = P_{SAT}
Gain ⁶	G	-	18.5	-	dB	$V_{DD} = 50 \text{ V, } I_{DQ} = 125 \text{ mA, } P_{OUT} = 41.5 \text{ dBm}$
WCDMA Linearity ⁶	ACLR	-	-35	-	dBc	$V_{DD} = 50 \text{ V, } I_{DQ} = 125 \text{ mA, } P_{OUT} = 41.5 \text{ dBm}$
Drain Efficiency ⁶	η	-	34	-	%	$V_{DD} = 50 \text{ V, } I_{DQ} = 125 \text{ mA, } P_{OUT} = 41.5 \text{ dBm}$
Output Mismatch Stress ³	VSWR	-	-	TBD	Ψ	No damage at all phase angles, $V_{\rm DD}$ = 50 V, $I_{\rm DQ}$ = 125 mA, $P_{\rm OUT}$ = 60 W Pulsed
Dynamic Characteristics						
Input Capacitance ⁷	C_{GS}	-	15.3	-	pF	$V_{DS} = 50 \text{ V, } V_{gs} = -8 \text{ V, f} = 1 \text{ MHz}$
Output Capacitance ⁷	C _{DS}	-	4.7	-	pF	$V_{DS} = 50 \text{ V, } V_{gs} = -8 \text{ V, f} = 1 \text{ MHz}$
Feedback Capacitance	C_{GD}	-	0.5	-	pF	$V_{DS} = 50 \text{ V, } V_{gs} = -8 \text{ V, f} = 1 \text{ MHz}$

Notes:

¹ Current limit for long term, reliable operation.

² Refer to the Application Note on soldering at http://www.cree.com/rf/document-library

³ Measured for the CGHV27060MP

 $^{^{\}rm 4}$ See also, the Power Dissipation De-rating Curve on Page 4.

¹ Measured on wafer prior to packaging.

² Scaled from PCM data.

 $^{^3}$ Pulse Width = 100 μ s, Duty Cycle = 10%

 $^{^4}P_{SAT}$ is defined as $I_{GS} = 1.0$ mA peak

⁵ Measured in CGHV27060MP-TB.

 $^{^6}$ Single Carrier WCDMA, 3GPP Test Model 1, 64 DPCH, 45% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF, V_{DD} = 50 V.

⁷ Includes package.



Typical Performance

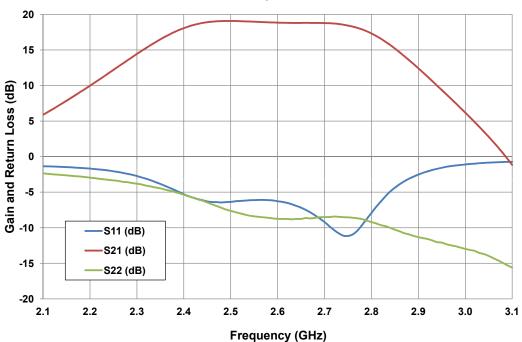
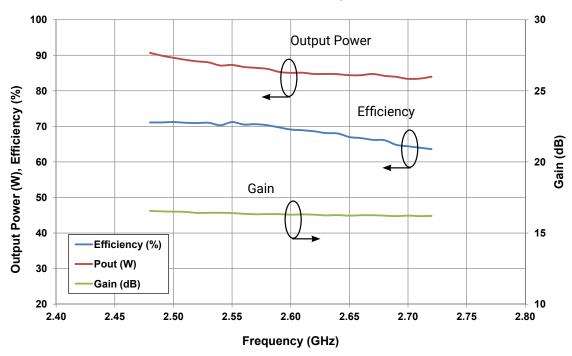


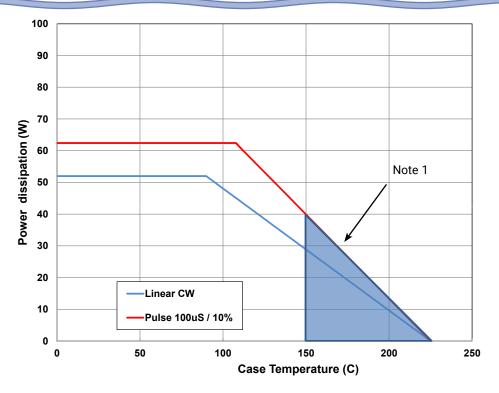
Figure 1. - Small Signal Gain and Return Losses of the CGHV27060MP Measured in Demonstration Amplifier Circuit CGHV27060MP-TB

Figure 2. - Gain, Power Added Efficiency & Average Power Output at 10% Duty Cycle for the CGHV27060MP Measured in Demonstration Amplifier Circuit CGHV27060MP-TB





CGHV27060MP Power Dissipation De-rating Curve



Note 1. Area exceeds Maximum Case Temperature (See Page 2).

Electrostatic Discharge (ESD) Classifications

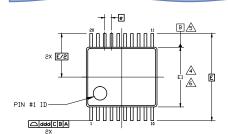
Parameter	Symbol	Class	Test Methodology
Human Body Model	НВМ	1A (> 250 V)	JEDEC JESD22 A114-D
Charge Device Model	CDM	2 (125 V to 250 V)	JEDEC JESD22 C101-C

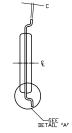
Moisture Sensitivity Level (MSL) Classification

Parameter	Symbol	Level	Test Methodology
Moisture Sensitivity Level	MSL	3 (168 hours)	IPC/JEDEC J-STD-20



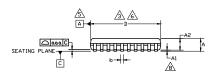
Product Dimensions CGHV27060MP (4.4 mm TSSOP 20-Lead Package)

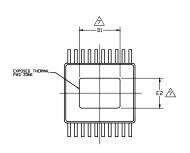


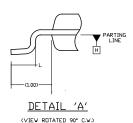


NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
- ⚠ DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
- $\underline{\underline{\mathbb{A}}}$ DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE
- riangle datums a and b to be determined at datum plane H.
- ⚠ DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.
- 7. "D1" AND "E2" DIMENSIONS DO NOT INCLUDE MOLD FLASH.
- $\stackrel{\textstyle \bigodot}{\underline{}}$ at is defined as the vertical clearance from the seating plane to the lowest point on the package BODY.







S , .				
M _B	DI	MENSIO	NS	N _D
٦	MIN.	NDM.	MAX.	N _O TE
Α			1.10	
A ₁	0.05		0.15	8
Aa	0.85	0.90	0.95	
aaa	0.076			
b	0.19	ı	0.30	
_	0.09	ı	0.20	
D	6.40	6.50	6.60	3,6
E1	4.30	4.40	4.50	4,6
e 0.65 BSC				
Е	6.40 BSC			
	0.50	0.60	0.70	
D1	4.10	4.20	4.30	7
E2	2.90	3.00	3.10	7
ddd		0.20		

 PINDUT TABLE

 PIN
 FUNCTION

 1
 GND

 2
 GND

 3
 RF INPUT

 4
 RF INPUT

 5
 RF INPUT

 6
 RF INPUT

 9
 GND

 10
 GND

 11
 GND

 12
 GND

 13
 RF DUTPUT

 14
 RF DUTPUT

 15
 RF DUTPUT

 16
 RF DUTPUT

 16
 RF DUTPUT

 18
 RF DUTPUT

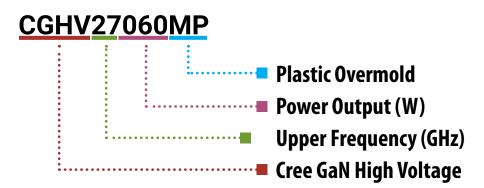
 18
 RF DUTPUT

 19
 GND

 20
 GND



Part Number System



Parameter	Value	Units
Upper Frequency ¹	2.7	GHz
Power Output	60	W
Package	MP	-

Table 1.

Note¹: Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Character Code	Code Value
А	0
В	1
С	2
D	3
E	4
F	5
G	6
Н	7
J	8
K	9
Examples:	1A = 10.0 GHz 2H = 27.0 GHz

Table 2.



Product Ordering Information

Order Number	Description	Unit of Measure	lmage
CGHV27060MP	GaN HEMT	Each	CCHY2720GONP
CGHV27060MP-AMP1	Test board with GaN HEMT installed	Each	



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