

PIC16F87XA Rev. B0 Silicon Errata Sheet

The PIC16F87XA Rev. B0 parts you have received conform functionally to the Device Data Sheet (DS39582B), except for the anomalies described below. This Errata Sheet supersedes any previously published Errata for PIC16F87XA Rev. B0.

All the problems listed here will be addressed in future revisions of the PIC16F87XA silicon.

Work around

This problem is specific to the Rev. B0 and has been resolved by Rev. B2 of the silicon (date codes later than 0242xxx).

1. Module: A/D (Electrical Specifications)

Note: This issue applies **only** to 28-pin parts of this device family (PIC16F873A and PIC16F876A). PIC16F874A and PIC16F877A devices are **not** affected.

The linearity and error specifications of the A/D module vary from the originally published specifications. The new values for 28-pin devices are shown in Table 1 (below).

To meet these specifications while operating the microcontroller at the maximum clock speed of 20 MHz, the A/D conversion clock must always be configured for divide-by-64 operation (ADCON0<7:6> = 10, ADCON1<6> = 1).

The 40-pin devices of the PIC16F87XA product family continue to meet the previously published specifications in the Device Data Sheet.

**TABLE 1: A/D CONVERTER CHARACTERISTICS (PARTIAL): PIC16F873A/876A (INDUSTRIAL)
PIC16LF873A/876A (INDUSTRIAL)**

Param No.	Sym.	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
A03	EIL	Integral linearity error	PIC16F873A/876A	—	—	±1.4	—	—	<±1	LSb
A04	EDL	Differential linearity error	PIC16F873A/876A	—	—	±1.4	—	—	<±1	LSb
A07	EGN	Gain error	PIC16F873A/876A	—	—	±2.0	—	—	<±1	LSb

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2. Module: Flash Program Memory

To ensure proper reading of data from tables in Flash Program Memory, as described in Section 3.5 of the Device Data Sheet, the following work around is necessary.

Work around

A software workaround will enable Flash program memory to function as published. One NOP should precede and six NOPs should follow the instruction that sets the read bit.

Replace the required 3-instruction sequence, shown in Example 3-3 of the Data Sheet, with the sequence shown in Example 1 (below). The interrupts should be disabled during this process.

This problem is specific to Rev. B0 and has been resolved by Rev. B2 of the silicon (date codes later than 0242xxx).

EXAMPLE 1:

```
BCF    INTCON, GIE    ;Disable the interrupts
NOP                    ;This NOP is required for the workaround.
BSF    EECON1, RD     ;This initiates program memory read.
NOP                    ;Any instructions here are ignored while program memory is read in the
NOP                    ;second instruction cycle after BSF EECON1, RD.
NOP                    ;These four NOP's are required for the workaround.
NOP
NOP
NOP
BSF    INTCON, GIE    ;Enable the interrupts
```

3. Module: Core

Certain code sequence and placement may cause the corruption of a few bits in the instruction fetch when the part is used above 4 MHz. A corrupted instruction fetch will cause the part to execute an improper instruction and result in unpredictable outputs.

Microchip cannot predict which code sequences and placement will cause this failure. If this failure mechanism exists in your system, it should be evident during statistically significant preproduction testing (minimum suggested sample size 100 units) of your particular code sequence and placement.

Any code change should be tested in the same manner prior to their implementation. If most parts fail your tests, or if failures are seen at all voltages or at all frequencies, this indicates that the problem experienced does not relate to this failure mechanism.

This problem has not been observed at operating frequencies below 4 MHz.

Work around

Use the part at or below 4 MHz.

This problem is specific to Rev. B0 and has been resolved by Rev. B2 of the silicon (date codes later than 0242xxx).

4. Module: A/D (Operation)

The ADC is disabled when $ADCON1\langle 3:0 \rangle = 011x$ (all inputs digital) and $CMCON\langle 2:0 \rangle = 111$ (comparators are off).

This is a special case that conflicts with the second sentence of Note 1 on page 131 of the device data sheet: "Pins configured as digital inputs will convert an analog input."

Work around

For the ADC module to be enabled, it is necessary to either:

1. Enable the comparators ($CMCON\langle 2:0 \rangle \neq 111$).
2. Configure at least one ADC channel as an analog input ($ADCON1\langle 3:0 \rangle \neq 011x$).

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39582B), the following clarifications and corrections should be noted.

None.

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APPENDIX A: REVISION HISTORY

Rev A Document (5/2002)

First revision of this document. Added silicon issues 1 (A/D) and 2 (Flash Program Memory).

Rev B Document (8/2002)

Added silicon issues 3 (Oscillator) and 4 (A/D Operation).

Added data sheet clarification issue 1 (Comparator).

Rev C Document (12/2002)

Replaced silicon issue 3 (Oscillator) with (Core).

Updated silicon issues 1 (A/D Electrical Specifications), 2 (Flash Program Memory) and 4 (A/D Operation).

Rev D Document (3/2003)

Added data sheet clarification issue 2 (Packaging – Pinout and Product Identification).

Rev E Document (9/2003)

Added data sheet clarification issue 3 (Voltage Reference Specifications).

Rev F Document (10/2003)

Removed all data sheet clarification issues because of updated data sheet revision.

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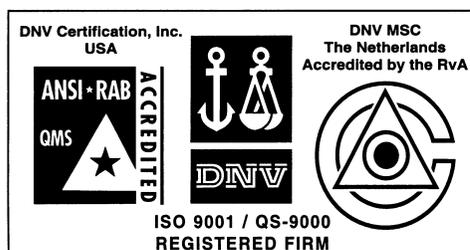
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