Enpirion EN2390QI DC-DC Converter w/Integrated Inductor Evaluation Board

Introduction

Thank you for choosing Altera Enpirion power products!

This evaluation board user guide applies to the EN2390 devices mounted on PCB's with the part number 06907 Rev A. and two extra components on the backside. In addition to this document, you will also need the latest device datasheet.

- The EN2390QI features integrated inductor, power MOSFETS, controller, a bulk of the compensation network, and protection circuitry against system faults. This level of integration delivers a substantial reduction in footprint and parts count over competing solutions. The evaluation board is optimized for engineering ease of testing through programming options, clip leads, test points etc.

- The EN2390QI features a customer programmable output voltage by means of a resistor divider. The resistor divider allows the user to set the output voltage to any value within the range 0.75V to 3.3V. The evaluation board, as shipped is populated with a 4 resistor divider option. The upper resistor is fixed and has a phase lead capacitor in parallel. One of the 4 lower resistors is selected with the jumper option for different output voltages. To change V_{OUT}, retain the upper resistor and capacitor and change only the lower resistor.

- The input and output capacitors are X5R or X7R multi-layer ceramic chip capacitors. The Soft-start capacitor is a small value X7R MLCC. Pads are available to have multiple input and output capacitors. This allows for evaluation of performance over a wide range of input/output capacitor combinations.

- Clip-on terminals are provided for ENA and POK. Banana jacks are provided for $12V_{IN}$, AVIN, and V_{OUT} terminals. Several signal and GND clip-on test points are also provided to measure V_{IN}, V_{OUT}, and GND nodes.

- A jumper is provided for controlling the Enable signal. Enable may also be controlled using an external switching source by removing the jumper and applying the enable signal to the ENA clip-on terminal.

- Foot print is also provided for an SMA connector to S_IN input. A switching input to this pin allows the device clock to be phase locked to an external signal. This external clock synchronization allows for moving any offending beat frequency to be moved out-of-band. A swept frequency applied to this pin results in spread spectrum operation and reduces the peaks in the noise spectrum of emitted EMI.

- A two pin header footprint is provided for the S_OUT pin. This signal can be used to synchronize another EN2390 to the switching frequency coming out of the S_OUT pin.

- The board comes with input decoupling and PVIN (12VIN) reverse polarity protection to guard the device against common setup mishaps. Please note there is no reverse polarity protection on AVIN input.

Quick Start Guide

STEP 1: Set the ENA jumper J3 to the Disable Position, as shown in Figure 1.

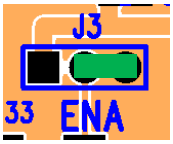


Figure 1: Shows the Enable jumper in the DISABLE position.

STEP 2: With power off, connect the 12V nominal Power Supply to the input power connectors, 12VIN (J7) and GND (J11) as indicated in Figure 4.

> **CAUTION**: Be mindful of the polarity. Even though the evaluation board comes with reverse polarity protection diodes, it may not protect the device under all conditions.

STEP 3: Make sure the two-in header J1 is properly populated depending on how you want to power AVIN. If you want to use the device in a single input supply mode, and use the on-chip AVINO pin, then populate J1 with a shorting jumper. If you want to supply your own external AVIN, then remove the jumper from J1, and connect a 3.3V nominal power supply to the AVIN (J9) and GND (J11).

> **NOTE**: When using the external AVIN mode with long wires coming to the board, it may be necessary to populate an 0805 tantalum capacitor in the C16 position. This capacitor should not be on the board when using the single-supply mode.

> **CAUTION**: be mindful of the AVIN input polarity. There is no reverse polarity protection on this input.

CAUTION: Do not apply an external AVIN to the device with the J1 jumper populated. Doing so will damage the device.

STEP 4: Connect the load to the output connectors VOUT (J6) and GND (J10), as indicated in Figure 4.

STEP 5: Select the output voltage setting jumper. Figure 2 shows what output voltages are achieved by selecting each jumper position. Note that depending on the tolerance of the resistors populated on the board, each output voltage setting may have a larger tolerance than just the VFB pin as specified in the datasheet. Please see Figure 5 and the Bill of Materials section.

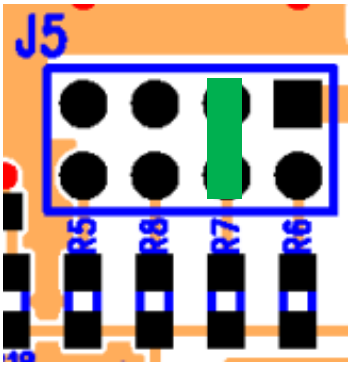


Figure 2: Output Voltage selection jumpers J5. Nominal jumper position voltages from left to right are: 3.31V, 1.8V, 1.2V and 1.0V. Jumper shown selects 1.20V output Do not change jumper positions while the board is powered.

Please note: The loop compensation circuit for this version of evaluation board has been chosen for a wide range of PVIN and V_{OUT} values using output capacitors for best performance. In order to optimize the loop for any specific PVIN/V_{OUT} operating point, please see the compensation table in the datasheet. See Figures 4 and 5.

STEP 6: Apply AVIN (either through AVINO output or through an external voltage), and $12V_{IN}$ to the device. **Please note the allowable slew rate range on PVIN as specified in the datasheet.** Next, move the ENA jumper to the enabled position. The EN2390QI is now powered up. Various measurements such as efficiency, line and load regulation, input / output ripple, load transient, drop-out voltage measurements may be conducted at this point. The under voltage lock out thresholds, and temperature coefficient of the output voltage may also be measured in this configuration.

Alternatively, you can leave the ENA jumper in the enabled position, and turn on the device using the input voltage PVIN. **Please note the allowable slew rate range on PVIN as specified in the datasheet.** Please review the Power Up Sequence section in the datasheet before turning the unit on using PVIN.

CAUTION: Please refer to the datasheet for the maximum voltages on the 12V (PVIN) and AVIN inputs. THIS DEVICE CANNOT BE HOT-PLUGGED INTO A 12V RAIL.

STEP 6A: Power Up/Down Behavior – Remove ENA jumper and connect a pulse generator (output disabled) signal to the clip-on test point below ENA and Ground. Set the pulse amplitude to swing from 0 to 2.5 volts. Set the pulse period to 10msec. and duty cycle to 50%. Hook up oscilloscope probes to ENA, SS, POK and VOUT with clean ground returns. Apply power to evaluation board. Enable pulse generator output. Observe the SS capacitor and VOUT voltage ramps as ENA goes high and again as ENA goes low. The device when powered down ramps down the output voltage in a controlled manner before fully shutting down. The output voltage level when POK is asserted /de-asserted as the device is powered up / down may be observed as well as the clean output voltage ramp and POK signals.

STEP 7: External Clock Synchronization / Spread Spectrum Modes: In order to activate this mode, it may be necessary to a solder a SMA connector at J4. Alternately the input clock signal leads may be directly soldered to the through holes of J4 as shown below.

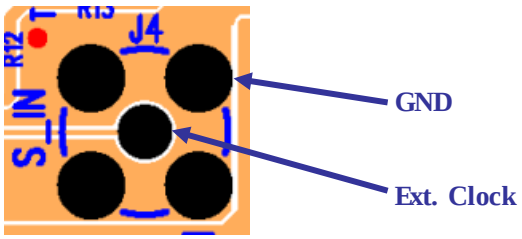


Figure 3: SMA Connector for External Clock Input

Power down the device. Move ENA into disable position. Connect the clock signal as just indicated. The clock signal should be clean and have a frequency in the range of the nominal frequency ±10%; amplitude 0 to 2.5 volts with a duty cycle between 20 and 80%. With S_IN signal disabled, power up the device and move ENA jumper to Enabled position. The device is now powered up and outputting the desired voltage. The device is switching at its free running frequency. The switching waveform may be observed between test points SW and GND. Now enabling the S_IN signal will automatically phase lock the internal switching frequency to the externally applied frequency as long as the external clock parameters are within the specified range. To observe phase-lock connect oscilloscope probes to the input clock as well as to the SW test point. Phase lock range can be determined by sweeping the external clock frequency up / down until the device just goes out of lock at the two extremes of its range.

For spread spectrum operation the input clock frequency may be swept between two frequencies that are within the lock range. The sweep (jitter) repetition rate should be limited to 10 kHz. The radiated EMI spectrum may be now measured in various states – free running, phase locked to a fixed frequency and spread spectrum.

Before measuring radiated EMI, place a 10uF X7R or X5R capacitor at the input and output edges of the PCB (C8 and C9 positions), and connect the PVIN power and the load to the board at or near these capacitors. The added capacitor at the input edge is for high-frequency decoupling of the input cables. The one added at the output edge is meant to represent a typical load decoupling capacitor. We recommend doing EMI testing in single-supply mode only as this will simplify the test setup.

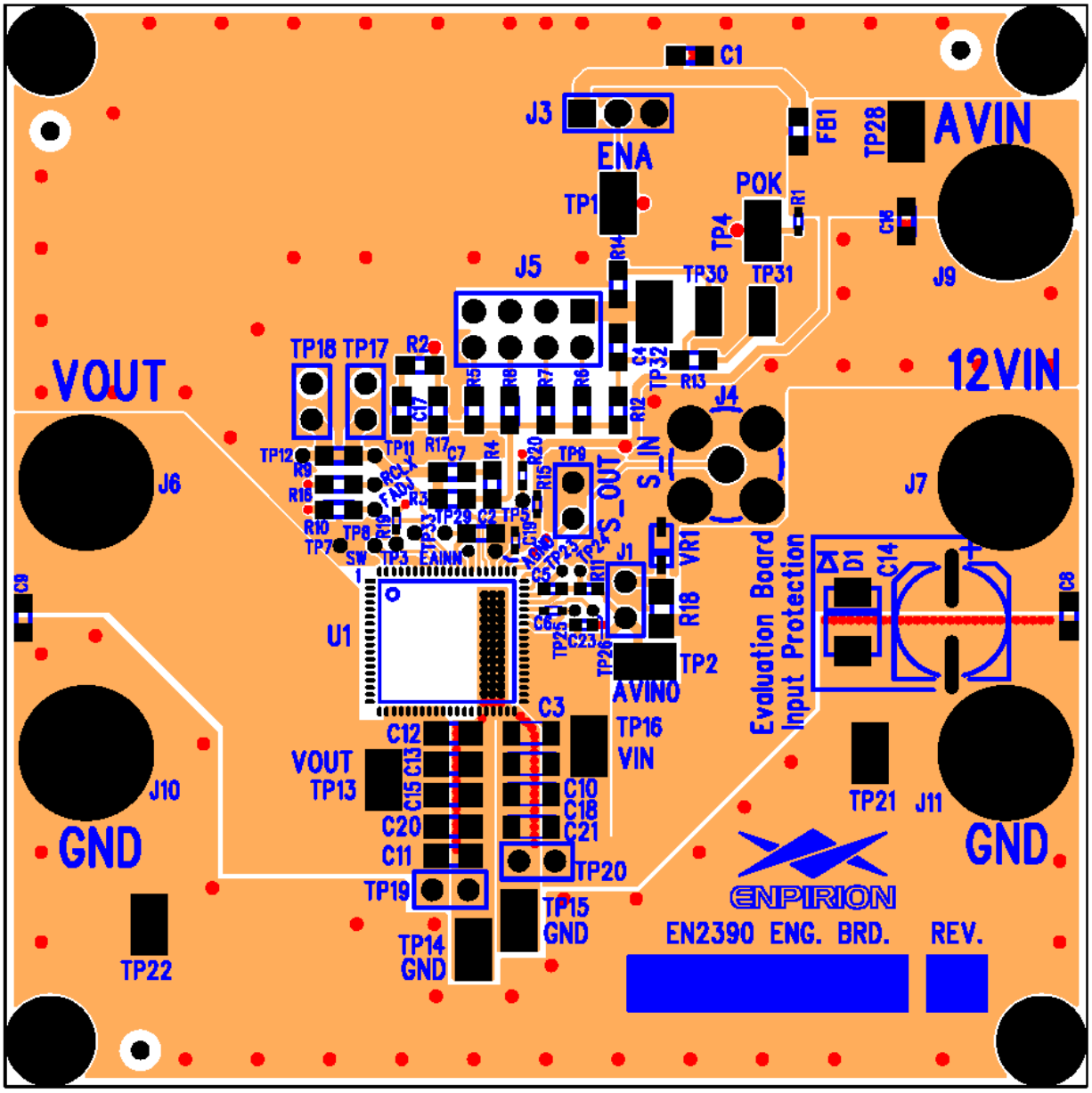


Figure 4: Evaluation Board Top and Assembly Layers.

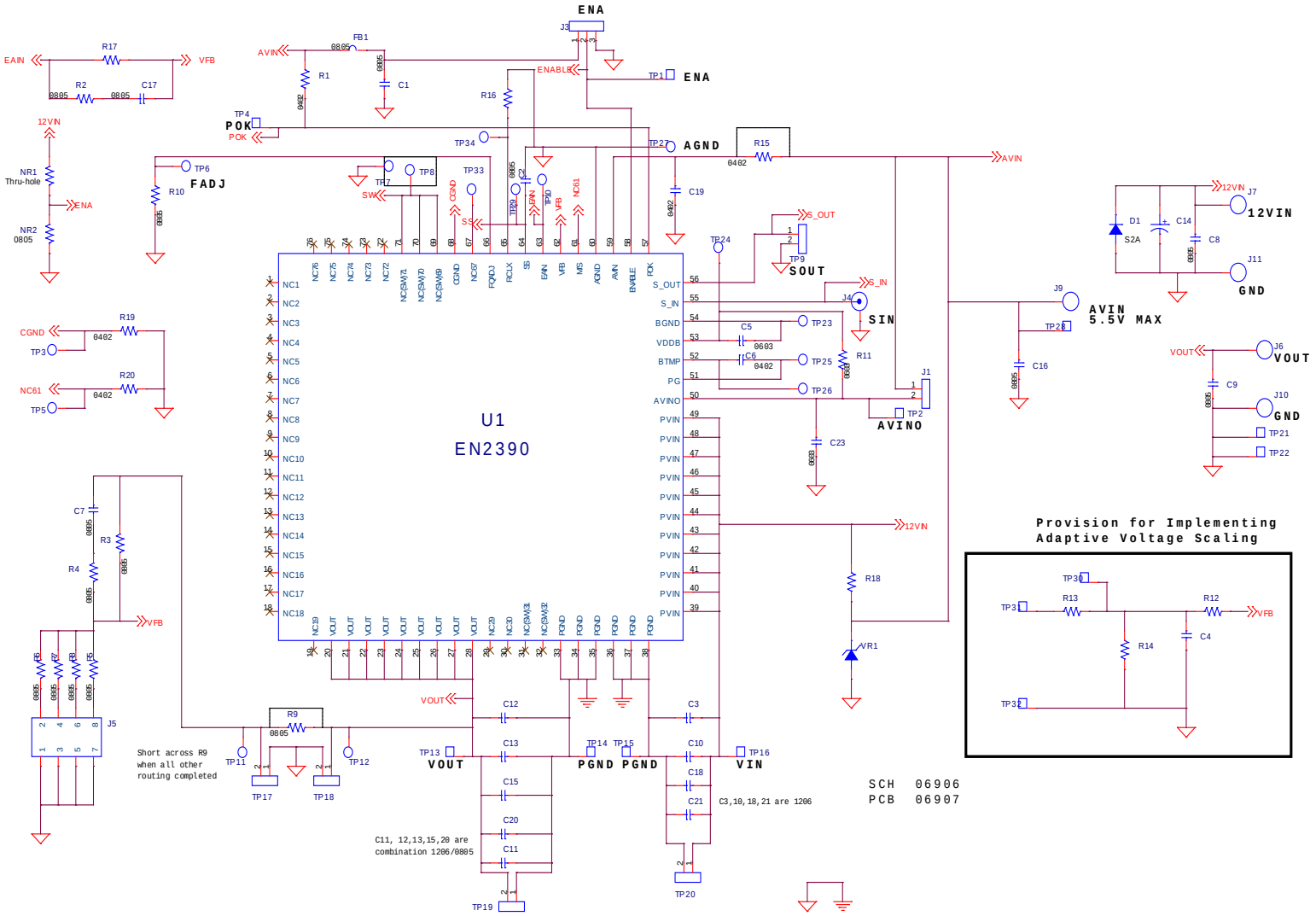
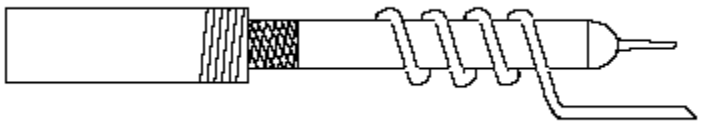


Figure 5: EN2390 Evaluation Board Schematic (NR1 & NR2 are additional components on the back side)

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided (TP13 to TP16). This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a low-loop-inductance scope probe tip similar to one shown below to measure switching signals and input / output ripple to avoid noise coupling into the probe ground lead. Input ripple, output ripple, and load transient deviation are best measured near the respective input / output capacitors. For more accurate ripple measurement, please see Enpirion App Note regarding this subject.



4. The board includes a pull-up resistor for the POK signal and ready to monitor the power OK status at clip lead marked POK.
5. This product has built-in short-circuit protection. If protection against an overload condition is required, an appropriate external solution needs to be used. Please refer to the Enpirion application note for further details on this subject.

Bill of Materials

Designator	Qty	Description
C2	1	CAP, 47000PF 0805 X7R 10% 50V CERAMIC
C3, C10	2	CAP, 22UF 1206 X5R 10% 25V CERAMIC
C5	1	CAP CER 0.22UF 16V X5R 0402
C6	1	CAP, 47000PF 0402 X7R 10% 25V CERAMIC
C7	1	CAP, 33PF 0805 NP0 5% 50V CERAMIC
C12	1	CAP CER 100UF 6.3V X5R 1206
C13, C15	2	CAP CER 47UF 10V X5R 1206
C14	1	CAP, SMT ELECTROLYTIC, 150UF, 25V
C19, C23	2	CAP, 1.0UF 0402 X5R 10% 10V CERAMIC
C1, C4, C8, C9, C11, C16-C18, C20, C21, FB1, J4, R2, R9, R12-R15, R18, R20, VR1	21	NOT USED
D1	1	S2A DIODE, Micro Commercial S2A-TP
FB1	1	SMT FERRITE BEAD 4A 0805, Wurth Electronik 742792012
J1	1	CONNECTOR HEADER, 2 POSITION, Samtec TSW-102-07-T-S
J3	1	CONNECTOR HEADER, 3 POSITION, Samtec TSW-103-07-T-S
J5	1	CONNECTOR HEADER, 8 POSITION Dual, Samtec TSW-104-24-T-D
J6, J7, J9-J11	5	BANANA JACK, KEYSTONE 575-4
R1	1	RES 100K OHM 1/16W 1% 0402 SMD
R3, R7	2	RES 200K OHM 1/8W 0.1% 0805 SMD
R4	1	RES ZERO OHM 1/8W 5% 0805 SMD
R5	1	RES 44.2K OHM 1/8W 1% 0805 SMD
R6	1	RES 301K OHM 1/8W 0.1% 0805 SMD
R8	1	RES 100K OHM 1/8W 0.1% 0805 SMD
R10	1	RES 3.01K OHM 1/8W 1% 0805 SMD
R11	1	RES 4.75K OHM 1/10W 1% 0402 SMD
R16	1	RES 100K OHM 1/8W 1% 0805 SMD
R17	1	RES 33.2K OHM 1/8W 1% 0805 SMD
R19	1	RES ZERO OHM 1/10W 5% 0402 SMD
TP1, TP2, TP4, TP13-TP16, TP21,TP22, TP28,TP32	11	TEST POINT SURFACE MOUNT, KEYSTONE 5016
TP30, TP31	2	TEST POINT SURFACE MOUNT, KEYSTONE 5015
U1	1	EN2390QI QFN 9A
NR1	1	RES 10.0 OHM 1/4W 1% AXIAL
NR2	1	RES 2.26K OHM 1/4W 1% 0805 SMD

Validation Status: EN2390QI – 02

This device is an engineering sample and may not meet one or more of the specifications itemized in the product datasheet. Validation testing is currently in progress. Validation tests completed and yet to be done are summarized below. These devices are being provided for early evaluation and feedback.

VALIDATION COMPLETED TO DATE

The following tests have been completed at room temperature unless otherwise noted:

- Efficiency and Power Loss
- Load Regulation
- Line Regulation
- Ripple
- Load Transient Response
- Stability/Bode Measurements
- Design Verification Testing (partial)

VALIDATION TO BE COMPLETED

POK Response
Efficiency and Power Loss (-40 to 85 C)
Load Regulation (-40 to 85 C)
Line Regulation (-40 to 85 C)
Vout Temperature coefficient (-40 to 85 C)
Thermal Shutdown
Startup and Shutdown – Enable Toggled
Startup and Shutdown – Supply Power Up
Overcurrent protection and short circuit testing
Design Verification Testing (complete)
Operating temperature range testing
Datasheet Electrical Characteristics compliance

CURRENTLY IDENTIFIED ERRATA

1. Some devices may exhibit higher OCP (over current protection) threshold than expected.

CORRECTIVE ACTION PLAN

Root cause is identified. Production devices will have this issue resolved.

Contact Information

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