## PNP - MJ15023, MJ15025*

## *MJ15025 is a Preferred Device

## Silicon Power Transistors

The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

## Features

- High Safe Operating Area (100\% Tested) -2 A @ 80 V
- High DC Current Gain $-\mathrm{h}_{\mathrm{FE}}=15$ (Min) @ $\mathrm{I}_{\mathrm{C}}=8$ Adc
- $\mathrm{Pb}-$ Free Packages are Available*

MAXIMUM RATINGS


THERMAL CHARACTERISTICS

| Characteristics | Symbol | Max | Unit |
| :---: | :---: | :---: | :---: |
| Thermal Resistance, Junction-to-Case | $\mathrm{R}_{\theta \mathrm{JC}}$ | 0.70 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width $=5 \mathrm{~ms}$, Duty Cycle $\leq 10 \%$.
[^0]
## ON Semiconductor ${ }^{\circledR}$

http://onsemi.com

## 16 AMPERES

 SILICON POWER TRANSISTORS 200 - 250 VOLTS, 250 WATTS

TO-204AA (TO-3) CASE 1-07 STYLE 1

## MARKING DIAGRAM



| MJ1502x | $=$ Device Code |
| :--- | :--- |
|  | $x=3$ or 5 |
| G | $=$ Pb-Free Package |
| A | $=$ Assembly Location |
| Y | $=$ Year |
| WW | $=$ Work Week |
| MEX | $=$ Country of Origin |

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MJ15023 | TO-204 | 100 Units / Tray |
| MJ15023G | TO-204 <br> (Pb-Free) | 100 Units / Tray |
| MJ15025 | TO-204 | 100 Units / Tray |
| MJ15025G | TO-204 <br> (Pb-Free) | 100 Units / Tray |

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}\right.$ unless otherwise noted)

| Characteristic |  | Symbol | Min | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OFF CHARACTERISTICS |  |  |  |  |  |
| Collector-Emitter Sustaining Voltage (Note 2) $\left(\mathrm{I}_{\mathrm{C}}=100 \mathrm{mAdc}, \mathrm{I}_{\mathrm{B}}=0\right)$ | MJ15023 <br> MJ15025 | $\mathrm{V}_{\text {CEO(sus) }}$ | $\begin{aligned} & 200 \\ & 250 \end{aligned}$ | - | - |
| $\begin{aligned} & \text { Collector Cutoff Current } \\ & \left(\mathrm{V}_{\mathrm{CE}}=200 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{BE} \text { (off) })}=1.5 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{CE}}=250 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{BE}}(\text { off })=1.5 \mathrm{Vdc}\right) \end{aligned}$ | MJ15023 <br> MJ15025 | $I_{\text {CEX }}$ |  | $\begin{aligned} & 250 \\ & 250 \end{aligned}$ | $\mu \mathrm{Adc}$ |
| $\begin{aligned} & \text { Collector Cutoff Current } \\ & \left(\mathrm{V}_{\mathrm{CE}}=150 \mathrm{Vdc}, \mathrm{I}_{\mathrm{B}}=0\right) \\ & \left(\mathrm{V}_{\mathrm{CE}}=200 \mathrm{Vdc}, \mathrm{I}_{\mathrm{B}}=0\right) \end{aligned}$ | MJ15023 <br> MJ15025 | $I_{\text {CEE }}$ | - | $\begin{aligned} & 500 \\ & 500 \end{aligned}$ | $\mu \mathrm{Adc}$ |
| Emitter Cutoff Current $\left(\mathrm{V}_{\mathrm{CE}}=5 \mathrm{Vdc}, \mathrm{I}_{\mathrm{B}}=0\right)$ | Both | $\mathrm{l}_{\text {ebo }}$ | - | 500 | $\mu \mathrm{Adc}$ |

SECOND BREAKDOWN
Second Breakdown Collector Current with Base Forward Biased $\left(\mathrm{V}_{\mathrm{CE}}=50 \mathrm{Vdc}, \mathrm{t}=0.5 \mathrm{~s}\right.$ (non-repetitive)) $\left(\mathrm{V}_{\mathrm{CE}}=80 \mathrm{Vdc}, \mathrm{t}=0.5 \mathrm{~s}\right.$ (non-repetitive))

| $\mathrm{I}_{\mathrm{S} / \mathrm{b}}$ |  |  | Adc |
| :--- | :--- | :--- | :--- |
|  | 5 <br> 2 | - |  |

ON CHARACTERISTICS

| $\begin{aligned} & \text { DC Current Gain } \\ & \left(I_{C}=8 \mathrm{Adc}, \mathrm{~V}_{\mathrm{CE}}=4 \mathrm{Vdc}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=16 \mathrm{Adc}, \mathrm{~V}_{\mathrm{CE}}=4 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{h}_{\text {FE }}$ | 15 5 | 60 | - |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Collector-Emitter Saturation Voltage } \\ & \left(I_{C}=8 \mathrm{Adc}, I_{\mathrm{B}}=0.8 \mathrm{Adc}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=16 \mathrm{Adc}, \mathrm{I}_{\mathrm{B}}=3.2 \mathrm{Adc}\right) \end{aligned}$ | $\mathrm{V}_{\text {CE(sat) }}$ |  | 1.4 4.0 | Vdc |
| Base-Emitter On Voltage $\left(I_{C}=8 \mathrm{Adc}, \mathrm{V}_{\mathrm{CE}}=4 \mathrm{Vdc}\right)$ | $\mathrm{V}_{\mathrm{BE} \text { (on) }}$ | - | 2.2 | Vdc |

## DYNAMIC CHARACTERISTICS

| Current-Gain - Bandwidth Product <br> $\left(\mathrm{I}_{\mathrm{C}}=1\right.$ Adc, $\left.\mathrm{V}_{\mathrm{CE}}=10 \mathrm{Vdc}, \mathrm{f}_{\text {test }}=1 \mathrm{MHz}\right)$ | $\mathrm{f}_{\mathrm{T}}$ | 4 | - | MHz |
| :--- | :---: | :---: | :---: | :---: |
| Output Capacitance <br> $\left(\mathrm{V}_{\mathrm{CB}}=10 \mathrm{Vdc}, \mathrm{I}_{\mathrm{E}}=0, \mathrm{f}_{\text {test }}=1 \mathrm{MHz}\right)$ | $\mathrm{C}_{\mathrm{ob}}$ | - | 600 | pF |

2. Pulse Test: Pulse Width $=300 \mu \mathrm{~s}$, Duty Cycle $\leq 2 \%$.


Figure 1. Active-Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_{C}-V_{C E}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.
The data of Figure 1 is based on $\mathrm{T}_{\mathrm{J}(\mathrm{pk})}=200^{\circ} \mathrm{C}$; $\mathrm{T}_{\mathrm{C}}$ is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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TYPICAL CHARACTERISTICS


Figure 2. Capacitances


Figure 4. DC Current Gain


Figure 3. Current-Gain - Bandwidth Product

Figure 5. "On" Voltages

## PACKAGE DIMENSIONS

TO-204 (TO-3)
CASE 1-07
ISSUE Z


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 1.550 REF |  | 39.37 REF |  |
| B | --- | 1.050 | --- | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC |  | 10.92 BSC |  |
| H | 0.215 BSC |  | 5.46 BSC |  |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | 0.665 BSC |  | 16.89 BSC |  |
| N | --- | 0.830 | --- | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC |  | 30.15 BSC |  |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

STYLE 1:
PIN 1. BASE 2. EMITTER CASE: COLLECTOR

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[^0]:    *For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

