

ADP2441 Evaluation Board

FEATURES

Full-featured evaluation board for the [ADP2441](#)
Configurable synchronous step down dc-dc switching regulator
Operating voltage range of board: $V_{IN} = 6\text{ V to }36\text{ V}$
Output voltage is set to 5 V or can be adjusted
Maximum load 1 A
Switching frequency set to 500 kHz or adjustable switching frequency of 300 kHz to 1 MHz
Power saving mode at light load
Precision enable input pin
Current limit protection
Power good output
External soft start set to 6 ms or external tracking available
Board size: 53 mm × 53 mm

DOCUMENTS NEEDED

[ADP2441 data sheet](#)
UG-407

GENERAL DESCRIPTION

The [ADP2441](#) evaluation board is a complete, dc-to-dc switching regulator design based on the [ADP2441](#), a configurable, 1 A, synchronous step-down, dc-to-dc regulator.

The [ADP2441](#) is a synchronous, step-down dc-to-dc switching regulator that uses a current mode pulse-width modulation (PWM) control scheme at medium-to-heavy load currents for high efficiency and smoothly transitions to a pulse skip mode at light loads to conserve power. The power switch and synchronous rectifier are integrated for minimal external part count and high efficiency. The [ADP2441](#) is optimized for operation with small ferrite core inductors and ceramic capacitors to deliver the maximum output power per square millimeter of the PCB board area.

The [ADP2441-EVALZ](#) is available with 5 V at 1 A output, switching frequency set to 500 kHz. If needed, the [ADP2441](#) evaluation board configuration can be modified by changing the values of the appropriate passive components.

Complete specifications for the [ADP2441](#) device can be found in the [ADP2441](#) data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

ADP2441-EVALZ

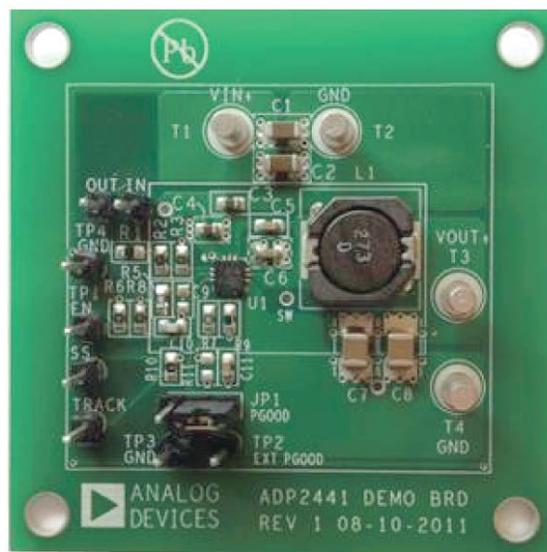


Figure 1.

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REVISION HISTORY

6/12—Initial Version: Revision 0

USING THE EVALUATION BOARD

POWERING UP THE EVALUATION BOARD

The ADP2441 evaluation board is provided fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

Input Power Source

The power source voltage must not exceed 36 V, the maximum operation input voltage of the ADP2441.

Make sure the power source is switched off before connecting it to the ADP2441 evaluation board. Connect the positive terminal of the power source to the evaluation board V_{IN} terminal (T1), and the negative terminal of the power source to the evaluation board GND terminal (T2). If the power source includes an ammeter, connect the ammeter in series with the input source voltage. Connect the positive lead (+) of the power source to the ammeter positive (+) connection, the negative lead (-) of the ammeter to the evaluation board V_{IN} terminal (T1), and the negative lead (-) of the power source to the evaluation board GND terminal (T2).

Output Load

Make sure the evaluation board is switched off before connecting the load. Connect the load directly to the evaluation board, with the positive (+) load connection to the V_{OUT} terminal (T3) and the negative (-) load connection to the GND terminal (T4). If an ammeter is used, connect it in series with the load: connect the positive (+) ammeter terminal to the evaluation board V_{OUT} terminal (T3), the negative (-) ammeter terminal to the positive (+) load terminal, and the negative (-) load terminal to the evaluation board GND terminal (T4).

Once the load is connected, make sure it is set to the proper current before powering the ADP2441 evaluation board. Before connecting a load to the output of the evaluation board, make sure that the output voltage does not exceed the maximum operating voltage range of the load.

Enabling and Disabling the DC-to-DC Switching Regulator

In the evaluation board, a voltage divider is used to generate an enable signal for the IC. As soon as voltage is applied to V_{IN} (24 V), IC is enabled.

Alternatively, header TP1 (EN) is available to enable and disable the evaluation board. To enable the output, connect the header TP1 to the V_{IN} supply or to an external voltage source. To disable the output connect the header TP1 to the GND.

PGOOD Signals

When the output is enabled and the output voltage, V_{OUT} , is in regulation, the logic signal at the PGOOD test point is high. In a typical application, a pull-up resistor from the PGOOD pin to the external supply is used to generate this logic signal.

On the evaluation board, the pull-up resistor (R7) is available to connect to the external supply through the jumper (JP1). Test Point TP2 is available to connect the external supply of 5 V.

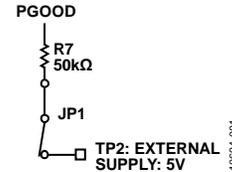


Figure 2 PGOOD Signal

External SS/TRK Signal

The SS/TRK pin is multipurpose. It can be used either for tracking the external supply or for soft start.

A header, TRK, is available on the board for connecting an external signal to be tracked by the regulator output voltage. Before applying a signal to the TRK header, make sure the voltage divider resistor values (R10, R11) connected on the evaluation board are the correct values (see the ADP2441 data sheet).

Alternatively, to program soft start time, a capacitor can be connected to SS/TRK pin. On the evaluation board, a 10 nF capacitor, C11, is connected for a soft start time of 6 ms.

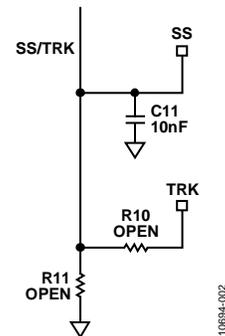


Figure 3. Soft Start Signal

MEASURING EVALUATION BOARD PERFORMANCE

Output Voltage Ripple

To observe the output voltage ripple, place an oscilloscope probe tip at Terminal T3 and connect the probe ground lead at the negative (–) Terminal T4. Set the oscilloscope to an ac-coupled, 100 mV/division and 2 μ s/division time base.

Switching Waveform

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor that is connected to the SW pin with the probe ground at Terminal T4, GND. Set the scope to dc, 5 V/division, and 2 μ s/division time base. The switching waveform should alternate between 0 V and approximately the input voltage.



Figure 4. Switch Node Measurement

Measuring Load Regulation

The load regulation should be measured by increasing the load at the output and looking at the change in output voltage. To minimize voltage drop, use short low-resistance wires, especially for heavy loads.

Measuring Line Regulation

Vary the input voltage and examine the change in the output voltage. In PWM mode, the output voltage ripple should be small (<50 mV) but in pulse skip mode, the output voltage ripple can be as large as 100 mV.

Measuring Efficiency

The efficiency, η , is measured by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of IR drops.

Inductor Current

The inductor current can be measured by removing one end of the inductor from its pad and connecting a current loop in series with it. Then a current probe can be used to measure the current flowing through the current loop.

Line Transient Response

Generate a step input voltage (V_{IN}) and observe the behavior of the output voltage, with an oscilloscope.

Load Transient Response

Generate a load current transient at the output, V_{OUT} , and observe the output voltage response with an oscilloscope. Use a current probe attached to the wire between the output and the load to visualize the current transient.

Loop Stability Measurement

Closed-loop response can be measured using a network analyzer. To measure the loop response, Header IN and Header OUT are available.

MODIFYING THE EVALUATION BOARD

The [ADP2441](#) evaluation board is provided fully assembled and tested for proper operation. The [ADP2441-EVALZ](#) has a fixed 5 V output voltage.

CHANGING THE OUTPUT VOLTAGE

The [ADP2441-EVALZ](#) output regulation voltage is set by a resistive voltage divider consisting of Resistors R2 and R3. Resistor R2 corresponds to the R_{TOP} resistor in the data sheet and Resistor R3 corresponds to the R_{BOTTOM} resistor in the data sheet. The output regulation voltage is determined by the equation

$$V_{OUT} = 0.6 \text{ V} \times \left[\frac{R2 + R3}{R3} \right]$$

where:

R2 is the value of the top resistor of the voltage divider (R_{TOP}).

R3 is the value of the bottom resistor of the voltage divider (R_{BOTTOM}).

V_{OUT} is the output regulation voltage in volts.

To set the output regulation voltage to the desired value, first determine the value of the bottom resistor, R3, by

$$R3 = \frac{V_{FB}}{I_{STRING}}$$

where:

$V_{FB} = 0.6 \text{ V}$, the internal reference.

I_{STRING} is the resistor divider string current (greater than 20 μA nominally).

Once R3 is determined, calculate the value of the top resistor, R2, by

$$R2 = R3 \left[\frac{V_{OUT} - V_{FB}}{V_{FB}} \right]$$

For example, to set the output regulation voltage of [ADP2441-EVALZ](#) to 3.3 V, calculate the value of Resistors R2 and R3 as shown in the following equations:

$$R3 = \frac{V_{FB}}{I_{STRING}} = \frac{0.6 \text{ V}}{60 \mu\text{A}} = 10 \text{ k}\Omega$$

$$\begin{aligned} R2 &= R3 \times \left[\frac{V_{OUT} - V_{FB}}{V_{FB}} \right] \\ &= 10 \text{ k}\Omega \times \left[\frac{3.3 \text{ V} - 0.6 \text{ V}}{0.6 \text{ V}} \right] = 45.3 \text{ k}\Omega \end{aligned}$$

Note that when the output voltage of [ADP2441-EVALZ](#) is changed, the output capacitors (C7 and C8), inductor (L1), and compensation components (R5 and C10) should be recalculated and changed according to the Application Information section in the [ADP2441](#) data sheet to ensure stable operation.

Table 1. Programming Output Voltage

Voltage (V)	R2 (k Ω)	R3 (k Ω)
12	190	10
5	73	10
3.3	45	10
1.2	10	10

CHANGING THE SWITCHING FREQUENCY

The switching frequency (f_{sw}) set point can be changed by replacing Resistor R9 with a different value using following equation:

$$R9 = \frac{92,500}{f_{sw}}$$

where:

R9 is the frequency resistor in k Ω .

f_{sw} is the switching frequency in kHz.

Table 2. Programming Frequency

R9 (k Ω)	Frequency (kHz)
308	300
132	700
92.5	1000

Note that when the switching frequency (f_{sw}) is changed, to ensure stable operation, the values of Inductor L1, C7, C8 (output capacitors), and R5, C10 (compensation components) must be recalculated and changed (see the [ADP2441](#) data sheet for details on external component selection).

CHANGING THE SOFT START TIME

The soft start time of the [ADP2441](#) on the evaluation board is programmed to 6 ms. To change the soft start time, t_{ss} , replace Capacitor C11 with a different capacitor value using the following equation:

$$C11 = \frac{I_{SS}}{V_{REF}} \times t_{ss}$$

where:

V_{REF} is the internal reference voltage and equals 0.6 V.

I_{SS} is the soft start current and equals 1 μA .

C11 is the soft start capacitor value.

t_{ss} is the soft start time

TYPICAL PERFORMANCE CHARACTERISTICS

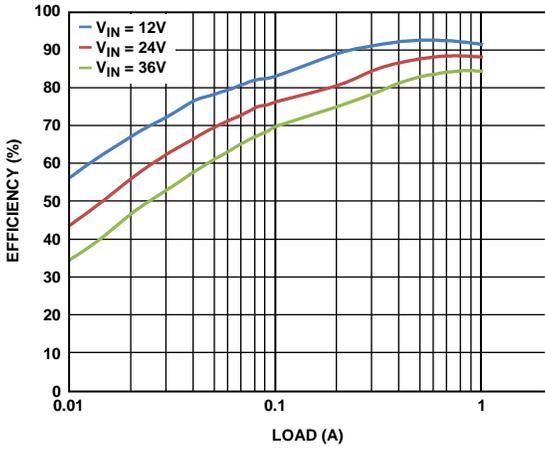


Figure 5. Efficiency vs. Load Current, $V_{OUT} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$

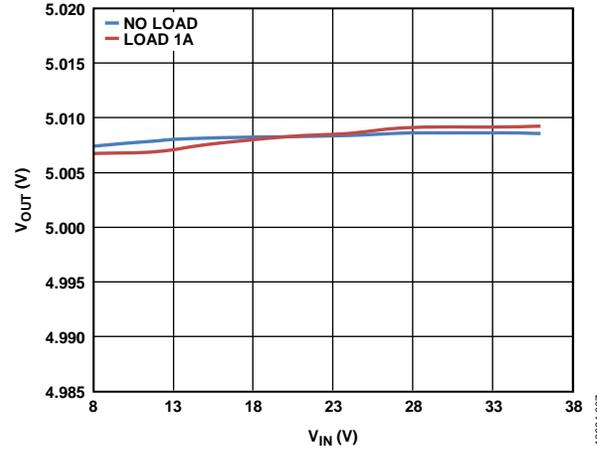


Figure 8. Line Regulation, $V_{OUT} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$

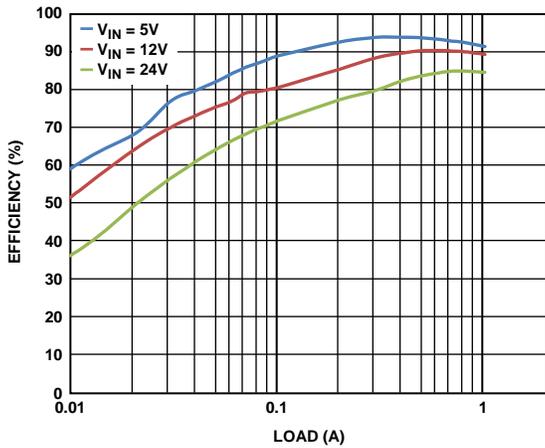


Figure 6. Efficiency vs. Load Current, $V_{OUT} = 3.3\text{ V}$, $f_{SW} = 500\text{ kHz}$

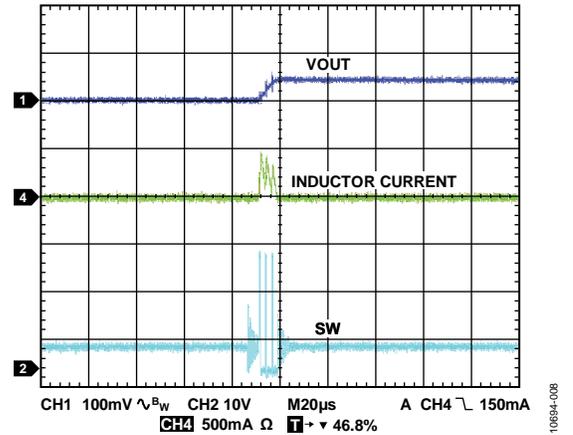


Figure 9. Pulse Skip Waveform
 $V_{IN} = 24\text{ V}$; $V_{OUT} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$, No Load

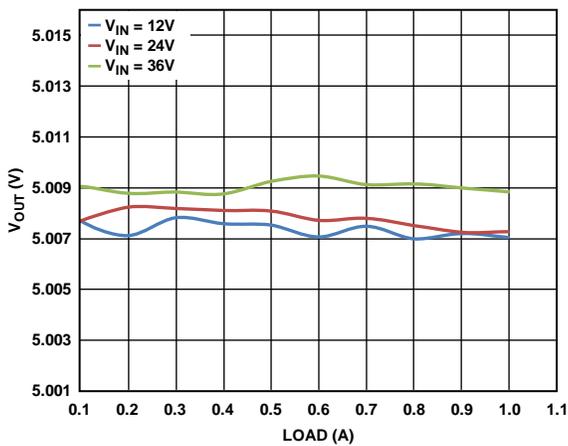


Figure 7. Load Regulation, $V_{OUT} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$

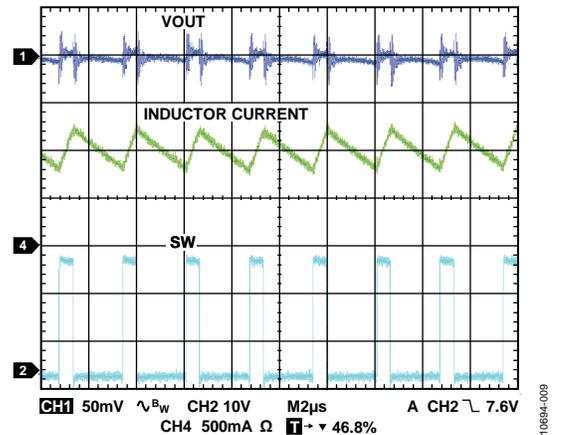


Figure 10. PWM Waveform, $V_{IN} = 24\text{ V}$, $V_{OUT} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$, Load = 1 A

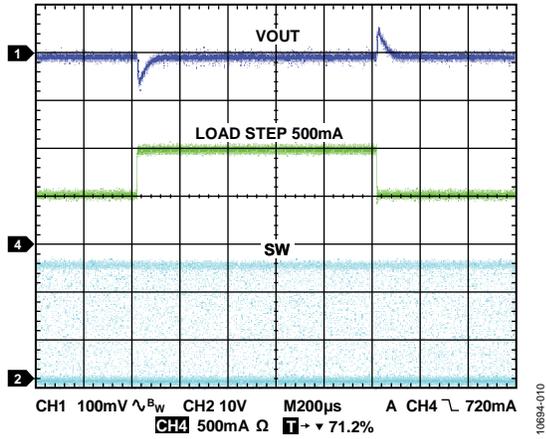


Figure 11. Load Transient, $V_{IN} = 24\text{ V}$, $V_{OUT} = 5\text{ V}$, 500 mA Step

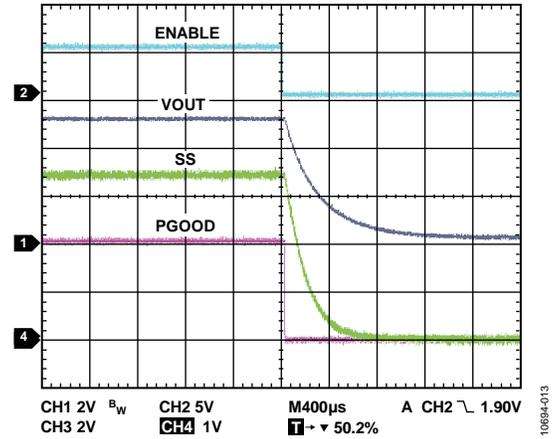


Figure 14. Shutdown; $V_{IN} = 24\text{ V}$, $V_{OUT} = 5\text{ V}$, Load $5\ \Omega$

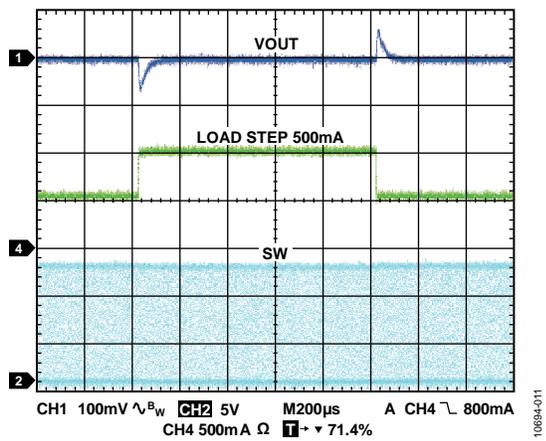


Figure 12. Load Transient, $V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, 500 mA

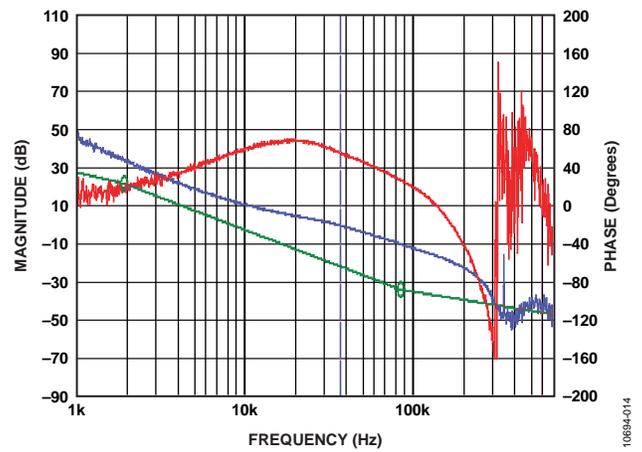


Figure 15. Bode Plot; $V_{IN} = 24\text{ V}$, $V_{OUT} = 5\text{ V}$, $f_{SW} = 500\text{ kHz}$, Load = 1 A, $f_{CO} = 37\text{ kHz}$, Phase Margin = 55°

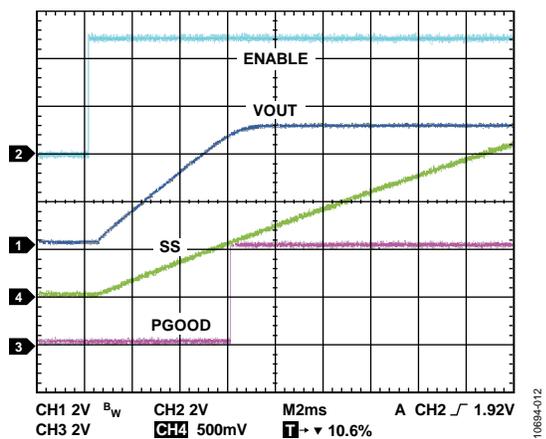


Figure 13. Startup; $V_{IN} = 24\text{ V}$, $V_{OUT} = 5\text{ V}$, Load $5\ \Omega$

EVALUATION BOARD SCHEMATICS AND ARTWORK

S10-16901

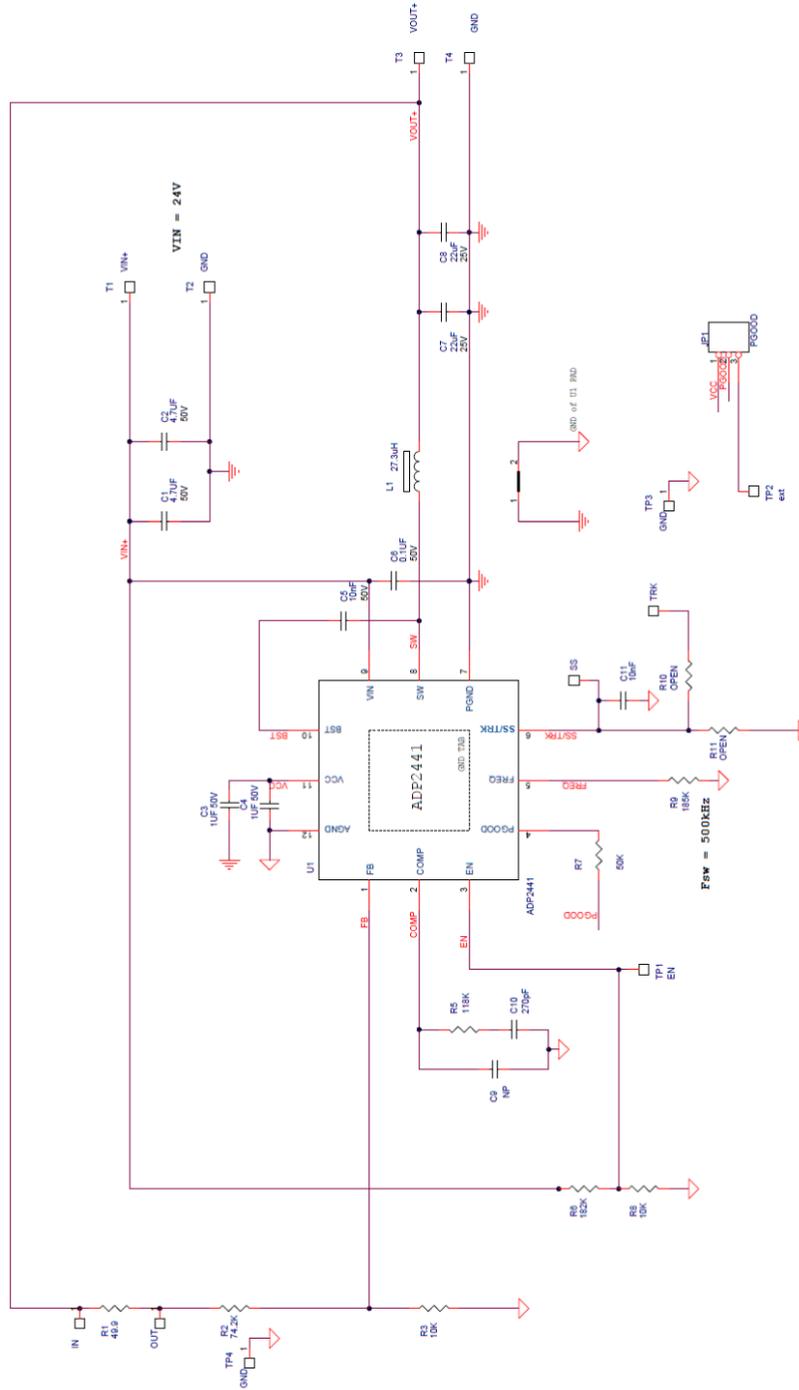


Figure 16.

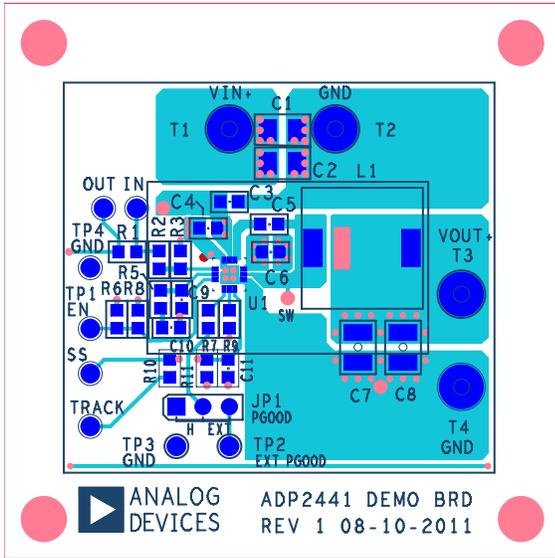


Figure 17. Top Layer

10694-016

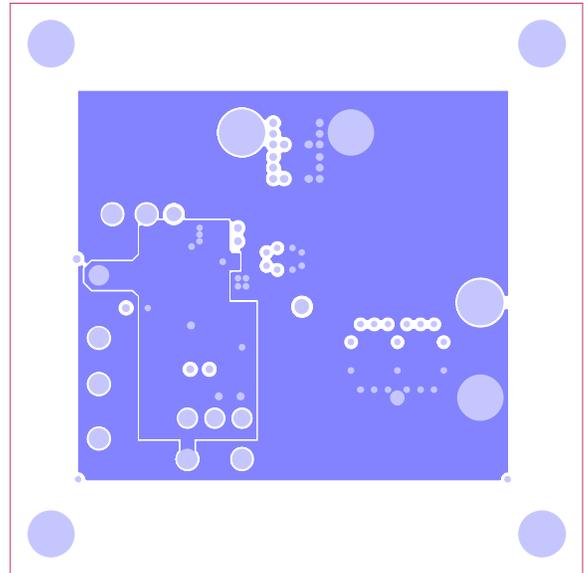


Figure 19. Second layer

10694-017

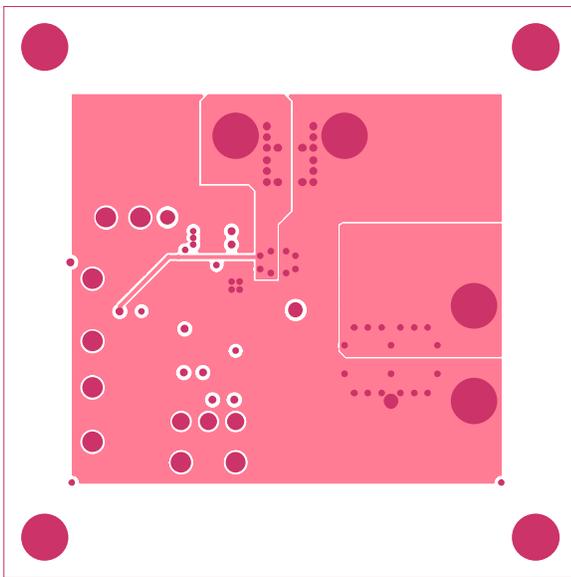


Figure 18. Third layer

10694-018

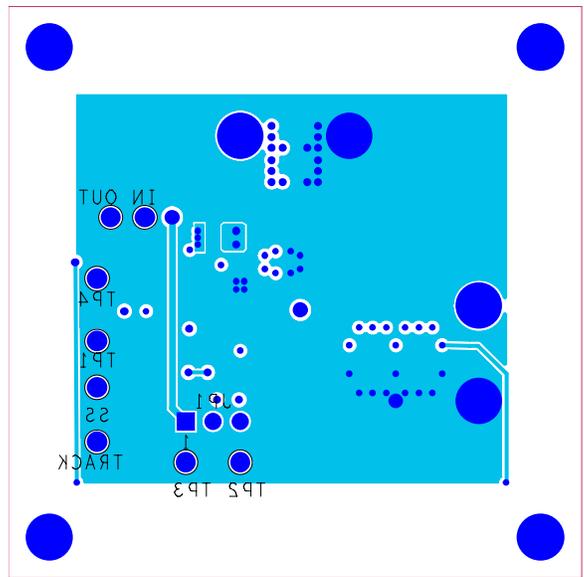


Figure 20. Bottom Layer

10694-019

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Manufacturer/Part Number
2	C1, C2	Capacitor MLCC, 4.7 μ F, 50 V, 1206, X7R	Murata GRM31CR71H475KA12L
2	C3, C4	Capacitor MLCC, 1 μ F, 25 V, 0603, X7R	Murata GRM188R71E105KA12D
1	C5	Capacitor, MLCC, 10 nF, 50 V, 0603, X7R	Murata GRM188R71H103KA01D
2	C7, C8	Capacitor, MLCC, 22 μ F, 25 V 1210, X7R	Murata GRM32ER71E226K
1	C11	Capacitor 10 nF, 50 V ceramic X7R	Panasonic ECJ-1VB1H103K
1	L1	MSS1038T-273	Coilcraft Coilcraft
1	C6	Capacitor MLCC, 0.1 μ F, 50 V, 0603, X7R	Murata GRM188R71H104KA93D
1	C10	Capacitor MLCC 270 pF, 50 V, 0603, X7R	Murata
1	R1	Resistor, 49.9 Ω , 1/10 W, 1% 0603 SMD	Determined by user
2	R3, R8	Resistor, 10 k Ω , 1/10 W, 1% 0603 SMD	Determined by user
1	R7	Resistor, 50 k Ω , 1/10 W, 1% 0603 SMD	Determined by user
1	R2	Resistor, 73.2 k Ω , 1/10 W, 1% 0603 SMD	Determined by user
1	R5	Resistor, 118 k Ω , 1/10 W, 1% 0603 SMD	Determined by user
1	R6	Resistor, 182 k Ω , 1/10 W, 1% 0603 SMD	Determined by user
1	R9	Resistor, 185 k Ω , 1/10 W, 1% 0603 SMD	Determined by user
1	R10	Resistor, 0 Ω , 1/10 W, 1% 0603 SMD	Determined by user
1	R11	Resistor, open, 1/10 W, 1% 0603 SMD	Determined by user
4	TRACK, SS, IN, OUT	Headers	Sullins PBC01SAAN
4	TP1, TP2, TP3, TP4	Headers	Sullins PBC01SAAN
1	JP1 PGOOD	Jumper	Sullins PBC03SAAN
4	T1, T2, T3, T4	Terminal, double turret, brass, 0.078"	Keystone 1502-1
1	U1	ADP2441	Analog Devices ADP2441

NOTES

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

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