HV9931 Unity Power Factor LED Lamp Driver

Features

- Constant output current
- Large step-down ratio
- Unity power factor
- Low input current harmonic distortion
- Fixed frequency or fixed off-time operation
- Internal 450V linear regulator
- Input and output current sensing
- Input current limit
- Enable, PWM and phase dimming

Applications

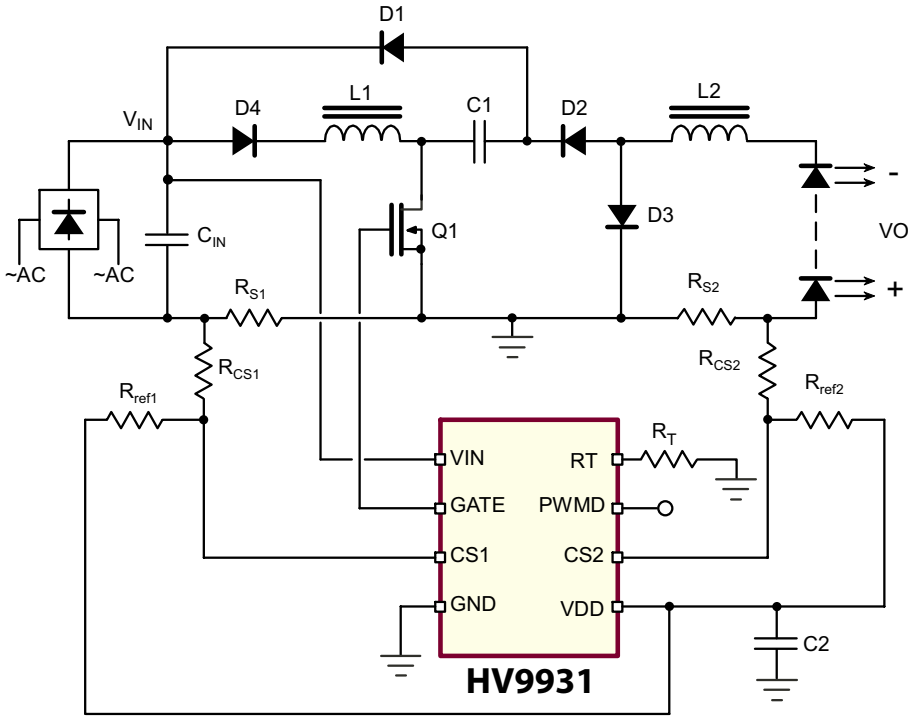
- Offline LED lamps and fixtures
- Street lamps
- Traffic signals
- Decorative lighting

General Description

The HV9931 is a fixed frequency PWM controller IC designed to control an LED lamp driver using a single-stage PFC buckboost-buck topology. It can achieve a unity power factor and a very high step-down ratio that enables driving a single high-brightness LED from the 85-264VAC input without a need for a power transformer. This topology allows reducing the filter capacitors and using non-electrolytic capacitors to improve reliability. The HV9931 uses open-loop peak current control to regulate both the input and the output current. This control technique eliminates a need for loop compensation, limits the input inrush current, and is inherently protected from input under-voltage condition.

Capacitive isolation protects the LED Lamp from failure of the switching MOSFET. HV9931 provides a low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to a few kilohertz. The PWM dimming capability enables HV9931 phase control solutions that can work with standard wall dimmers.

Typical Application Circuit



Ordering Information

Device	8-Lead SOIC (Narrow Body) *4.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*
HV9931	HV9931LG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

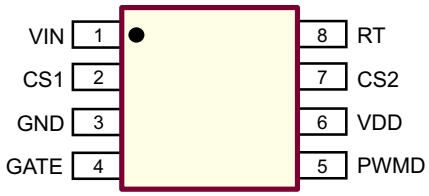
Parameter	Value
V_{IN} to GND	-0.5V to +470V
V_{DD} to GND	-0.3V to +13.5V
CS1, CS2, PWMD, GATE, RT to GND	-0.3V to (V_{DD} +0.3V)
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Continuous power dissipation (T_A = +25°C)	630mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

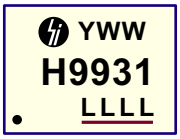
Package	θ_{ja}
8-Lead SOIC	128°C/W

Pin Configuration



8-Lead SOIC (LG)
(top view)

Product Marking



Y = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

8-Lead SOIC (LG)

Electrical Characteristics

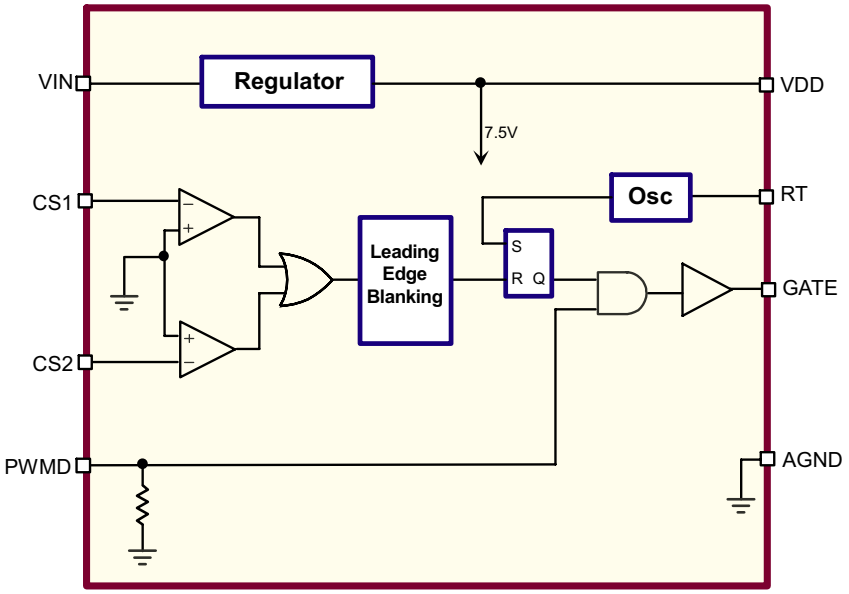
*(The * denotes the specifications which apply over the full operating junction temperature range of -40°C < T_A < +85°C, otherwise the specifications are at T_A = 25°C, V_{IN} = 12V, unless otherwise noted)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
Input						
V_{INDC}	Input DC supply voltage range*	8.0	-	450	V	DC input voltage
I_{INSD}	Shut-down mode supply current*	-	0.5	1.0	mA	PWMD connected to GND
Internal Regulator						
V_{DD}	Internally regulated voltage	7.12	7.50	7.88	V	V_{IN} = 8.0, $I_{DD(EXT)}$ = 0, GATE = 500pF, R_T = 226KΩ
$\Delta V_{DD,\ line}$	Line regulation of V_{DD}	0	-	1.0	V	V_{IN} = 8.0 - 450V, $I_{DD(ext)}$ = 0, GATE = 500pF, R_T = 226kΩ,
UVLO	V_{DD} undervoltage lockout threshold	6.45	6.70	6.95	V	V_{DD} rising
ΔUVLO	V_{DD} undervoltage lockout hysteresis	-	500	-	mV	---
PWM Dimming						
$V_{PWMD(lo)}$	PWMD input low voltage	-	-	1.0	V	V_{IN} = 8.0 - 450V
$V_{PWMD(hi)}$	PWMD input high voltage	2.4	-	-	V	V_{IN} = 8.0 - 450V
R_{PWMD}	PWMD pull-down resistance	50	100	150	kΩ	V_{PWMD} = 5.0V

Electrical Characteristics *(cont.)* *(The * denotes the specifications which apply over the full operating junction temperature range of -40°C < T_A < +85°C, otherwise the specifications are at T_A = 25°C, V_{IN} = 12V, unless otherwise noted)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
GATE						
$V_{GATE(hi)}$	GATE high output voltage*	V_{DD} -0.3	-	V_{DD}	V	I_{GATE} = 10mA, V_{DD} = 7.5V, V_{IN} open
$V_{GATE(lo)}$	GATE low output voltage*	0	-	0.3	V	I_{GATE} = -10mA, V_{DD} = 7.5V, V_{IN} open
T_{RISE}	GATE output rise time	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V, V_{IN} open
T_{FALL}	GATE output fall time	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V, V_{IN} open
T_{DELAY}	Delay from CS trip to GATE	-	150	300	ns	V_{CS1}, V_{CS2} = -100mV
T_{BLANK}	Blanking delay	150	215	280	ns	V_{CS1}, V_{CS2} = -100mV
Oscillator						
F_{OSC}	Oscillator frequency	80	100	120	kHz	R_T = 226KΩ
Comparators						
$V_{OFFSET1}$ $V_{OFFSET2}$	Comparator input offset voltage*	-15	-	15	mV	---

Functional Block Diagram



HV9931

Functional Description

Power Topology

The HV9931 is optimized to drive Supertex's proprietary single-stage, single-switch, non-isolated topology, cascading an input power factor correction (PFC) buck-boost stage and an output buck converter power stage. This power converter topology offers numerous advantages useful for driving high-brightness light emitting diodes (HB LED). These advantages include unity power factor, low harmonic distortion of the input AC line current, and low output current ripple. The output load is decoupled from the input voltage with a capacitor making the driver inherently failure-safe for the output load. The power converter topology also permits reducing the size of a filter capacitor needed, enabling use of non-electrolytic capacitors. The latter advantage greatly improves reliability of the overall solution.

The HV9931 is a peak current-mode controller that is specifically designed to drive a constant current buck-boost-buck power converter. This patent pending control scheme features two identical current sense comparators for detecting negative current signal levels. One of the comparators regulates the output LED current, while the other is used for sensing the input inductor current. The second comparator is mainly responsible for the converter start-up. The control scheme inherently features low inrush current and input under-voltage protection. The HV9931 can operate with programmable constant frequency or constant off-time. In many cases, the constant off-time operating mode is preferred, since it improves line regulation of the output current, reduces voltage stress of the power components and simplifies regulatory EMI compliance. (See Application Note AN-H52.)

Input Voltage Regulator

The HV9931 can be powered directly from its VIN pin, and takes a voltage from 8V to 450V. When a voltage is applied at the VIN pin, the HV9931 seeks to maintain a constant 7.5V at the VDD pin. The V_{DD} voltage can be also used as a reference for the current sense comparators. The regulator is equipped with an under-voltage protection circuit which shuts off the HV9931 when the voltage at the VDD pin falls below 6.2V.

The VDD pin must be bypassed by a low ESR capacitor (≥ 0.1µF) to provide a low impedance path for the high frequency current of the output GATE driver.

The HV9931 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator and the HV9931 will function by drawing power from the external voltage source connected to the VDD pin.

PWM Dimming and Wall Dimmer Compatibility

PWM Dimming can be achieved by applying a TTL-compatible square wave signal at the PWMD pin. When the PWMD pin is pulled high, the GATE driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the GATE driver is disabled and the external MOSFET turns off. The HV9931 is designed so that the signal at the PWMD pin inhibits the driver only, and the IC need not go through the entire start-up cycle each time ensuring a quick response time for the output current.

The power topology requires little filter capacitance at the output, since the output current of the buck stage is continuous, and since AC line filtering is accomplished through the middle capacitor rather than the output one. Therefore, disabling the HV9931 via its PWMD or VIN pins can interrupt the output LED current in accordance with the phase-controlled voltage waveform of a standard wall dimmer.

Oscillator

Connecting an external resistor from RT pin to GND programs switching frequency:

$$F_S\,[kHz] = \frac{25000}{R_T\,[K\Omega] + 22}$$

Connecting the resistor from the RT pin to the GATE programs constant off-time:

$$T_{OFF}\,[\mu s] = \frac{R_T\,[K\Omega] + 22}{25}$$

Input and Output Current Feedback

Two current sense comparators are included in the HV9931. Both comparators have their non-inverting inputs internally connected to ground (GND). The CS1 and CS2 inputs are inverting inputs of the comparators. Connecting a resistor divider into either of these inputs from a positive reference voltage and a negative current sense signal programs the current sense threshold of the comparator. The V_{DD} voltage of the HV9931 can be used as the reference voltage. If more accuracy is needed, an external reference voltage can be applied. When either the CS1 or the CS2 pin voltage falls below GND, the GATE pulse is terminated. A leading edge blanking delay of 215ns (typ) is added. The GATE voltage becomes high again upon receiving the next clock pulse of the oscillator circuit.

Referring to the Functional Circuit Diagram, the CS2 comparator is responsible for regulating output current. The output LED current can be programmed using the following equation:

$$R_{CS2} = \frac{Io + \frac{1}{2}\Delta I_{L2}}{7.5V} \cdot R_{REF2} \cdot R_{S2}$$

where ΔI_{L2} is the peak-to-peak current ripple in L2. The CS1 comparator limits the current in the input inductor L1. There is no charge in the capacitor C1 upon the start-up of the converter. Therefore, L2 cannot develop the output current, and the HV9931 starts-up in the input current limiting mode. The CS1 current threshold must be programmed such that no input current limiting occurs in normal steady-state operation. The CS1 threshold can be programmed in accordance with a similar equation:

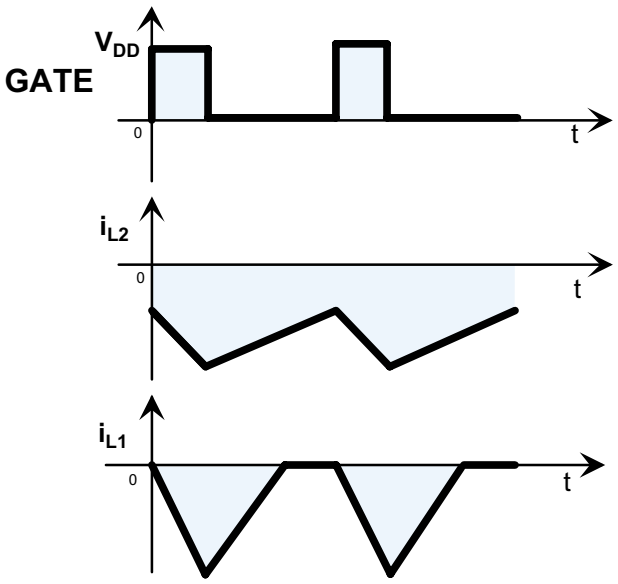
$$R_{CS1} = \frac{I_{L1(PK)}}{7.5V} \cdot R_{REF1} \cdot R_{S1}$$

where $I_{L1(PK)}$ is the maximum peak current in L1.

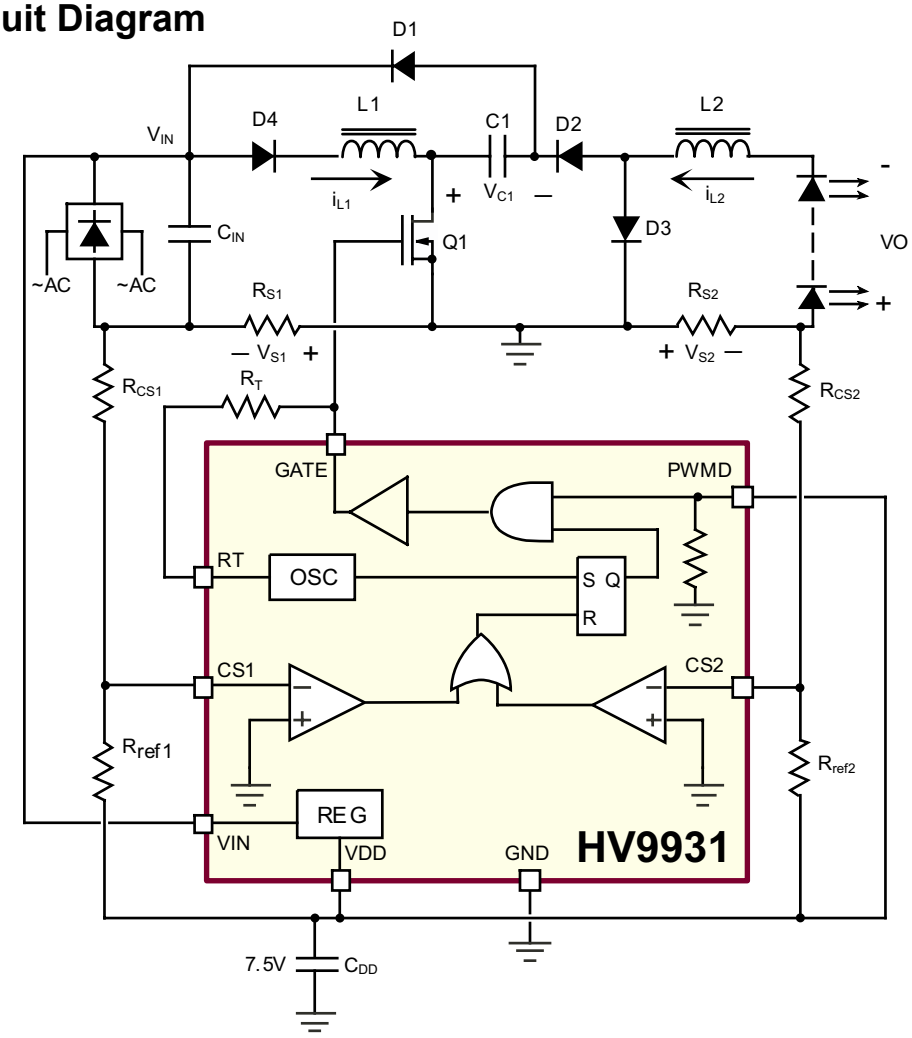
MOSFET Gate Driver

Typically, the GATE driving capability of the HV9931 is limited by the amount of power dissipation in its linear regulator. Thus, care must be taken selecting a switching MOSFET to be used in the circuit. An optimal trade-off must be found between the GATE charge and the on-resistance of the MOSFET to minimize the input regulator current.

Switching Waveform



Functional Circuit Diagram

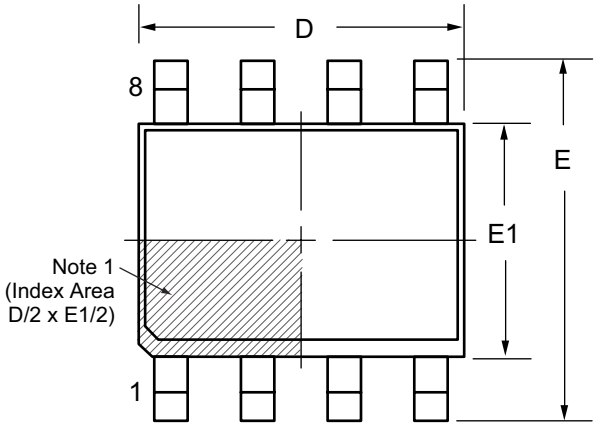


Pin Description

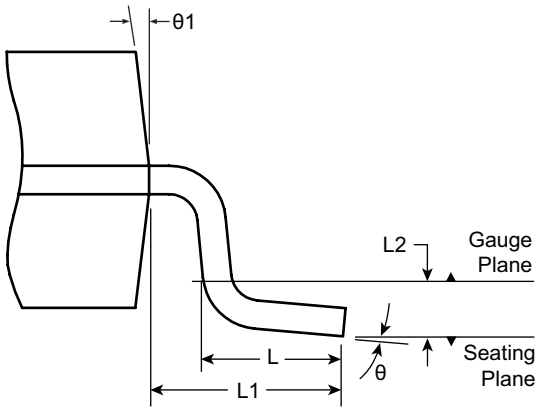
Pin #	Pin Name	Description
1	VIN	This pin is the input of a high voltage regulator.
2	CS1	This pin is used to sense the input and output currents of the converter. It is the inverting input of the internal comparator.
3	GND	Ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train.
4	GATE	This pin is the output GATE driver for an external N-channel power MOSFET.
5	PWMD	When this pin is pulled to GND, switching of the HV9931 is disabled. When the PWMD pin is released, or external TTL high level is applied to it, switching will resume. This feature is provided for applications that require PWM dimming of the LED lamp.
6	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND.
7	CS2	This pin is used to sense the input and output currents of the converter. It is the inverting input of the internal comparator.
8	RT	Oscillator control. A resistor connected between this pin and GND sets the PWM frequency. A resistor connected between this pin and GATE sets the PWM off-time.

8-Lead SOIC (Narrow Body) Package Outline (LG)

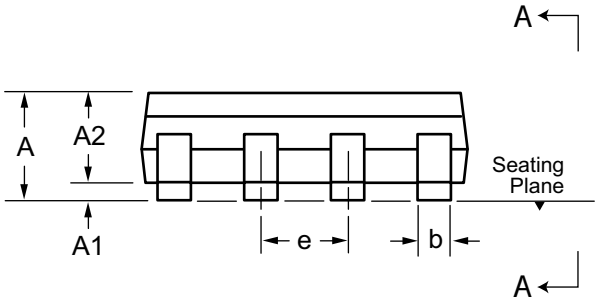
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



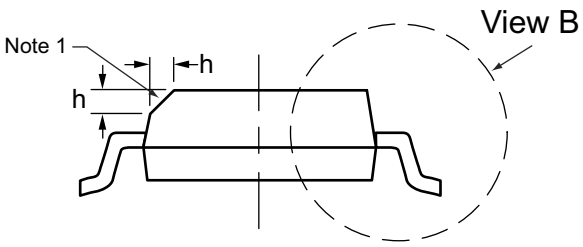
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

Drawings are not to scale.

***Supertex Doc. #:** DSPD-8SOLGTG, Version H101708.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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