3 Volt Intel® Advanced Boot Block Flash Memory 28F004/400/008/800/ 016/160/320/640B3 (x8/x16)

Specification Update

April 2002

Notice: The 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3 may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 297948-012

Contents

Revision History

Date	Version	Description
06/02/98	-001	Document includes all known specifications to date (original version).
07/09/98	-002	Added specification change for µBGA* package pinout
08/10/98	-003	Added Errata for Program and Erase Failure when V_{PP} = 12 V and V_{CCQ} = 1.65 V – 2.5 V Added Errata for Maximum I_{CCD} Change
10/02/98	-004	This document references 290580-006 Removed Valid Ordering Information Combinations Change for 32-Mbit Densities (fixed in 290580-006) Removed µBGA* Package Pinout Change (fixed in 290580-006) Removed µBGA* Package Mark Clarification (fixed in 290580-006) Removed I_{PPD} Test Condition Clarification (fixed in 290580-006) Name changed from *Smart 3 Advanced Boot Block Flash Memory Family*
12/01/98	-005	Erratum #1 fixed in A-1 Stepping
02/16/99	-006	Specification Update title modified—added part numbers for clarity
02/03/99	-007	Merged existing document with 28F160B3 specification update document (297835-004). Added 32-Mb Maximum V_{CC} Change specification change.
10/05/00	-008	Renamed Specification Change #1, *32-Mb Maximum V_{CC} Change*, to *0.25µm 32-Mb V_{CC} Change,* and modified it to indicate that the affected product is the 32-Mb product on the 0.25µm process
05/03/01	-009	Added Erratum #6, *28F320B3TC Block Locking Failure* Added Erratum #7, *28F320B3xC Reset Failure*
07/20/01	-010	Updated Erratum #7, *28F320B3xC Reset Failure,* added 3.3v V_{CC} max
11/05/01	-011	Added Erratum #8, *28F640C3xC* for Maximum I_{CCD} / I_{CCS} Change
3/21/02	-012	Added Erratum #9, 28F160B3xC Erase Resume Issue

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
3 Volt Intel® Advanced Boot Block Flash Memory, 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3 Datasheet	290580-011

Nomenclature

Errata are design defects or errors. These may cause the behavior of the 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3 to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 28F004/400B3, 28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	This erratum exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping, or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings					Page	Status	Errata
	0.4 micron A-0	0.4 micron A-1	0.25 micron A–0	0.25 micron A–2	0.18 micron A-0, A-2, A-3			
1	X	X				10	Fixed	Block Locking during Write Operations if CE# is Toggled High
2	X	X				11	Fixed	Invalid Read Durations for CE# High Pulse Width
3	X	X				11	Fixed	Temperature Effect on V_{CC} Ramp
4				X		12	Fixed	Program and Erase Failure When V_{PP} = 12 V and V_{CCQ} = 1.65 V – 2.5 V
5						12	Doc	Maximum I_{CCD} Change
6					X	13	Fix	28F320B3TC Block Locking Failure
7					X	14	Fix	28F320B3xC Reset Failure
8					X	11	Fix	28F640C3xC Maximum ICCS and ICCD Change
9					X	12	Fix	28F160B3xC Erase Resume Issue

Specification Changes

Number	Page	Specification Changes
1	18	0.25µm 32-Mb Maximum V_{CC} Change

Specification Clarifications

Number	Steppings	Page	Specification Clarifications
	A–0		
N/A		18	None in this specification update revision

Documentation Changes

Number	Document Revision	Page	Documentation Changes
N/A		18	None in this specification update revision

Identification Information

Markings

The Finished Processing Order (FPO) number correlates to a specific device stepping as illustrated in the table below:

Stepping[1]	Identifier
0.4 micron A stepping	Ninth digit on topside FPO mark (third line) = J, K, L, M, or N.

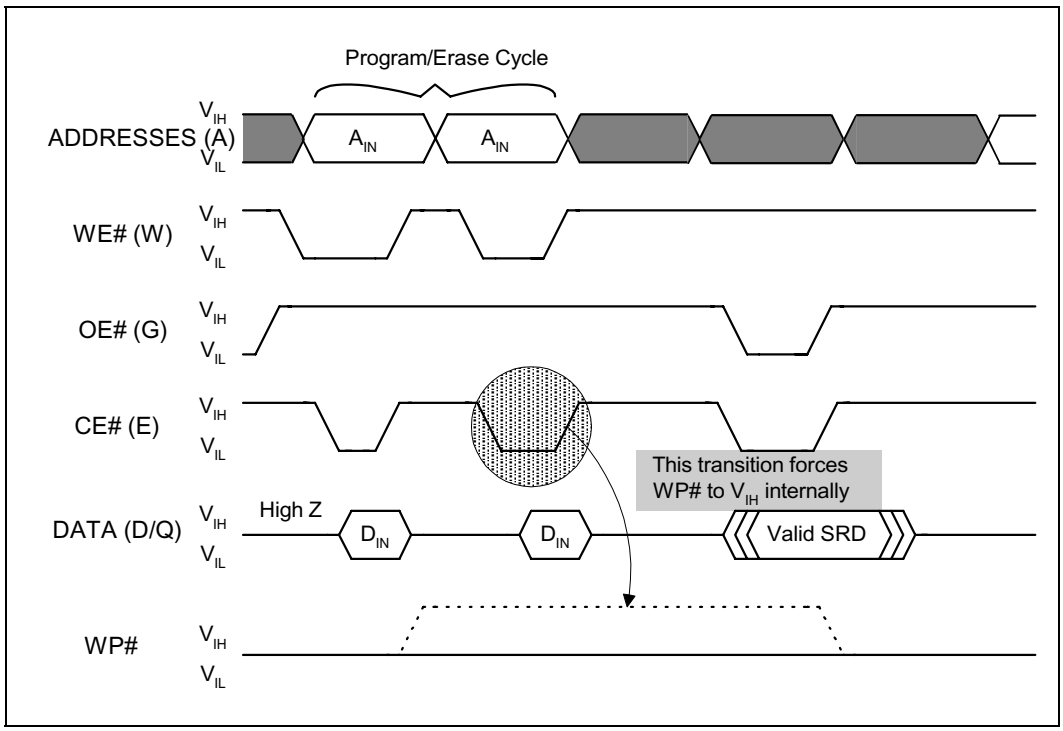
NOTE:
1. Device steppings are based on continuous improvements made in manufacturing and testing of the device and represent the current material shipped.

Errata

1. Block Locking during Write Operations If CE# Is Toggled High

Problem: In normal operation, WP# = V_{IL} locks the upper two (or lower two, in the case of a bottom boot device) parameter blocks. If a program or erase command is issued to a locked block, the WSM sets the program or erase status bit and the block lock status bit to "1" and prevents the program or erase operation to the locked block.

However, initial samples of the 28F160B3 flash memory device ignore the WP# pin if CE# is toggled high during the second cycle of a program or erase operation. Any program and/or erase commands issued to locked blocks **may change** memory contents even if WP# = V_{IL} (assuming $V_{PP} > V_{PPLK}$).



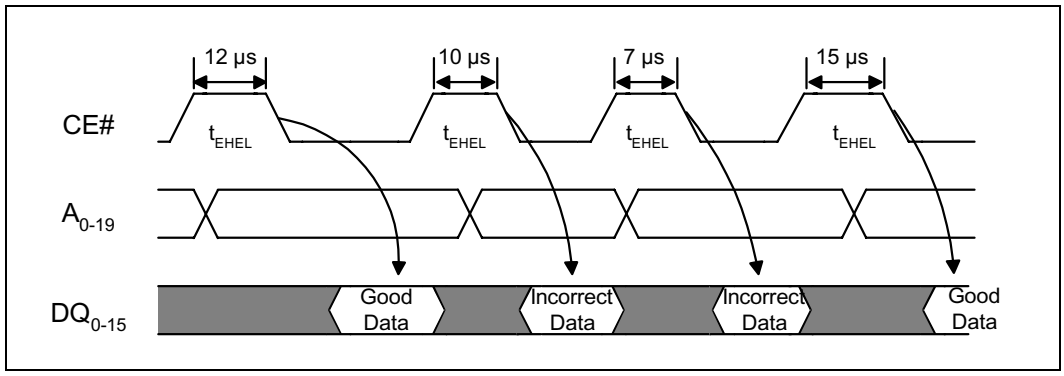
Implication: This erratum causes the lockable blocks to be unlocked regardless of the state of WP# when CE# is toggled high during the write cycle(s).

Workaround: Applications using A-0 material should hold CE# low and toggle WE# to latch command, address, and data during a program or erase operation.

Only 28F160B3 A-0 stepping (0.4 µm material) is affected by this erratum. This erratum has been fixed in the A-1 stepping. Refer to *Summary Table of Changes* to determine the affected stepping(s).

2. Invalid Read Durations for CE# High Pulse Width

Problem: During consecutive read operations, CE# may be left low or toggled as desired. If CE# is toggled high (see diagram below) for 4 µs–11 µs between read operations, subsequent reads will return incorrect data.



Implication: If CE# is not toggled between consecutive reads, there is no impact. Any application that toggles CE# between read operations will be affected if the CE# high pulse width is within the nonfunctional range, i.e., 4 µs ≤ t_{EHEL} ≤ 11 µs.

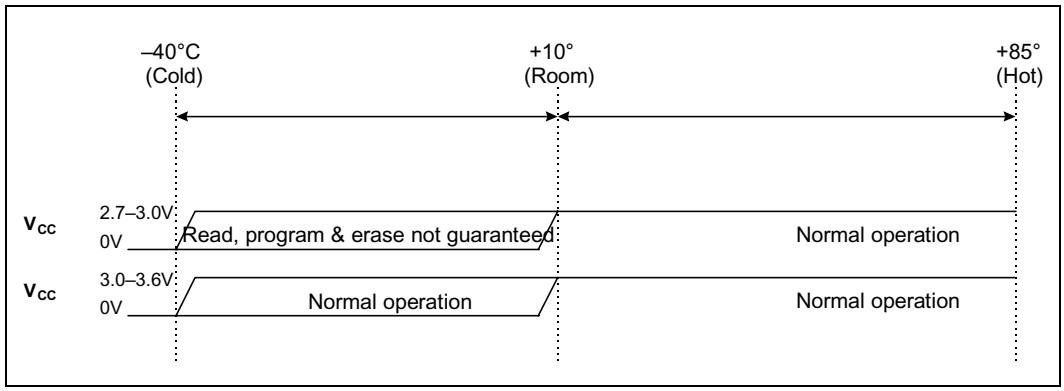
Workaround: Either of the following actions will prevent this erratum:

1. Do not toggle CE# between consecutive read operations
2. Insure t_{EHEL} is less than 4 ms or greater than 11 µs

Status: Only 28F160B3 A-0 stepping (0.4 µm material) is affected by this erratum. This erratum has been fixed in the A-1 stepping. Refer to *Summary Table of Changes* to determine the affected stepping(s).

3. Temperature Effect on V_{CC} Ramp

Problem: The 28F160B3 flash memory operates from 2.7 V–3.6 V across the full extended temperature range (–40 °C to +85 °C). For a limited number of 28F160B3 engineering samples, when ramping V_{CC} to below 3.0 V and below +10 °C (–40 °C to +10 °C), the device is not guaranteed to respond to read, program, and erase operations (see diagram below). If V_{CC} ramps to a value between 3.0 V and 3.6 V, the device functions normally across the entire extended temperature range.



Implication: If V_{CC} is ramped to [and maintained at] a level below 3 V between –40 °C and +10 °C, the device may not function properly.

Workaround: Either of the following actions will prevent this erratum:

1. Ramp V_{CC} above 3.0 V in order to trip the V_{CC} detector; once the detector has "tripped," the voltage may be lowered below 3.0 V for normal operation
2. Only ramp V_{CC} at temperatures above +10 °C.

Status: Only engineering samples of 28F160B3 A-0 stepping (0.4 µm material) from lot 7705998FOB and 7705999FOB [backside mark] are affected. This erratum affects all A-0 µBGA* package engineering samples. Only A-0 TSOP samples with a printed backside mark are affected. If the TSOP package has no backside mark then it is **not** affected. This erratum has been fixed in the A-1 stepping.

4. Program and Erase Failure When V_{PP} = 12 V and V_{CCQ} = 1.65 V - 2.5 V

Problem: During production programming (V_{PP} = 12 V) with V_{CCQ} between 1.65 V and 2.5 V, the device will fail to program or erase.

Implication: Customers should not implement 12 V production programming with V_{CCQ} between 1.65 V and 2.5 V. This may be corrected on future steppings.

Status: Refer to the *Summary Tables of Changes* to determine the affected stepping(s).

5. Maximum I_{CCD} Change

Problem: The maximum I_{CCD} increases from 20 µA to 25 µA. The following in the revised I_{CCD} specification:

Sym	Parameter	V_{CC}	2.7 V–3.6 V		2.7 V–2.85 V		2.7 V–3.3 V		Unit	Test Conditions
		V_{CCQ}	2.7 V–3.6 V		1.65 V–2.5 V		1.8 V–2.5 V			
		Note	Typ	Max	Typ	Max	Typ	Max		
I_{CCD}	V_{CC} Power-Down Current	6	7	25	7	25	7	25	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or GND RP# = GND ± 0.2 V

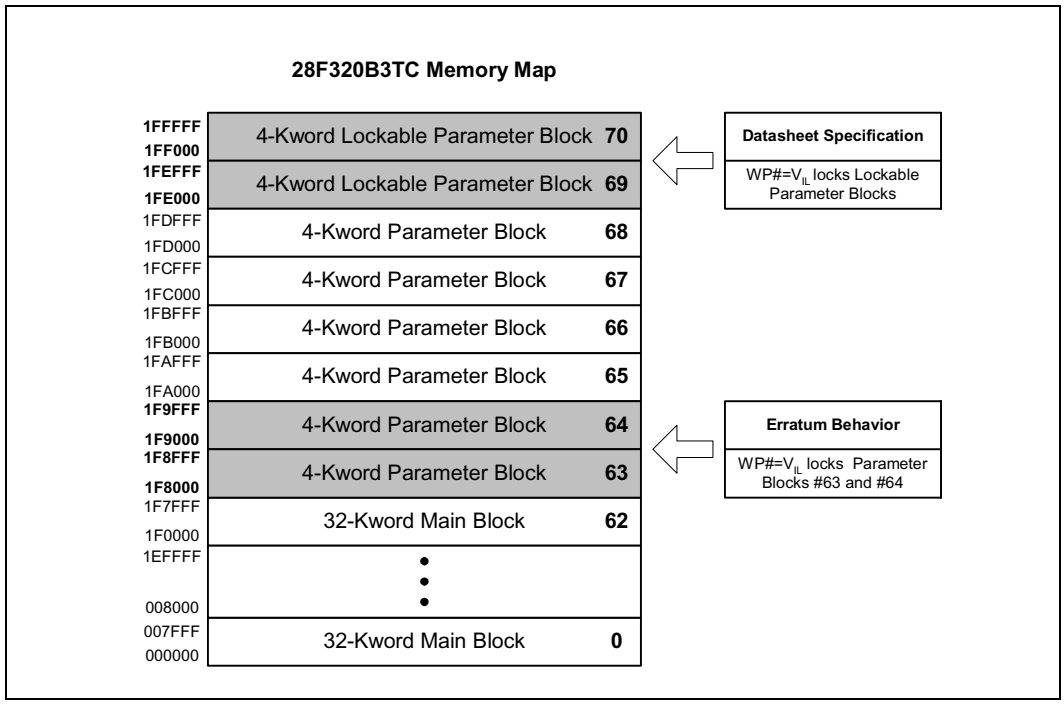
NOTE: Since each column lists specifications for a different V_{CC} and V_{CCQ} voltage range combination, the test conditions V_{CC} Max, V_{CCQ} Max, V_{CC} Min, and V_{CCQ} Min refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column.

Implication: The maximum I_{CCD} is specified under worst case conditions only (V_{CC} = 3.6 V, temperature = +85 °C). The typical I_{CCD} specification should be used to determine I_{CCD} current draw under typical conditions (V_{CC} = 3.3 V, temperature = +25 °C). The typical I_{CCD} specification has not changed.

Status: Refer to the *Summary Tables of Changes* to determine the affected stepping(s)

6. 28F320B3TC Block Locking Failure

Problem: For the 0.18µm 32 M-bit top boot devices affected by this erratum, block locking functionality deviates from the datasheet specification. WP#=V_{IL} protects blocks #63 and #64, instead of blocks #69 and #70).



Implication: There are two implications to this erratum:

1) The two Lockable Parameter Blocks (blocks #69 and #70) are not protected when WP#=V_{IL}; and

2) When WP#=V_{IL}, blocks #63 and #64 will be locked, and any attempts to program or erase these two blocks may fail.

Workaround: There are two workarounds for this erratum:

1) Set WP#=V_{IH} when programming or erasing blocks #63 and #64. In addition, hold $V_{PP} \leq V_{PPLK}$ when not programming or erasing for additional protection against accidental writes; and

2) Temporarily, have software swap the contents of blocks #63 and #64 with the contents of blocks #69 and #70. If code was originally in blocks #69 and #70, utilize jump routine to blocks #63 and #64.

Status: This erratum affects all 0.18µm 28F320B3 top boot devices. A fix has been identified for this erratum and is intended to be implemented in a future microcode revision.

7. 28F320B3xC Reset Failure

Problem: The 0.18µm 28F320B3xC devices can unintentionally reset under certain conditions where V_{PP} toggles.

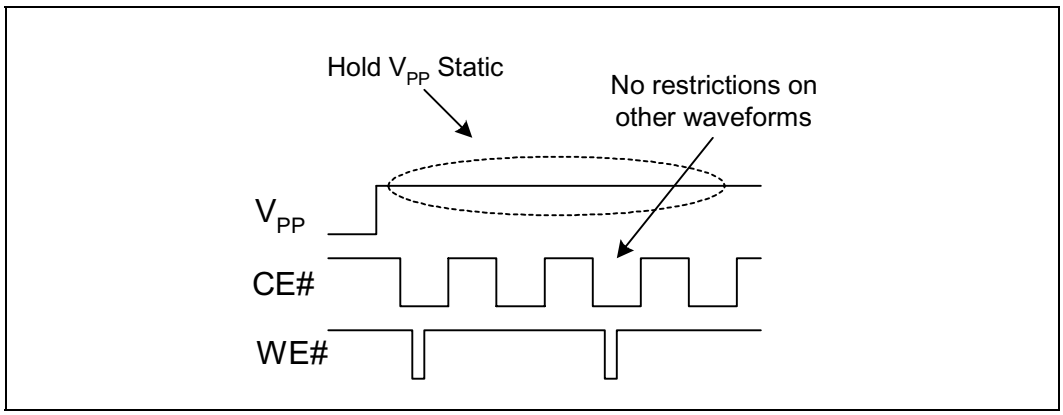
Implication: When the reset occurs, any command being executed is interrupted and the flash switches to read array mode.

Workaround: There are four workarounds for this erratum:

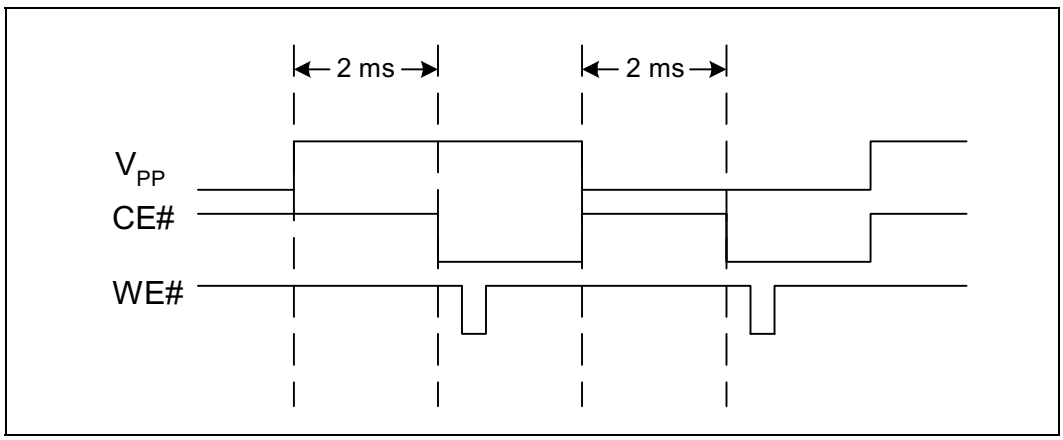
1) Tie V_{PP} to V_{CC}

2) If the third and forth digits on the top side FPO mark (third line) are equal or greater than “23”, then V_{CC} may be set from 2.7 V to 3.3 V. V_{CC} must not exceed 3.3 V.

3) Set V_{PP} to a static high or static low level as shown here; and



4) Wait 2 ms after a V_{PP} transition to access the flash device as shown here.



Note: This erratum affects all 0.18µm 28F320B3 devices. Root cause has been identified and fixes are being evaluated.

8. 28F640B3xC Maximum I_{CCS} and I_{CCD} Change

Problem: On the 0.18µm 28F640B3xC device, the maximum I_{CCS} and I_{CCD} deviates from the published specification and increases from 15 µA to 20 µA. The following table shows the revised I_{CCS} and I_{CCD} specifications.

Sym	Parameter	V_{CC}	2.7 V –3.6 V		Unit	Test Conditions
		V_{CCQ}	2.7 V –3.6 V			
		Note	Type	Max		
I_{CCS}	V_{CC} Standby Current	1,2	7	20	µA	V_{CC} = V_{CC}Max CE# = RP# = V_{CCQ} or during Program/ Erase Suspend WP# = V_{CCQ} or GND
I_{CCD}	V_{CC} Deep Power-Down Current	1,2	7	20	µA	V_{CC} = V_{CC}Max V_{CCQ} = V_{CCQ}Max V_{IN} = V_{CCQ} or GND RP# = GND ± 0.2 V

NOTE:
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25 °C.
2. The test conditions V_{CC}Max, V_{CCQ}Max, V_{CC}Min, and V_{CCQ}Min refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column.

9. 28F160B3xC Erase Resume Issue

Problem: On the 0.18µm 28F160B3xC device, a design anomaly was discovered. During an Erase-Suspend operation, if the Program (40H/10H) sequence is executed, under limited conditions the proceeding Erase Resume command (D0H) may not actually resume the device. No customers have reported failures in product applications. Customers who use any version of FDI (Intel Flash Data Integrator) software will not see this issue. If the Read Array command is issued prior to the Erase Resume command, users will not see the issue (typical in XIP applications).

Implication: The Resume Command (D0H) may be ignored by the device and will not correctly resume. The device will appear to remain in suspend (via status register). After a reset of the flash device the status register will clear. This failure has been recreated in a lab environment only.

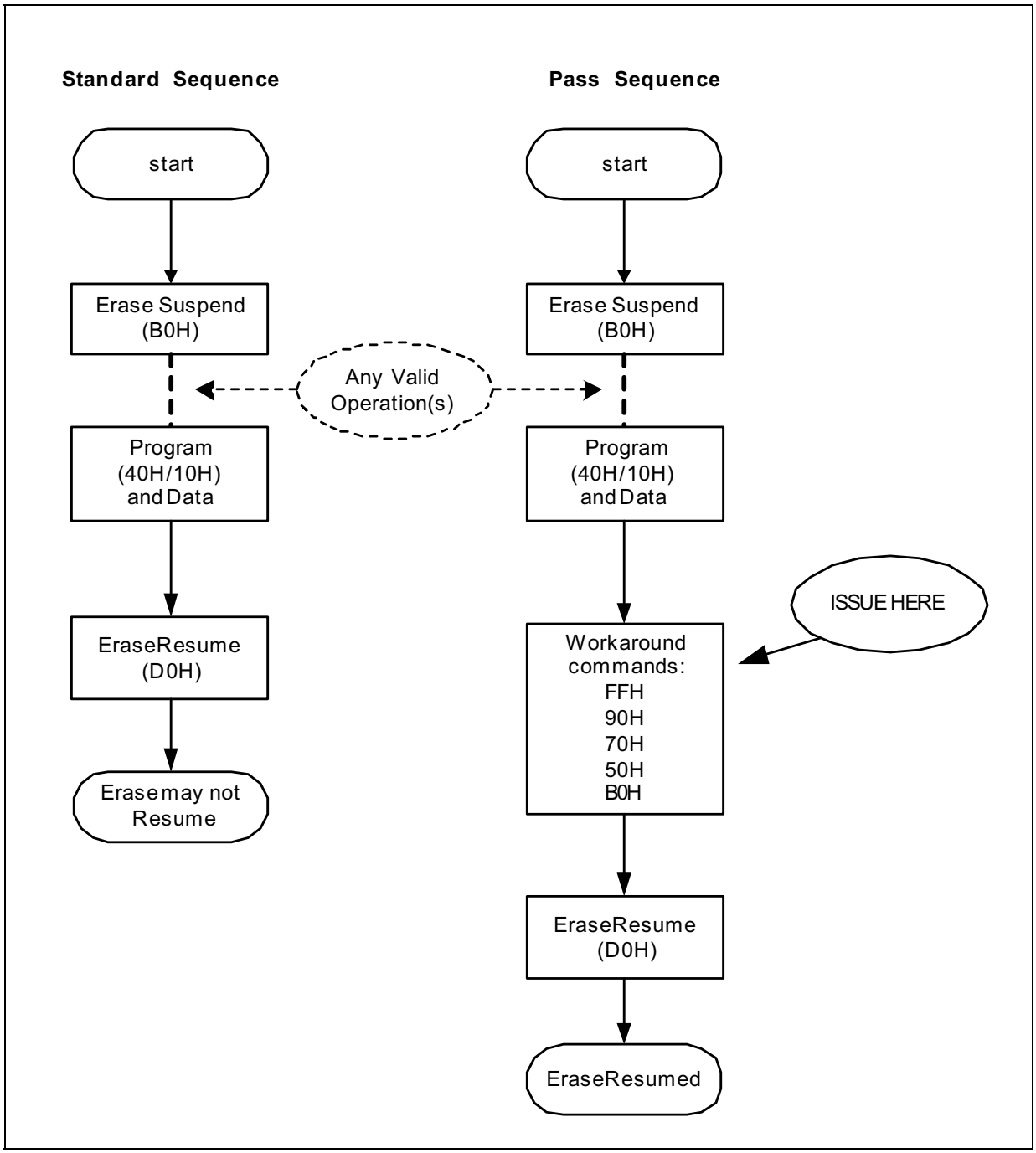
Workaround: There are 2 workarounds for this erratum.

1. If FDI (Intel Flash Data Integrator) software is used, users will not see the issue.
2. During an Erase-Suspend (B0H), user must issue any of the following commands listed in Table-1 after issuing the Program (40H/10H) and data sequence but before issuing the Erase-Resume (D0H) command.

Command	First Bus Cycle			Second Bus Cycle	
	Oper	Addr	Data	Oper	Addr
Read Array	Write	X	FFH		
Read Identifier	Write	X	90H	Read	IA
Read Status Register	Write	X	70H	Read	X
Clear Status Register	Write	X	50H		
Program/Erase Suspend	Write	X	B0H		

NOTES:
IA: Identifier Address **X:** Don't Care

Figure 1. Workaround Placment



Status: Root cause has been identified. New material will be available in August 2002.

Specification Changes

1. 0.25µm 32-Mb Maximum V_{CC} Change

Issue: The maximum V_{CC} decreases from 3.6 V to 3.3 V on 0.25µm 32-Mb versions only. The following table shows the revised V_{CC} specification.

Symbol	Parameter	Notes	Min	Max	Units
V_{CC}	V_{CC} Supply Voltage	1	2.7	3.3	Volts

Other implied specification changes, as a result of the V_{CC} change, are described in the following table:

Symbol	Parameter	Notes	Min	Max	Units
V_{CC1}	V_{CC} Supply Voltage	1	2.7	3.3	Volts
V_{CC2}	V_{CC} Supply Voltage	1	3.0	3.3	Volts
V_{CCQ1}	I/O Supply Voltage	1	2.7	3.3	Volts
V_{PP1}	Supply Voltage	1	1.65	3.3	Volts

NOTE: 1. V_{CC} and V_{CCQ} must share the same the same supply when they are in the V_{CC1} range.

The maximum V_{CC} has changed on the 0.25µm 32-Mb devices. The maximum V_{CC} specification has not changed on the 16-Mb, 8-Mb, or devices on the 0.18µm process. This may become an issue if the system voltage regulator used has a V_{CC} range tolerance that is outside the new specification, which may cause the device to operate in a condition which is outside the specifications of the current datasheet.

Specification Clarifications

There are no specification clarifications in this Specification Update revision.

Documentation Changes

There are no documentation changes in this Specification Update revision.