AS3833

6 Channel High-Precision LED Controller for LCD Backlight with Integrated Step-Up Controller

General Description

The AS3833 is a 6 channel high precision LED controller with PWM input for driving external bipolar transistors in LCD-backlight or various other general lighting applications.

The integrated step-up controller provides the necessary output voltage for the LED string supply.

The SMPS feedback control optimizes the power efficiency by adjusting the LED string supply voltage.

Built in safety features include undervoltage and thermal shutdown as well as open and short LED detection.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3833, 6 Channel High-Precision LED Controller for LCD Backlight with Integrated Step-Up Controller are listed below:

Figure 1:
Added Value of Using AS3833

Benefits	Features
• Easy integration	• 1 PWM input for dimming, no software needed.
• Highest brightness uniformity	• Absolute LED current accuracy of ± 0.8% and channel to channel matching of ± 0.6%
• Innovative BJT temperature supervision	• On chip temperature supervision of external bipolar transistor with programmable threshold.
• Low BOM	• Due to integrated DC/DC step up controller
• On chip safety features and automatic fault handling	• Short/OPEN LED detection, temperature shutdown, undervoltage shutdown, overvoltage protection
• Single sided PCB support	• SOIC-28 package can be routed on a single sided PCB saving system cost, TQFP-32 available for double sided PCB

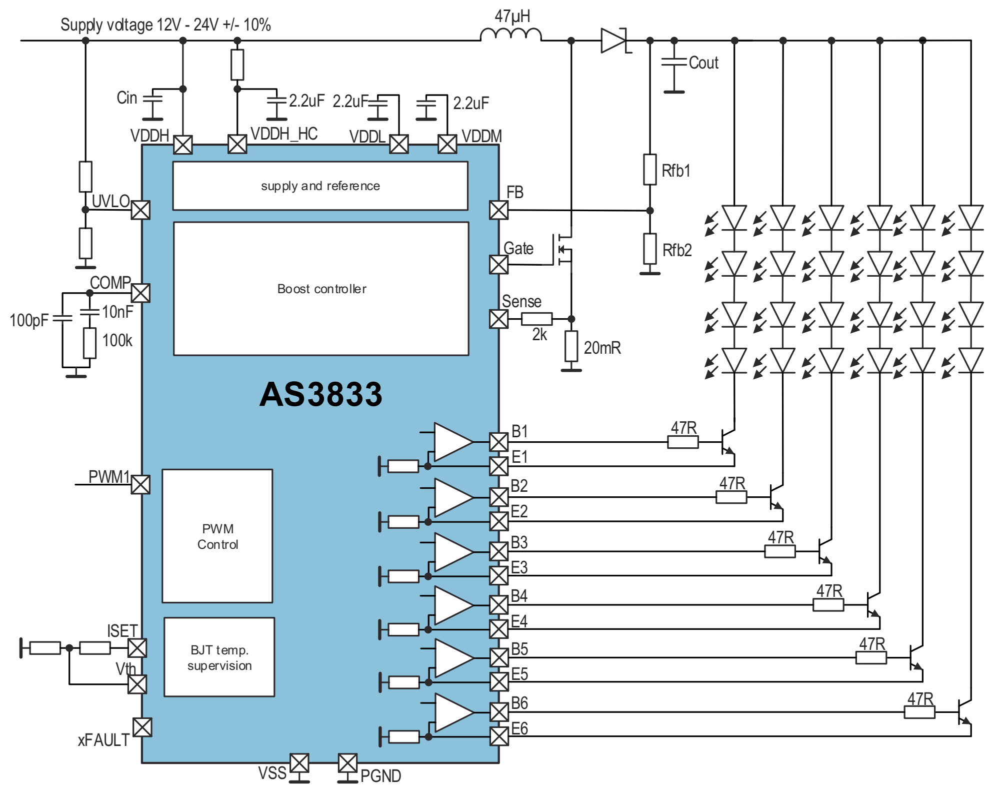
Applications

AS3833 is suitable for LED backlighting used in LCD TV sets, monitors and various other general lighting applications.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS3833 Block Diagram



Pin Assignment

Figure 3:
Pin Assignment of AS3833 (Top View)

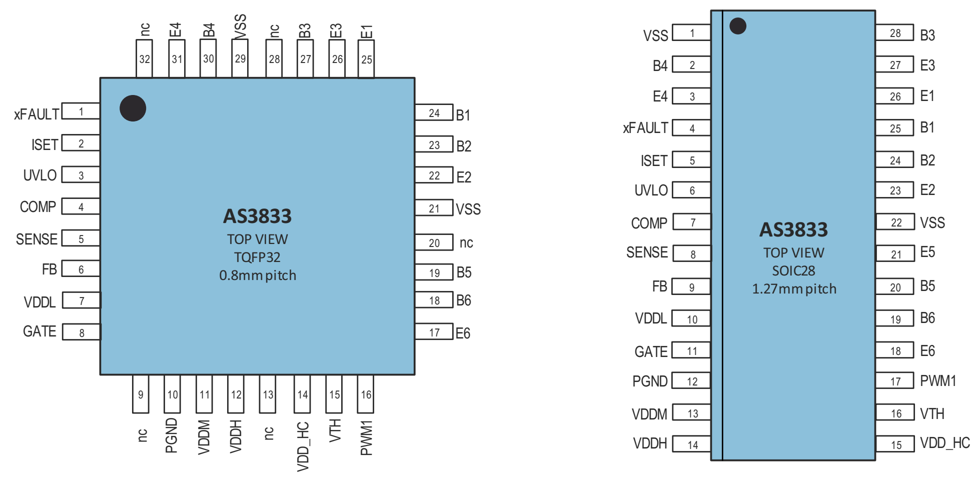


Figure 4:
Pin Description

Pin Number TQFP-32	Pin Number SOIC-28	Pin Name	Pin Type	Description
29	1	VSS	P	**Analog ground**
30	2	B4	A_I/O	**Base 4**. Connect to base of external transistor
31	3	E4	A_I/O	**Emitter 4**. Connect to emitter of external transistor
1	4	xFAULT	DO_OD	**Fault output**. Active low
2	5	ISET	A_I/O	**Current setting**. Connect current setting resistor
3	6	UVLO	A_I/O	**Undervoltage lockout input**
4	7	COMP	A_I/O	**Compensation network**. Connect compensation network.
5	8	SENSE	A_I/O	**Current sense input**. Provide a short, direct PCB path between this pin and the positive side of the current sense resistor.
6	9	FB	A_I/O	**Output voltage feedback input**. Input for voltage divider. Connect voltage divider output as short as possible to this pin
7	10	VDDL	A_I/O	**Voltage regulator output 3.3V.** Connect 2.2µF decoupling capacitor to GND

Pin Number TQFP-32	Pin Number SOIC-28	Pin Name	Pin Type	Description
8	11	GATE	A_I/O	**Gate driver output**
10	12	PGND	P	**Power ground**
11	13	VDDM	P	**Voltage regulator output.** Connect 2.2µF decoupling capacitor to GND
12	14	VDDH	P	**Supply voltage**. Connect 1µF decoupling capacitor to GND
14	15	VDDH_HC	P	**Voltage regulator Input**. Connect 2.2µF decoupling capacitor to GND
15	16	VTH	A_I/O	**Reference input for overtemperature detection**
16	17	PWM1	DI_PD	**PWM input 1**. PWM input for channel 1
17	18	E6	A_I/O	**Emitter 6**. Connect to emitter of external transistor
18	19	B6	A_I/O	**Base 6**. Connect to base of external transistor
19	20	B5	A_I/O	**Base 5**. Connect to base of external transistor
20	21	E5	A_I/O	**Emitter 5**. Connect to emitter of external transistor
21	22	VSS	P	**Analog ground**
22	23	E2	A_I/O	**Emitter 2**. Connect to emitter of external transistor
23	24	B2	A_I/O	**Base 2**. Connect to base of external transistor
24	25	B1	A_I/O	**Base 1**. Connect to base of external transistor
25	26	E1	A_I/O	**Emitter 1**. Connect to emitter of external transistor
26	27	E3	A_I/O	**Emitter 3**. Connect to emitter of external transistor
27	28	B3	A_I/O	**Base 3**. Connect to base of external transistor

A_I/O	Analog pin
P	Power pin
DO	Digital output
DO_OD	Digital output open drain
DI	Digital input
DI_PU	Digital input with pullup resistor
DI_PD	Digital input with pull down resistor

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VDDH to VSS, VDDH_HC to VSS	-0.3	55	V	
VDDM to VSS, GATE to VSS	-0.3	25	V	
xFAULT to VSS	-0.3	7	V	
VDDL to VSS	-0.3	5	V	
Analog Pin Voltage to VSS (1)	-0.3	5	V	
Digital Pin Voltage to VSS(2)	-0.3	5	V	
Input Current (latch-up immunity)	-100	100	mA	JEDEC 78
Electrostatic Discharge				
Electrostatic Discharge HBM	± 1500		V	MIL 883 E method 3015
Electrostatic Discharge MM	± 200		V	JESD22-A115C
Continuos Power Dissipation (T_A = 70°C)				
Continuous Power Dissipation		1.5	W	P_T (3) for SOIC-28 Package
Continuous Power Dissipation Derating Factor		13	mW / °C	P_{DERATE} (4)

Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions				
Junction to ambient thermal resistance		76	ºC/W	SOIC-28 Package. For more information about thermal metrics, see application note *AN01 Thermal Characteristics.*
Junction Temperature (T_{Jmax})		150	ºC	
Storage Temperature Range	-55	150	ºC	
Package Body Temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Relative Humidity (non-condensing)	5	85	%	
Moisture Sensitivity Level	3			Maximum floor life time of 168h

Note(s):

1. Pins Vth, UVLO, Comp, Sense, FB, Iset, Ex, Bx.
2. Pins PWMx.
3. Depending on actual PCB layout and PCB used.
4. P_{DERATE} derating factor changes the total continuous power dissipation (P_T) if the ambient temperature is not 25ºC. Therefore for e.g. T_A=85ºC calculate P_T at 85ºC = P_T - P_{DERATE} x (85ºC - 25ºC)

Electrical Characteristics

VDDH = 24V, all voltages referenced to VSS, Typical values are at T_A = 25°C (unless otherwise specified). All limits are guaranteed. The parameters with min. and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		General				
T_A	Operating Temperature Range	Apply proper cooling to stay below maximum allowed T_J.	-20		85	°C
T_J	Operating Junction Temperature		-20		115	°C
		Power Supply				
VDDH	Supply voltage		12		50	V
VDDM	Driver supply voltage regulator output			9		V
VDDL	3V voltage regulator output			3.3		V
I_{DD}	Operating current consumption	UVLO=2V, PWM1=0, Rset=6kΩ, Vth=0.47V	4.6	5.0	5.6	mA
I_{DDQ}	Quiescent current consumption	UVLO=0V, PWM1=0, Rset=6kΩ, Vth=0.47V	2.25	2.50	2.75	mA
		Current Sink Parameters				
I_{LED_100}	Trimmed current accuracy	ILED=100mA, Tj=25 °C excluding error of Rset	0.8		0.8	%
I_{LED_ALL}	Current accuracy	ILED=50[(1)] to 250mA, BJT β>50 Tj=-20°C to 115°C	-1.5		1.5	%
I_{CH_100}	Channel to channel accuracy	ILED=100mA, Tj = 25°C	-0.6		0.6	%
V_{IsetX}	Reference voltage at pins Iset		1.18	1.20	1.22	V
Ratio	Ratio = ILED/Iset			500		
I_{BX}	Base output current limit		5.5		7.5	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Short Detection Comparator						
ACC_{short}	Overtemperature protection accuracy	Accuracy of V_{be} comparison with V_{TH} level	-10		10	mV
Power Supply Regulation						
B_{th}	BJT beta threshold		45	48	52	
Boost Controller Oscillator						
f_{osc}	Oscillator frequency		220	250	280	kHz
Boost Controller PWM						
D_{MAX}	Maximum duty cycle		85	87	89	%
Boost Controller Error Amplifier						
V_{FB}	Reference voltage at pin FB		1.23	1.25	1.27	V
A_V	Voltage gain			80		dB
BW	Bandwidth	A_V=0dB		2		MHz
I_{FB_in}	Voltage sense input current	Pins FB		0.1	0.2	µA
I_{comp_out}	Compensation output current	Pins COMP, V_{comp} = 1V		10		µA
Boost Controller Overcurrent Protection						
V_{SENSE}	Current sense threshold	Pin SENSE	600	800	1000	mV
Boost Controller Driver						
R_{driver}	Driver resistance sink and source	Pin GATE	4	6	8	Ω
V_{driver}	GATE maximum output voltage	IGATE = 0mA		VDDM		V
t_{RISE_driver}	GATE voltage rise time	VGATE=0 to 3V, CLOAD=3nF	15	25	50	ns
t_{FALL_driver}	GATE voltage fall time	VGATE=3 to 0V, CLOAD=3nF	15	25	50	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Boost Controller Undervoltage Lockout						
V_{UVLO}	Undervoltage lockout threshold		1.28	1.35	1.42	V
I_{UVLO_Hyst}	Undervoltage lockout hysteresis current			20		µA
Digital Pins						
V_{IH}	Logic high input threshold		1.8			V
V_{IL}	Logic low input threshold				0.8	V
V_{OL}	Logic low output level	PIN x FAULT open drain. I=-2mA			0.3	V
R_{PU}	Input resistance pull-up inputs			300		kΩ
R_{PD}	Input resistance pull-down inputs			300		kΩ
Thermal Protection						
T_{OFF}	Thermal shutdown threshold			140		°C
T_{hyst}	Thermal shutdown hysteresis			30		°C

Note(s):

1. It is not recommended to set ILED < 50mA in order to minimize influences of offset voltages.

Typical Operating Characteristics

$V_{OUTBoost}$ = 60V; I_{OUT} = 1A, T_A = 25ºC (unless otherwise specified)

Figure 7:
Boost - Efficiency vs. Output Current; V_{IN} = 13V

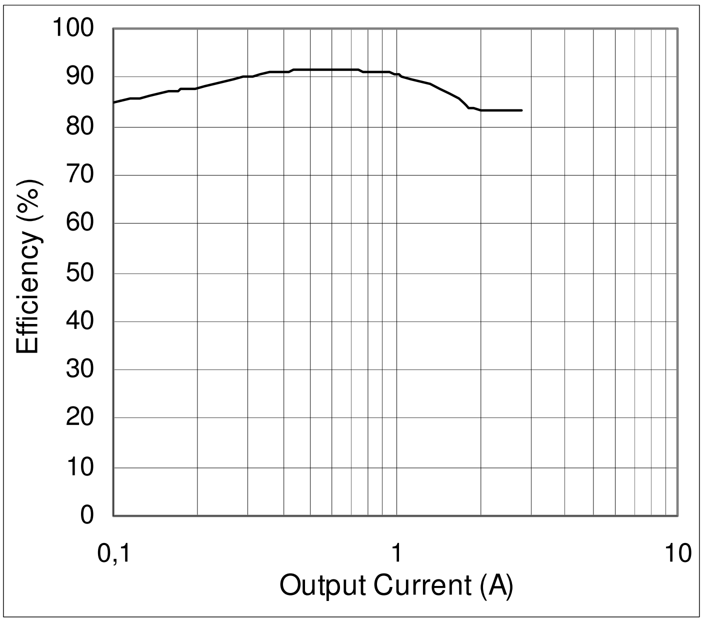


Figure 8:
Boost - Efficiency vs. Output Current; V_{IN} = 24V

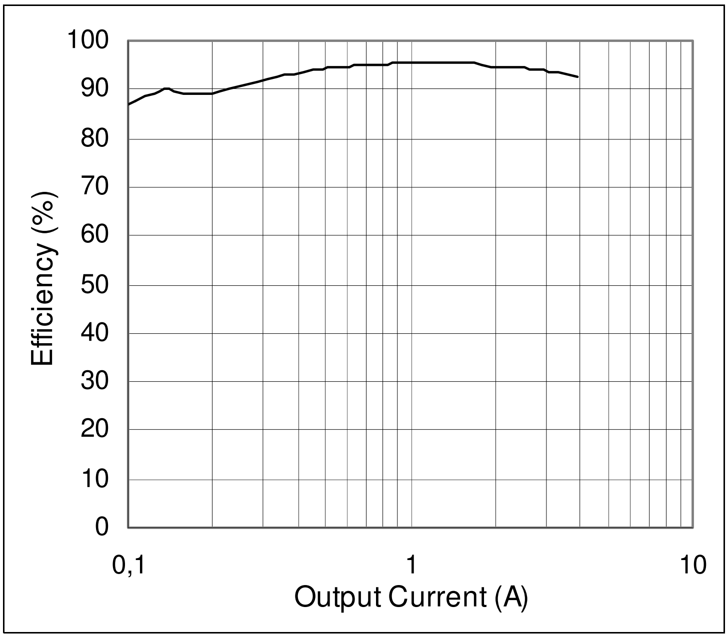


Figure 9:
V_{OUT} vs. I_{OUT}, V_{IN} = 13V

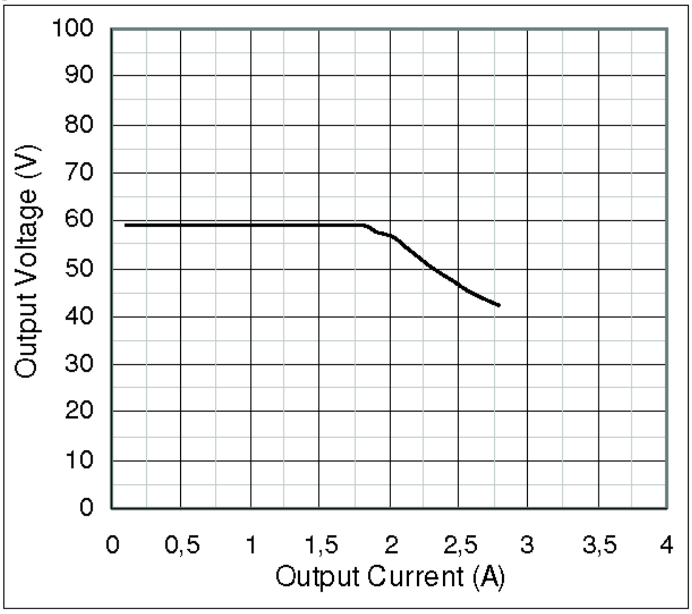


Figure 10:
V_{OUT} vs. I_{OUT}, V_{IN} = 24V

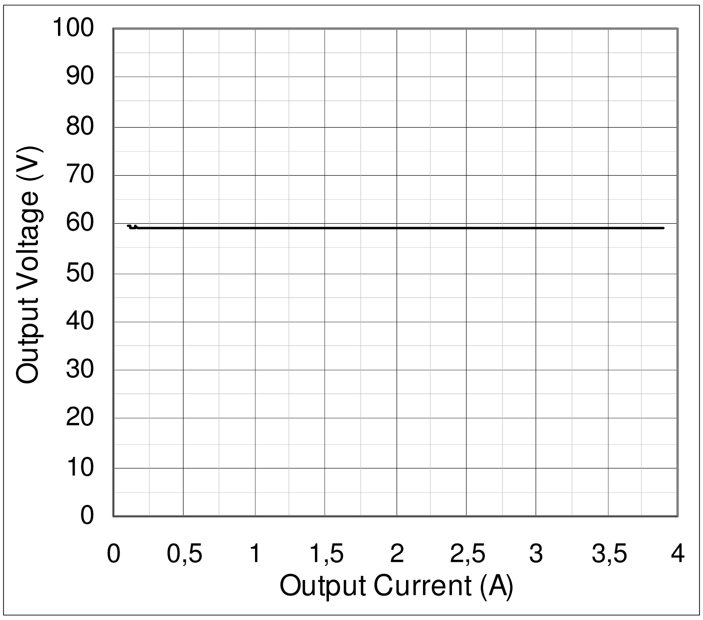


Figure 11:
Boost - Efficiency vs. Input Voltage, I_{OUT} = 1A

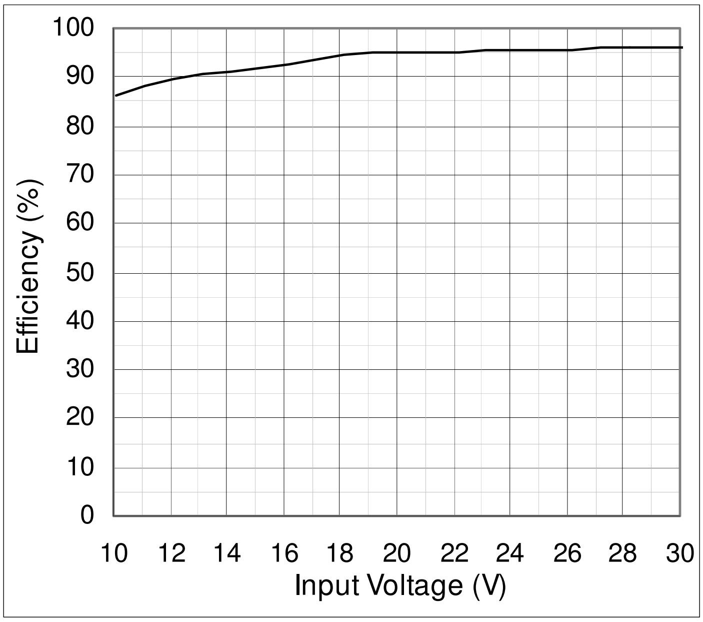
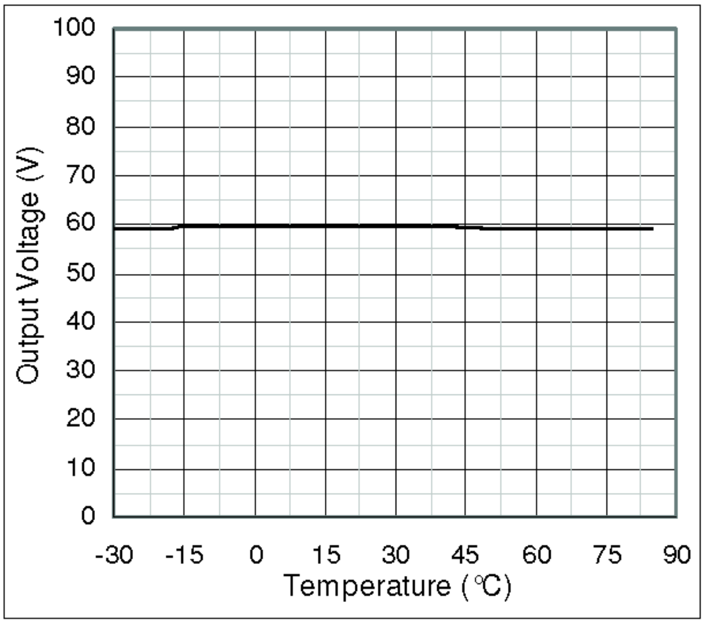


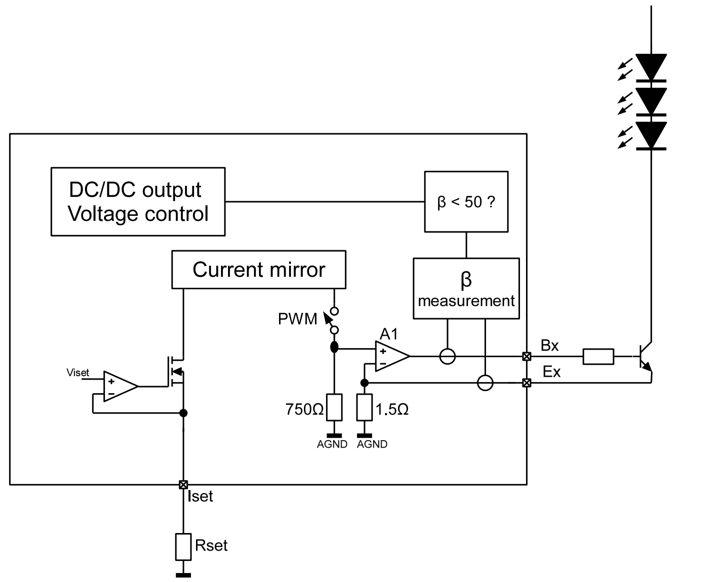
Figure 12:
V_{OUT} vs. Temp, V_{IN} = 24V, I_{OUT} = 0.2A



Detailed Description

Precision Current Output

Figure 13:
Current Output Stage



The LED-current is derived from either R_{set} using the following equation:

(EQ1)

$$I_{LED} = RATIO \times I_{set} = RATIO \times \frac{V_{set}}{R_{set}} = 500 \times \frac{1.2V}{R_{SET}}$$

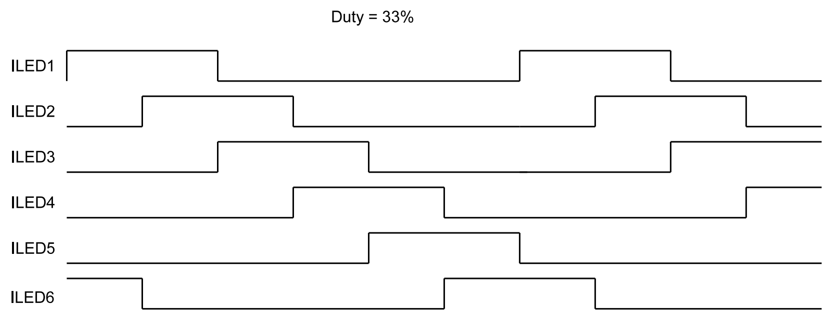
I_{set} is protected against a short to ground. In the case of a ground short the current I_{set} is limited to 660µA and the LED-current to 330mA.

I_{set} has a lower limit of 6µA with a 1µA hysteresis.This sets the lower limit of the LED-current to 3mA with R_{set}=200kΩ. If R_{set} is larger than 200kΩ, the LED-current is set to 0mA.

Phase Shift

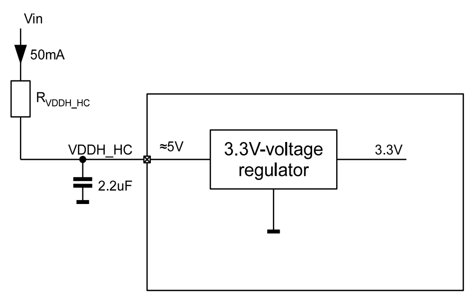
The outputs are controlled by the PWM-input and a built in phase shift generator. All outputs are phase shifted by 1/6 of the PWM-period. In order to calculate the phase shift timing, two PWM-periods are needed. This means that after changing the PWM-frequency, the phase shift is updated after the second period. The PWM-frequency must be in the range from 60Hz to 1kHz.

Figure 14:
Phase Shift



VDDH_HC Resistor

Figure 15:
VDDH_HC Resistor



Pin VDDH_HC is connected to an internal 3.3V voltage regulator. In order to keep the power dissipation of this regulator low, it is recommended to connect pin VDDH_HC to the power supply V_{IN} with a resistor. The resistor should guarantee sufficient voltage drop so that the remaining voltage at pin VDDH_HC is approximately 5V. The power dissipation of the R_{VDDH_HC} has to be considered.

(EQ2) $$R_{VDDH\_HC} = \frac{V_{in} - 5V}{75mA}$$

(EQ3) $$P_{R_{VDDH\_HC}} = (75mA)^2 \times R_{VDDH\_HC}$$

Typical values for R_{VVDH2} are:

V_{IN} = 13V: R_{VDDH_HC}= 100Ω / 1W

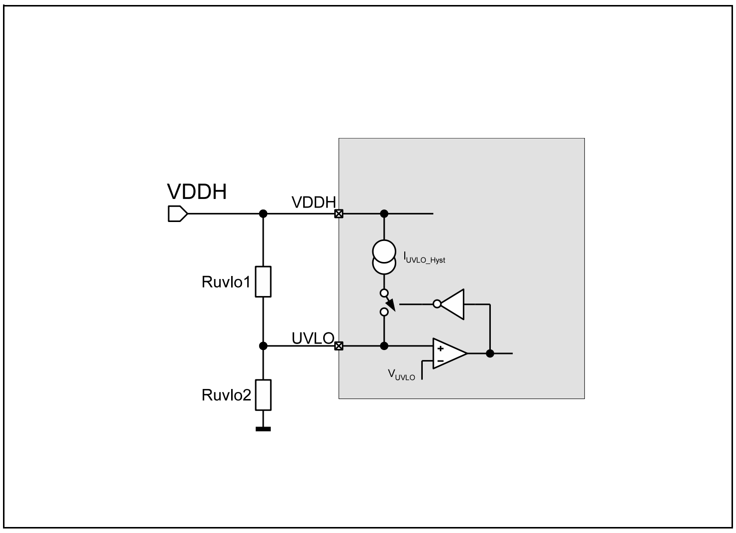
V_{IN} = 24V: R_{VDDH_HC}= 250Ω / 2W

Safety Features

Undervoltage Lockout

In order to avoid startup of the Boost controller at low supply voltage an undervoltage lockout function is implemented. The boost controller only turns ON when the voltage at pin UVLO exceeds VUVLO. Once the boost controller is turned ON a current source I_{UVLO_Hyst} is activated which increases the UVLO voltage and so shifts the turn OFF voltage level.

Figure 16:
Undervoltage Lockout



Following equations can be derived for adjusting the threshold voltages:

Undervoltage lockout HIGH level:

(EQ4)
$$V_{DDH\_UVH} = V_{UVLO} \times \left(1 + \frac{R_{UVLO1}}{R_{UVLO2}}\right)$$

Undervoltage lockout LOW level:

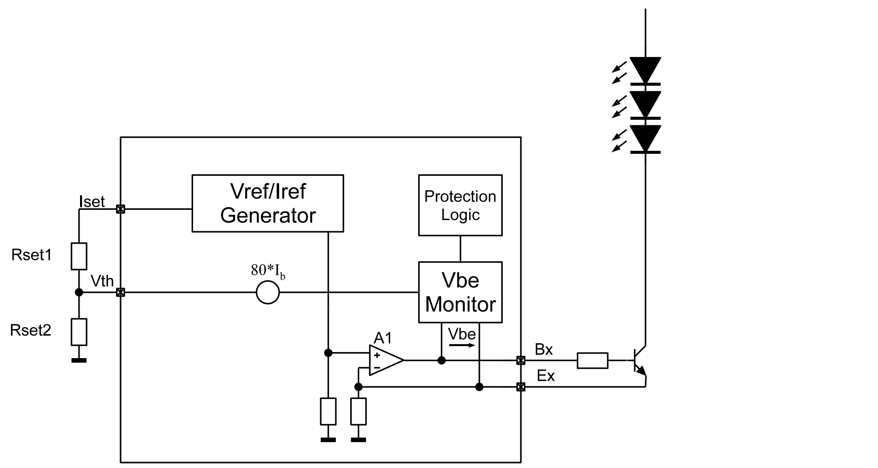
(EQ5)
$$V_{DDH\_UVL} = V_{UVLO} \times \left(1 + \frac{R_{UVLO1}}{R_{UVLO2}}\right) - I_{UVLO} \times R_{UVLO1}$$

Overtemperature Shutdown

If the device temperature reaches T_{OFF} the boost controller and all current outputs are turned OFF. After the temperature has decreased by T_{hyst} all blocks are turned ON again.

Short LED Protection

Figure 17:
Short LED Protection



A built in short protection comparator is monitoring the junction temperature T_J of the external bipolar transistors by measuring the base-emitter voltage V_{BE}.

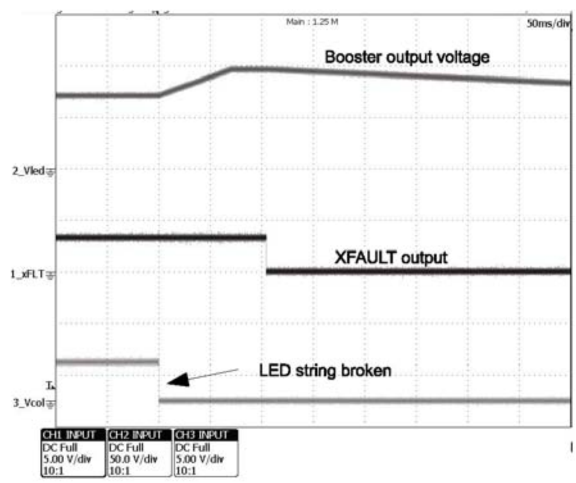
(EQ6) V_{BE}=1.2V -0.002 x T_J

T_J Junction temperature in K

When the measured V_{BE} gets lower than the voltage applied at pin Vth an overtemperature an hence an short LED condition is detected. Subsequently the fault output is activated (xFAULT = 0) and the corresponding output is deactivated.

Open LED Detection

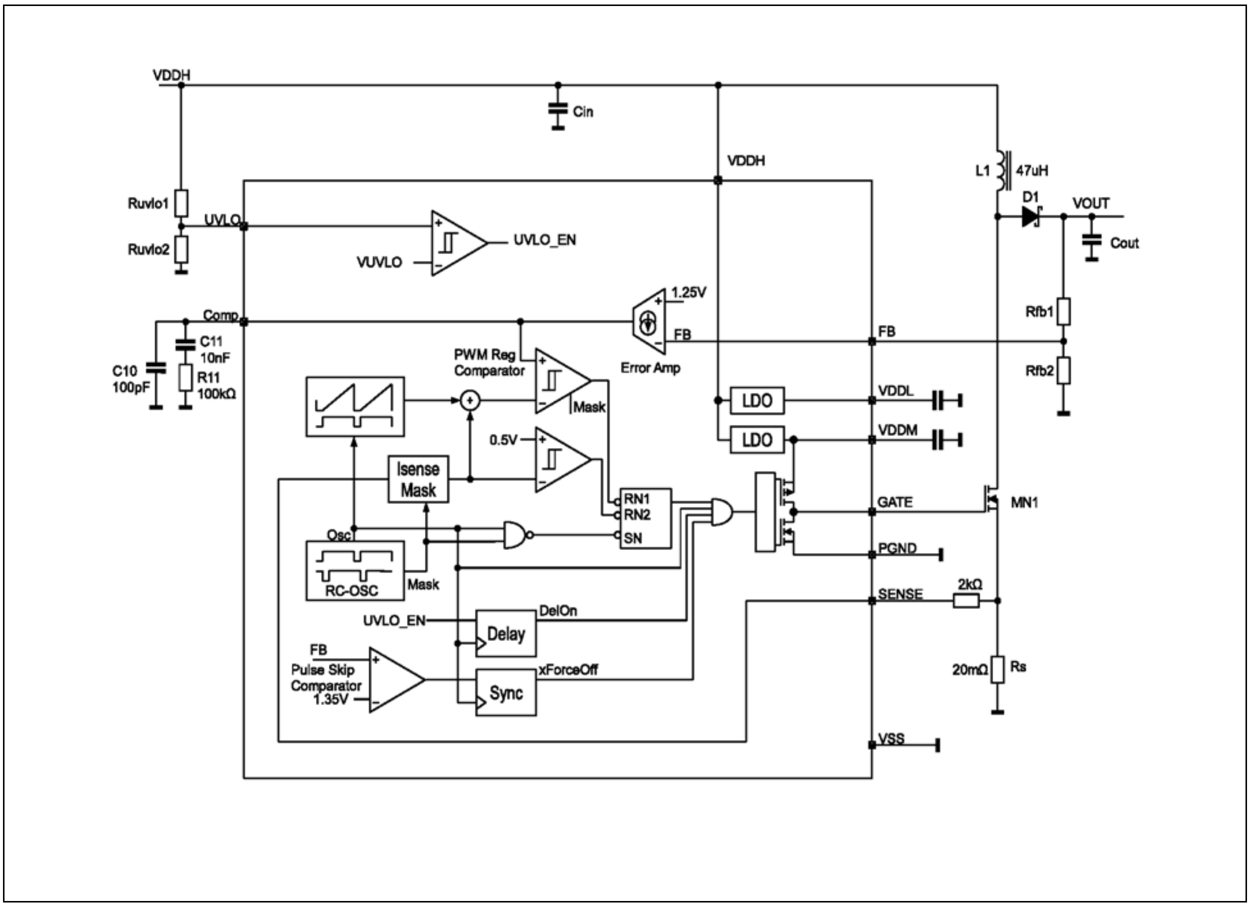
Figure 18:
Open LED Detection



A broken LED-string is detected during PWM=1. If a LED-string is broken the power supply feedback will increment the IDAC to increase the power supply output voltage. After the IDAC has reached its maximum value, a debounce counter is started. In order to run the debounce counter, the corresponding PWM-signal has to be high for more than 150µs. After the debounce counter has counted up for 32ms, the fault output is activated (xFAULT = 0) and the corresponding output is disconnected from the power supply feedback loop.

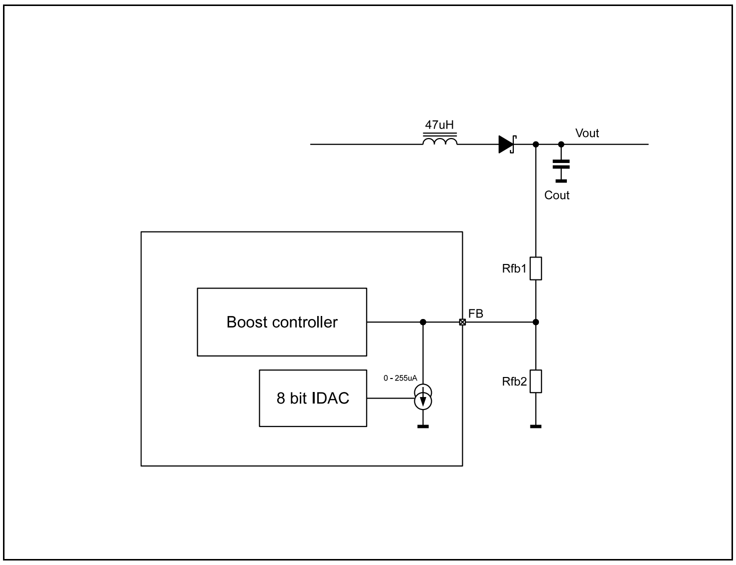
Boost Controller

Figure 19:
Boost Controller



Setting the Output Voltage

Figure 20:
V_{OUT} Setting



According to the requirements of the LED strings, the output voltage V_{out} is adjusted by the internal power supply feedback between:

$$V_{OUTmin} = V_{fb}\left(1 + \frac{R_{fb1}}{R_{fb2}}\right)$$

and

$$V_{OUTmax} = V_{fb}\left(1 + \frac{R_{fb1}}{R_{fb2}}\right) + 255\mu A \cdot R_{fb1}$$

Once V_{out_min} and V_{out_max} is known the external resistors can be calculated:

(EQ7) $$R_{fb1} = \frac{(V_{OUTmax} - V_{OUTmin})}{255\mu A}$$

(EQ8) $$R_{fb2} = \frac{V_{fb} \cdot R_{fb1}}{(V_{OUTmin} - V_{fb})}$$

Note(s): The overall resistance should be in the range of 100kΩ to 200kΩ to avoid any noise issues. Keep FB-line as short as possible.

Continuous Conduction Mode (CCM)

For normal operation the converter should stay in continuous conduction mode, to ensure that the inductor value must be bigger than L_{CRIT}.

(EQ9)
$$L_{CRIT} = \frac{\left(1 - \frac{V_{IN}}{V_{OUT} + V_D}\right) \times V_{IN}^2 \times R}{2 \times f_{SW} \times (V_{OUT} + V_D)^2}$$

Where:

V_{IN}	Input voltage at VDDH
V_{OUT}	Output voltage
V_D	Diode forward voltage at D1
f_{SW}	Switching frequency
R	Load resistor, should be calculated with minimum current load $R = V_{OUT} / I_{OUT\_min}$
I_{OUT_min}	Minimum output current (e.g. for LED driver only one LED string is on)

Duty Cycle

Within CCM, the well known relation between input and output voltage is derived in the following equation:

(EQ10)
$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{1}{1 - D}$$

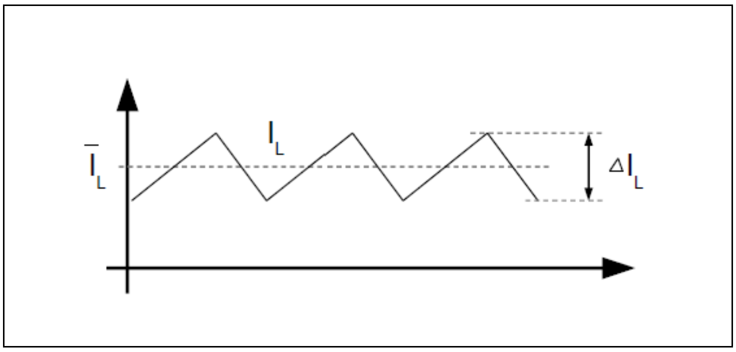
this means for the duty cycle:

(EQ11)
$$D = \left(1 - \frac{V_{IN}}{V_{OUT} + V_D}\right)$$

Inductor Current

The inductor current varies during a switching cycle. This variation can be expressed by the mean value of the inductor current and the delta rise/fall current within each cycle (see Figure 21).

Figure 21:
Inductor Current



Mean inductor current:

(EQ12)
$$\overline{I_L} = \frac{I_{OUT}}{1 - D}$$

Delta inductor current:

(EQ13)
$$\Delta I_L = \frac{D \times V_{IN}}{f_S \times L}$$

Peak current:

(EQ14)
$$I_{pk} = \overline{I_L} + \frac{\Delta I_L}{2} = \frac{I_{OUT}}{1 - D} + \frac{D \times V_{IN}}{2 \times f_S \times L}$$

RMS inductor current:

(EQ15)
$$I_{RMS} = \sqrt{\overline{I_L}^2 + \left(\frac{1}{12} \times \Delta I_L\right)^2}$$

This peak current is flowing through MN1 during phase 1 and through D1 during phase 2 of each cycle. Therefore this peak current is important for a proper diode, MOSFET and inductor selection.

Note(s): The saturation current of the inductor should be about 20% to 30% larger than the peak current

Input Capacitor

The input capacitor has to supply the delta inductor current and it should be selected according to:

(EQ16)
$$C_{IN} > \frac{\Delta I_L}{4 \times \Delta V_{IN} \times f_{SW}}$$

(EQ17)
$$ESR > \frac{\Delta V_{IN}}{2 \times \Delta I_L}$$

Output Capacitor

The output capacitor must be chosen according to the max allowable output ripple at high load.

(EQ18)
$$C_{OUT} > \frac{I_{OUT-max} \times D}{\Delta V_{OUT} \times f_{SW}}$$

(EQ19)
$$ESR > \frac{\Delta V_{OUT}}{\left(\frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times L \times f_{SW}}\right)}$$

Current Sense Resistor

(EQ20)
$$R_{S-max} = \frac{V_{SENSE}}{\overline{I_L} \times 0.5 \times \Delta I_L}$$

(EQ21)
$$P_{RS} = I^2{}_{L-rms} \times R_S \times D$$

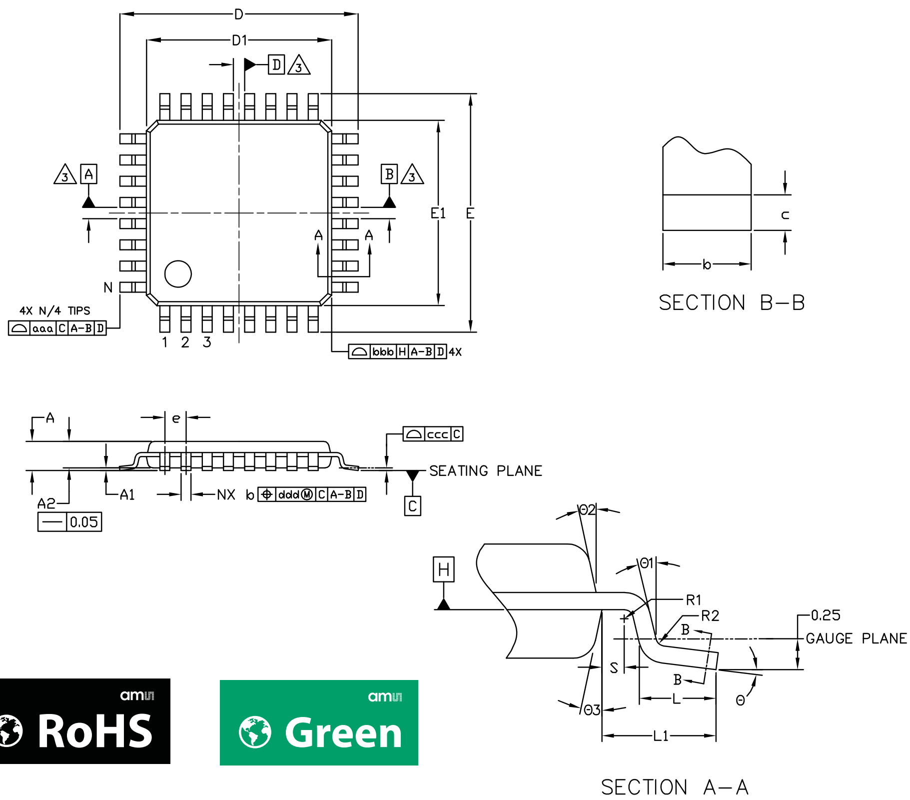
Note(s): Low inductance, specific designed current sensing resistors should be used, e.g. Stackpole Electronics CSR/CSRN series of sensing resistors with less than 0.2nH (typ.).

Compensation Network

A typical choice for values of the compensation network is C10 = 100pF, C11 = 10nF, R11 = 100kΩ. Use these values as initial choice and evaluate the transient response of the system to verify the behavior at output load change.

Package Drawings & Markings

Figure 22:
TQFP-32 Package Drawing



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.45
c	0.09	-	0.20
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
e		0.80 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	

Symbol	Min	Nom	Max
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Θ1	0°	3.5°	7°
Θ2	11°	12°	13°
Θ3	11°	12°	13°
aaa	-	0.20	-
bbb	-	0.20	-
ccc	-	0.10	-
ddd	-	0.20	-
N		32	

Note(s):

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Datums A & B to be determined at datum H.

Figure 23:
TQFP-32 Package Marking

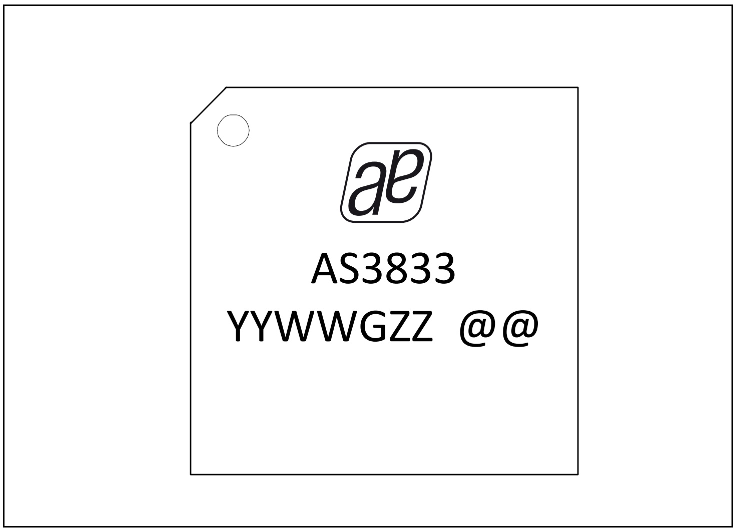
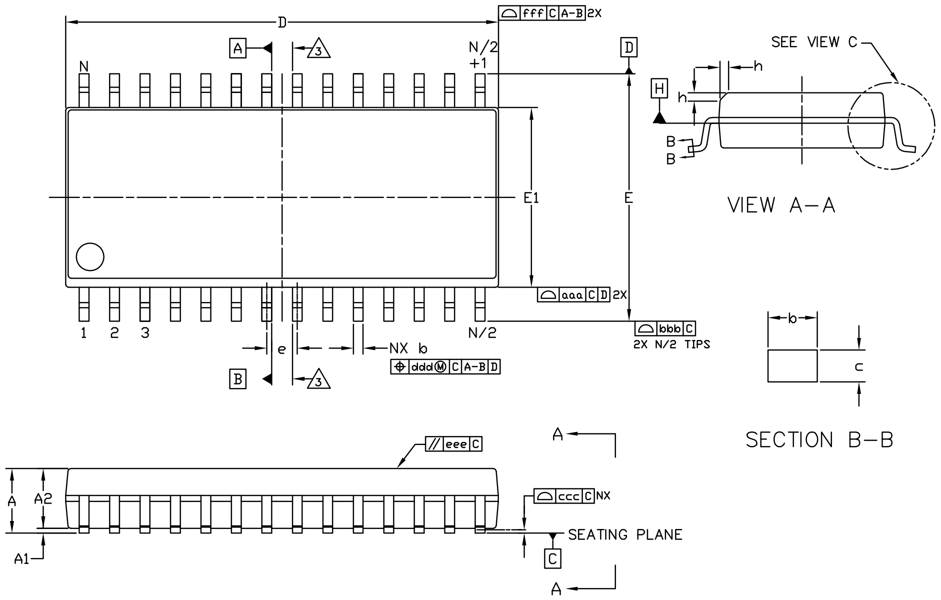
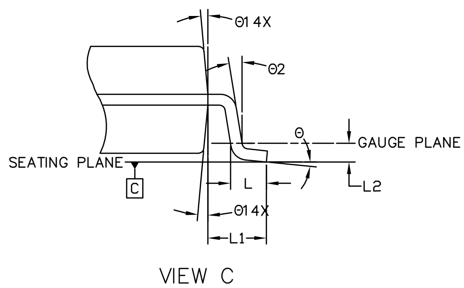


Figure 24:
Packaging Code

YY	WW	G	ZZ	@@
Manufacturing year	Manufacturing week	Plant identifier	Free choice/ traceability code	Sublot identifier

Figure 25:
SOIC-28 Package Drawing





Symbol	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.05	-	-
b	0.31	-	0.51
c	0.20	-	0.33
D	17.90 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		

Symbol	Min	Nom	Max
h	0.25	-	0.75
Θ	0°	-	8°
Θ1	5°	-	15°
Θ2	0°	-	-
aaa	0.10		
bbb	0.33		
ccc	0.10		
ddd	0.25		
eee	0.10		
fff	0.20		
ggg	0.15		
N	28		

Note(s):

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Datums A & B to be determined at datum H.

Figure 26:
SOIC-28 Package Marking

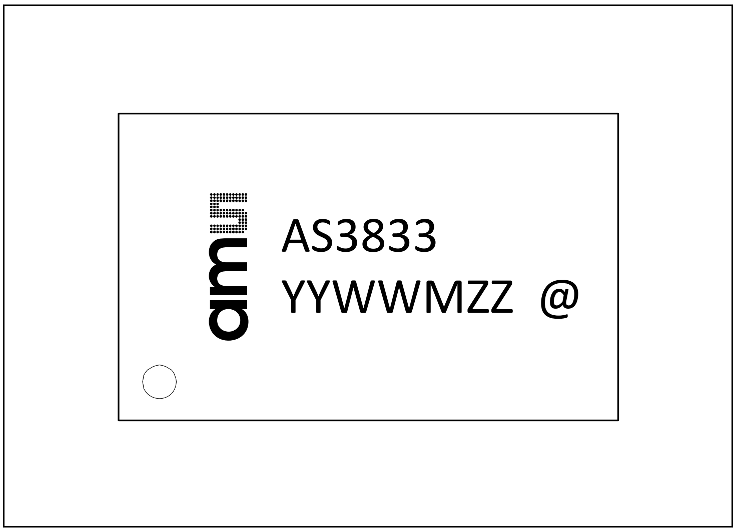


Figure 27:
Packaging Code

YY	WW	M	ZZ	@
Manufacturing year	Manufacturing week	Plant identifier	Free choice/ Traceability code	Sublot identifier

Ordering & Contact Information

Figure 28:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS3833-ZTQT	TQFP-32	AS3833	Tape & Reel	2000 pcs/reel
AS3833-ZSOT	SOIC-28	AS3833	Tape & Reel	1500 pcs/reel

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1.8 to current revision 2-01 (2016-Dec-08)	Page
1.8 to 2-00 (2016-Nov-29)	
Content of austriamicrosystems datasheet was converted to latest **ams** design	
Updated Subtitle, General Description, Applications and added Figure 1	1
Updated Figure 2	2
Updated Figure 3	3
Updated Figures 23 & 24	24
Updated Figures 26 & 27	26
Updated Figure 28	27
2-00 (2016-Nov-29) to 2-01 (2016-Dec-08)	
Updated Figure 5	5

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide