700MHz to 2700MHz Analog VGA with Threshold Alarm Circuit and Error Amplifier for Level Control

General Description

The MAX2092 high-linearity analog variable-gain amplifier (VGA) is a monolithic SiGe BiCMOS attenuator/amplifier/error amplifier with an alarm circuit designed to interface with 50Ω systems operating in the 700MHz to 2700MHz frequency range. The device features a gain range of +18.1dB to -22.3dB, a noise figure of 5.2dB, OIP3 linearity of +32.5dBm, and a wide RF bandwidth. Each of these features makes the device an ideal VGA for numerous receiver and transmitter applications. When paired with the MAX2091 or MAX2091B variable gain upconverter, a complete 2-chip IF-RF signal conditioning solution is possible for microwave point-to-point transmitters.

The MAX2092 operates from a single +5V supply, and is available in a compact 20-pin TQFN package (5mm x 5mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range from T_C = -40°C to +95°C.

Applications

- Microwave Point-to-Point Receivers and Transmitters
- RF Variable-Gain Stages
- Temperature Compensation Circuits
- Cellular Applications
- WiMAX® Applications
- LTE Applications
- Fixed Broadband Wireless Access
- Wireless Local Loop

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Benefits and Features

- Wide Band Analog VGA Increases System Performance
  - 700MHz to 2700MHz RF Frequency Range
  - High Linearity
    - +32.5dBm OIP3
    - +18.2dBm Output -1dB Compression Point
  - 18.1dB Gain with 40.4dB Attenuation Range and 0.03dB Gain Variation Over 100MHz Bandwidth at 1835MHz
  - 5.2dB Noise Figure (Includes Attenuator Insertion Loss)
- Integrated Error Amplifier and Alarm Circuit Simplifies ALC Operation
- Lowers Power Consumption with Power-Down Capability
- Package with Exposed Pad Improves Heat Dissipation and System Performance

***Ordering Information* appears at end of data sheet.**

19-6377; Rev 1; 7/15

maxim integrated™

Absolute Maximum Ratings

V_{CC_RF}, V_{CC_A}..-0.3V to +6V
RF_OUT, RF_IN .... -0.3V to (V_{CC} + 0.3V)
R_BIAS, CTRL1, CTRL2,
PLVLSET, DET_VIN ... -0.3V to Minimum (V_{CC} + 0.3V, +3.6V)
RF_IN Input Power ....+15dBm
RF_OUT Output Power...+23dBm
Continuous Power Dissipation (Note 1) 2.5W
Operating Case Temperature
Range (Note 2)...-40°C to +95°C
Maximum Junction Temperature....................................+150°C
Storage Temperature Range............................-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.
Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Package Thermal Characteristics

Junction-to-Ambient Thermal Resistance (θ_{JA})
(Notes 3, 4).. 32°C/W
Junction-to-Case Thermal Resistance (θ_{JC})
(Notes 1, 4)... 7°C/W

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.
Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(*Typical Application Circuit* with V_{CC} = 4.75V to 5.8V, V_{GND} = 0V, and T_C = -40°C to +95°C. Typical values are at V_{CC} = 5.5V and T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75		5.8	V
Total Supply Current	I_{DC}	Power down: CTRL1 = 0, CTRL2 = 0		2	3	mA
		VGA-only mode: CTRL1 = 1, CTRL2 = 0		80	90	
		ALC mode: CTRL1 = 1, CTRL2 = 1		93	110	
CTRL1/CTRL2 Logic-Low Input Voltage	V_{IL}				0.8	V
CTRL1, CTRL2 Logic-High Input Voltage	V_{IH}		2.2			V
Input Logic Current	I_{IH}, I_{IL}		-1		+1	µA
PLVLSET Input-Voltage Range	V_{IN}		0		2.5	V
DET_VIN Input-Voltage Range	V_{IN}		0		2.5	V

Recommended AC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 6)	700		2700	MHz

AC Electrical Characteristics

(*Typical Application Circuit* with analog attenuator set for maximum gain, V_{CC} = 4.75V to 5.8V, f_{RF} = 1835MHz, P_{RFIN} = -16dBm (CW), T_C = -40°C to +95°C, and RF ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{RF_IN} = -16dBm, $V_{PLVLSET}$ = 2.5V, CTRL1 = 1, CTRL2 = 0. Min/max specifications apply over supply, process, and temperature, unless otherwise noted.) (Notes 5, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Gain	G	f_{RF} = 974MHz		17.3		dB
		f_{RF} = 1835MHz		18.1		
		f_{RF} = 2200MHz		18.1		
Gain vs. Temperature				-0.007		dB/°C
Gain Flatness vs. Frequency		974MHz ±50MHz		0.22		dB_{P-P}
		1835MHz ±50MHz		0.03		
		1835MHz ±80MHz		0.03		
		1835MHz ±100MHz		0.03		
		2200MHz ±100MHz		0.1		
Noise Figure	NF	f_{RF} = 974MHz		5.0		dB
		f_{RF} = 1835MHz		5.2		
		f_{RF} = 2200MHz		5.5		
Total Attenuation Range		f_{RF} = 974MHz		40.1		dB
		f_{RF} = 1835MHz		40.4		
		f_{RF} = 2200MHz		39.2		
Output Second-Order Intercept Point	OIP2	P_{RFOUT} = +2dBm/tone, Δf = 1MHz, f1+ f2		50		dBm
Output Third-Order Intercept Point	OIP3	P_{RFOUT} = +2dBm/tone, Δf = 1MHz; f_{RF} = 974MHz		34.3		dBm
		P_{RFOUT} = +2dBm/tone, Δf = 1MHz; f_{RF} = 1835MHz		32.5		
		P_{RFOUT} = +2dBm/tone, Δf = 1MHz; f_{RF} = 2200MHz		31.4		
Output -1dB Compression Point	P_{-1dB}	(Note 8)		18.2		dBm
Second Harmonic		P_{RFOUT} = +5dBm		52		dBc
Third Harmonic		P_{RFOUT} = +5dBm		61		dBc
Input Return Loss		1835MHz ±50MHz		18		dB
Output Return Loss		1835MHz ±50MHz		23		dB
ALARM CIRCUIT (CTRL1 = 1 CTRL2 = 1)						
Lower Alarm Threshold		Input = DET_VIN		0.175		V
Upper Alarm Threshold		Input = DET_VIN		2.25		V
Hysteresis				29		mV
Alarm Output Logic 1		Output = $\overline{ALM}$	3.135	3.3	3.465	V
Alarm Output Logic 0		Output = $\overline{ALM}$			0.4	V

AC Electrical Characteristics (continued)

(*Typical Application Circuit* with analog attenuator set for maximum gain, V_{CC} = 4.75V to 5.8V, f_{RF} = 1835MHz, P_{RFIN} = -16dBm (CW), T_C = -40°C to +95°C, and RF ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{RF_IN} = -16dBm, $V_{PLVLSET}$ = 2.5V, CTRL1 = 1, CTRL2 = 0. Min/max specifications apply over supply, process, and temperature, unless otherwise noted.) (Notes 5, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG ATTENUATOR (CTRL1 = 1, CTRL2 = 0)						
Minimum Attenuator Control Voltage		Input = PLVLSET		0.25		V
Maximum Attenuator Control Voltage		Input = PLVLSET		2.3		V
Average Gain-Control Slope		$V_{PLVLSET}$ = 0.25V to 2.3V		19.4		dB/V
Maximum Gain-Control Slope		$V_{PLVLSET}$ = 0 to 2.5V		27		dB/V

Note 5: Production tested at T_C = +95°C. All other temperatures guaranteed by design and characterization.

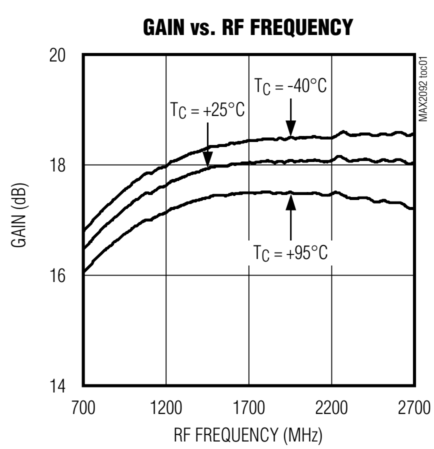
Note 6: Recommended functional range, not production tested. Operation outside this range is possible, but with degraded performance of some parameters.

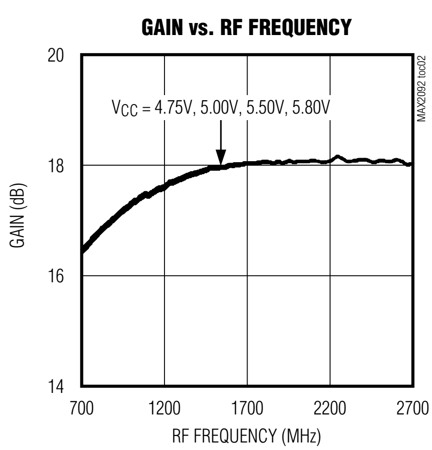
Note 7: All limits include external component losses. Output measurements are taken at the RF port of the *Typical Application Circuit*.

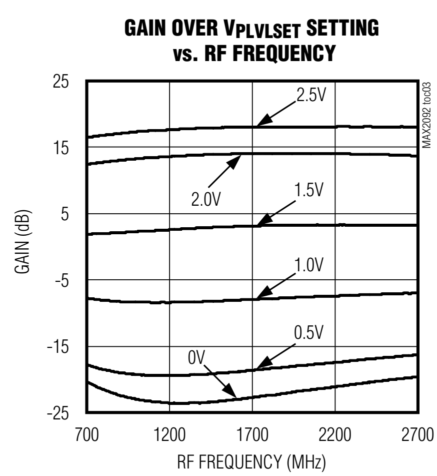
Note 8: It is advisable not to continuously operate the VGA RF-input above +12dBm.

Typical Operating Characteristics

(*Typical Application Circuit* with analog attenuator set to minimum attenuation, V_{CC} = 4.75V to 5.8V, f_{RF} = -16dBm, T_C = -40°C to +95°C, and RF ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{RF} = -16dBm, CTRL1 = 1, CTRL2 = 0, $V_{PLVLSET}$ = 2.5V, unless otherwise noted.)



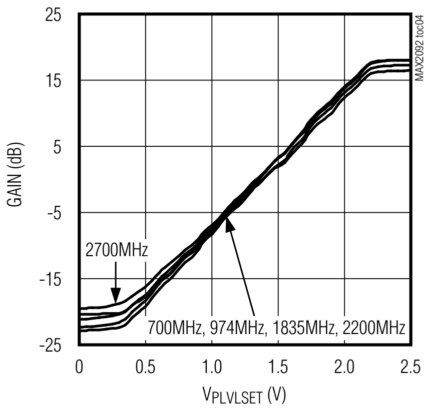




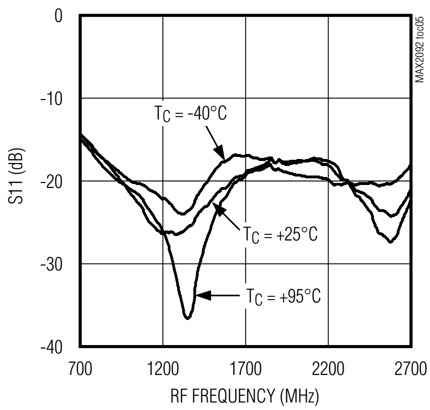
Typical Operating Characteristics (continued)

(*Typical Application Circuit* with analog attenuator set to minimum attenuation, V_{CC} = 4.75V to 5.8V, f_{RF} = -16dBm, T_C = -40°C to +95°C, and RF ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{RF} = -16dBm, CTRL1 = 1, CTRL2 = 0, $V_{PLVLSET}$ = 2.5V, unless otherwise noted.)

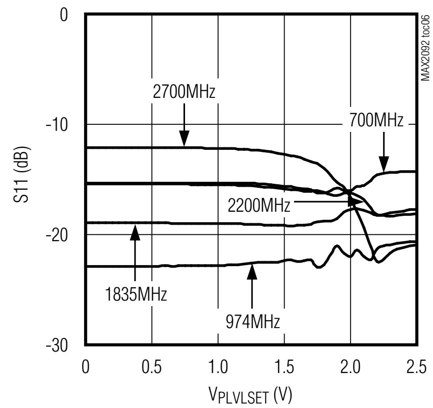
GAIN vs. $V_{PLVLSET}$ SETTING



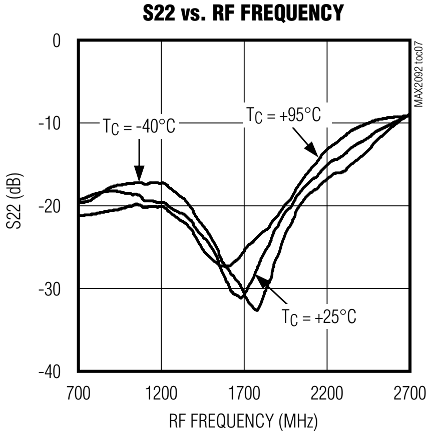
S11 vs. RF FREQUENCY



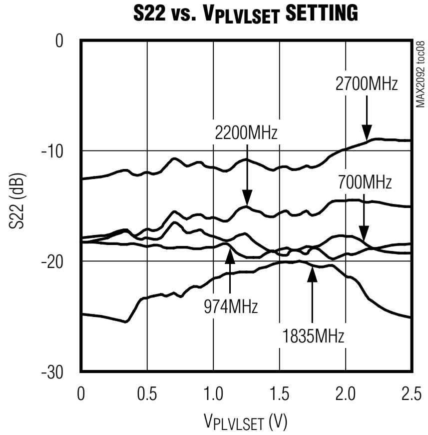
S11 vs. $V_{PLVLSET}$ SETTING



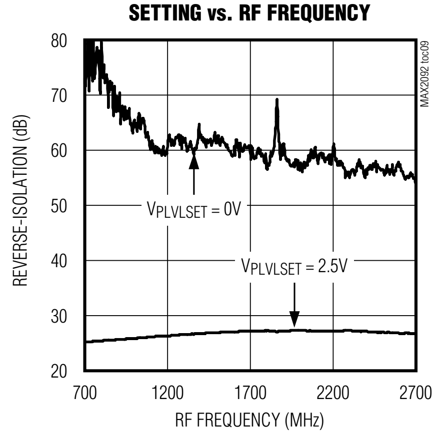
S22 vs. RF FREQUENCY



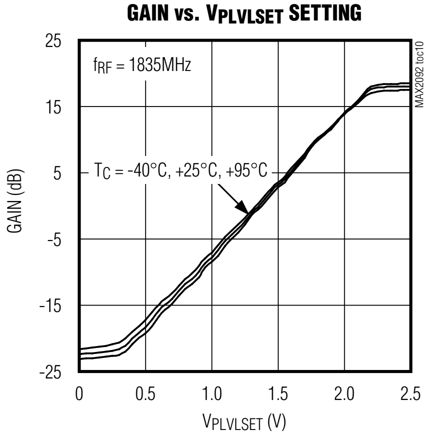
S22 vs. $V_{PLVLSET}$ SETTING



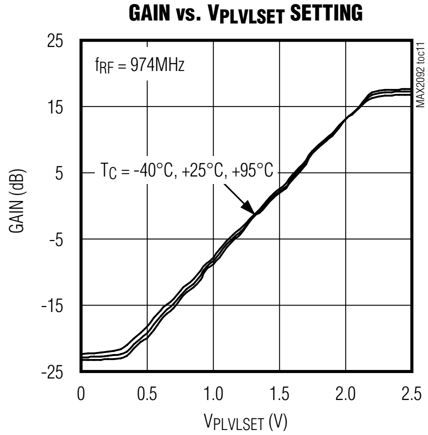
REVERSE-ISOLATION OVER $V_{PLVLSET}$ SETTING vs. RF FREQUENCY



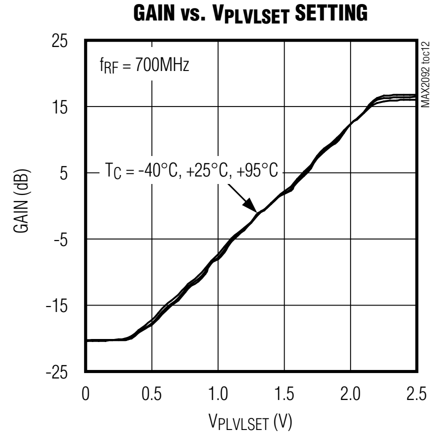
GAIN vs. $V_{PLVLSET}$ SETTING



GAIN vs. $V_{PLVLSET}$ SETTING



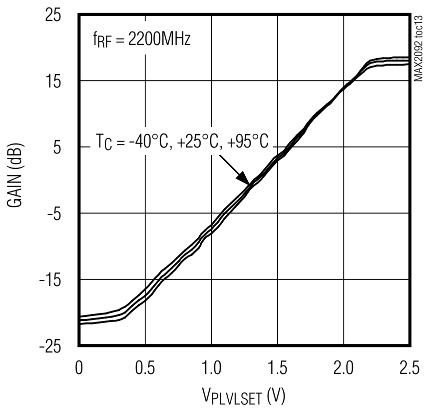
GAIN vs. $V_{PLVLSET}$ SETTING



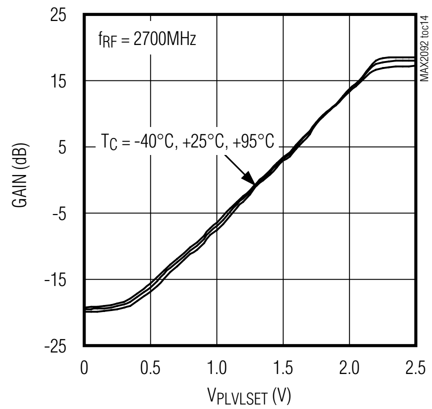
Typical Operating Characteristics (continued)

(*Typical Application Circuit* with analog attenuator set to minimum attenuation, V_{CC} = 4.75V to 5.8V, f_{RF} = -16dBm, T_C = -40°C to +95°C, and RF ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{RF} = -16dBm, CTRL1 = 1, CTRL2 = 0, $V_{PLVLSET}$ = 2.5V, unless otherwise noted.)

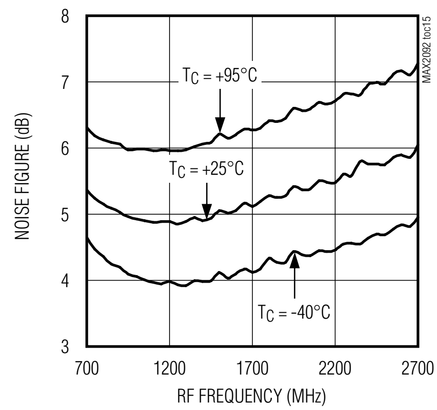
GAIN vs. $V_{PLVLSET}$ SETTING



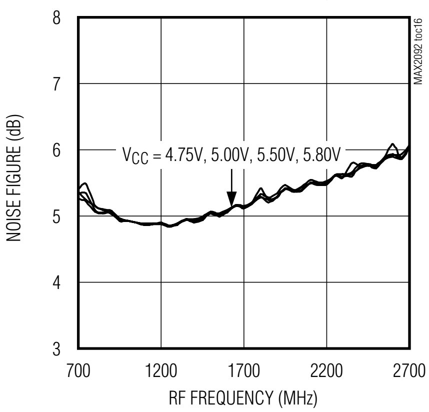
GAIN vs. $V_{PLVLSET}$ SETTING



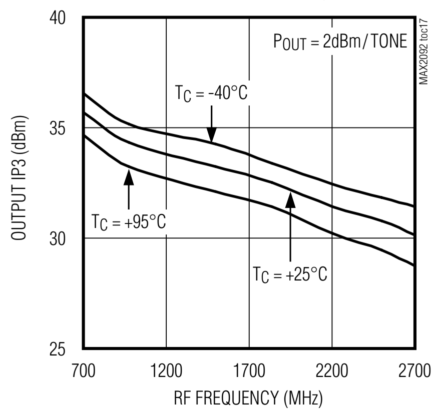
NOISE FIGURE vs. RF FREQUENCY



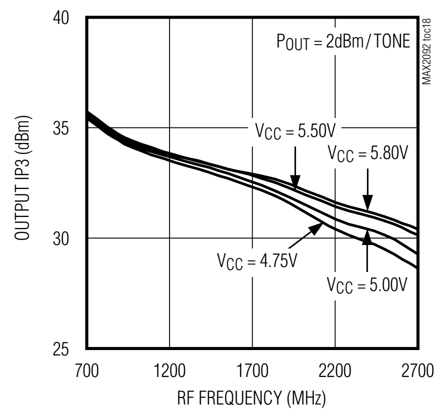
NOISE FIGURE vs. RF FREQUENCY



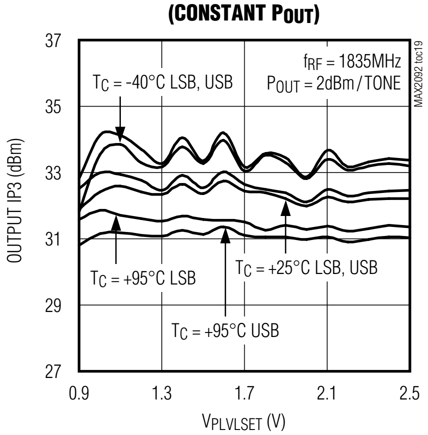
OUTPUT IP3 vs. RF FREQUENCY



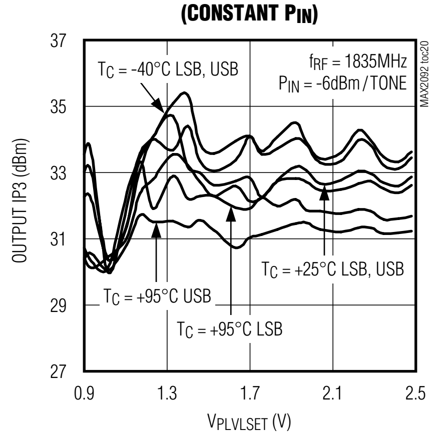
OUTPUT IP3 vs. RF FREQUENCY



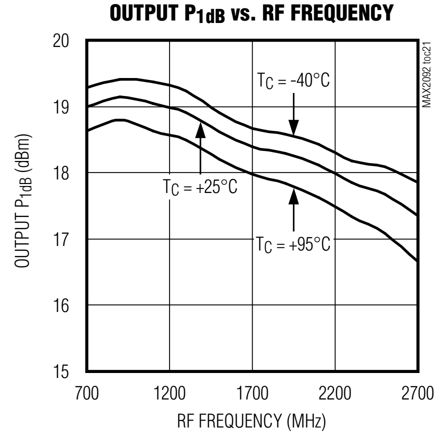
OUTPUT IP3 vs. $V_{PLVLSET}$ SETTING (CONSTANT P_{OUT})



OUTPUT IP3 vs. $V_{PLVLSET}$ SETTING (CONSTANT P_{IN})



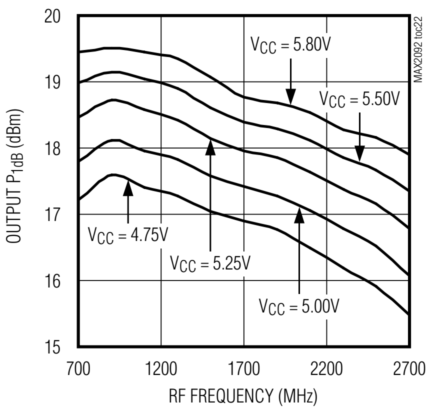
OUTPUT P_{1dB} vs. RF FREQUENCY



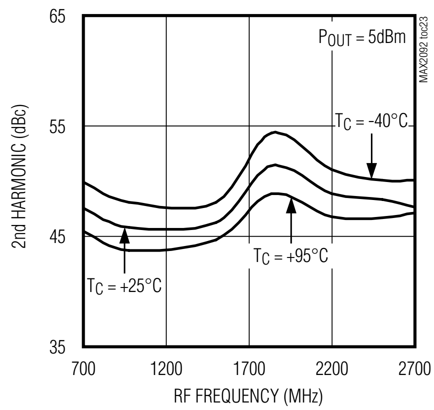
Typical Operating Characteristics (continued)

(*Typical Application Circuit* with analog attenuator set to minimum attenuation, V_{CC} = 4.75V to 5.8V, f_{RF} = -16dBm, T_C = -40°C to +95°C, and RF ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{RF} = -16dBm, CTRL1 = 1, CTRL2 = 0, $V_{PLVLSET}$ = 2.5V, unless otherwise noted.)

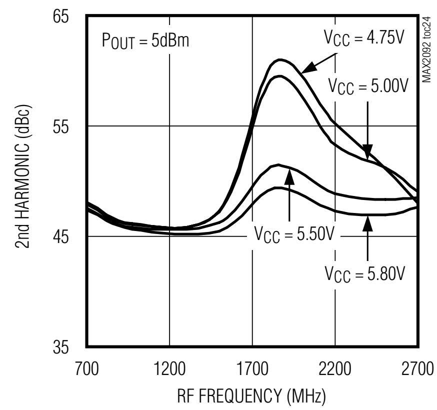
OUTPUT P1dB vs. RF FREQUENCY



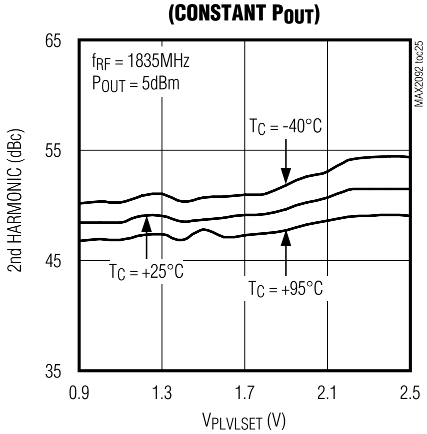
2nd HARMONIC vs. RF FREQUENCY



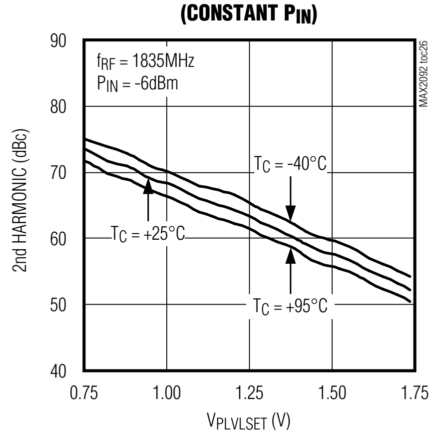
2nd HARMONIC vs. RF FREQUENCY



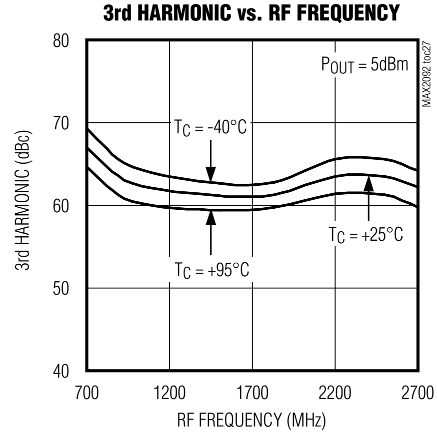
2nd HARMONIC vs. VPLVLSET SETTING (CONSTANT POUT)



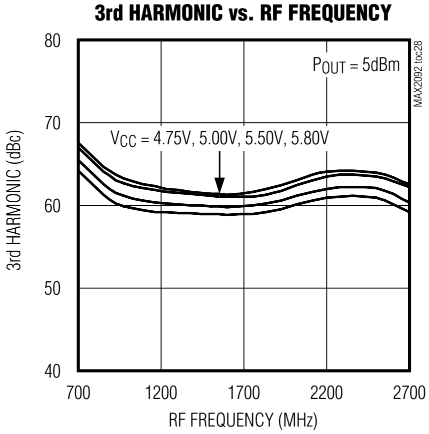
2nd HARMONIC vs. VPLVLSET SETTING (CONSTANT PIN)



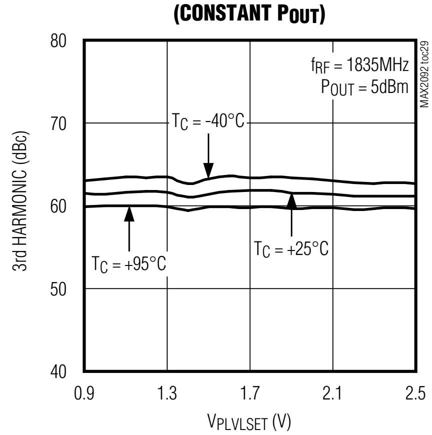
3rd HARMONIC vs. RF FREQUENCY



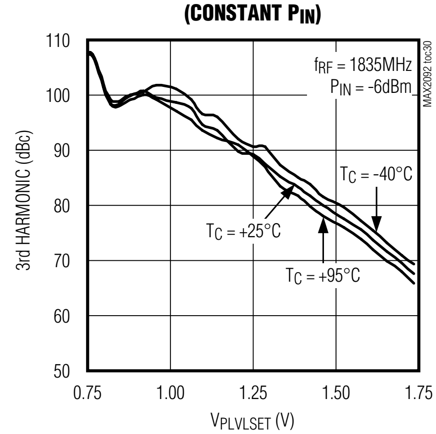
3rd HARMONIC vs. RF FREQUENCY



3rd HARMONIC vs. VPLVLSET SETTING (CONSTANT POUT)

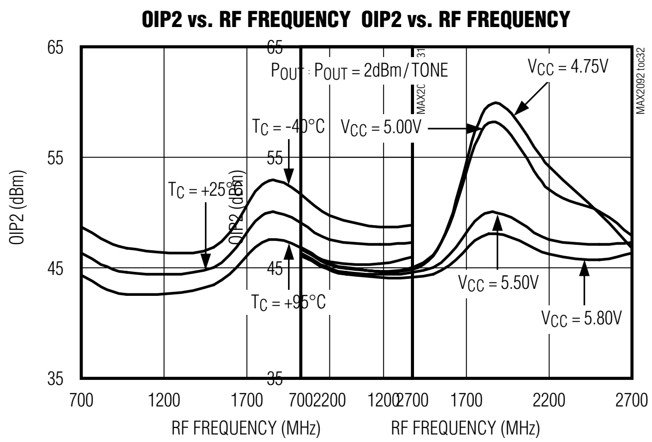


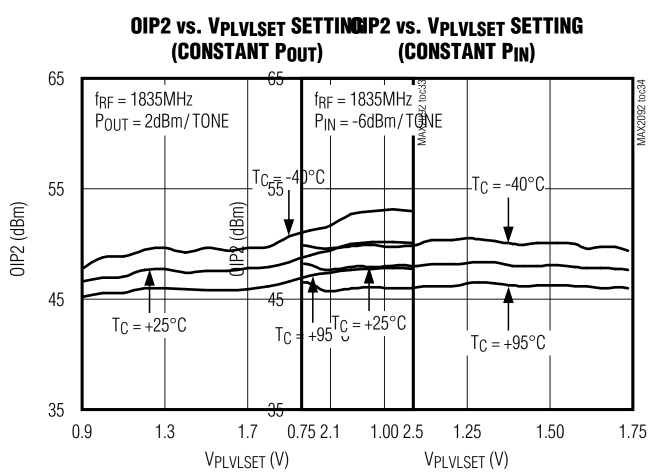
3rd HARMONIC vs. VPLVLSET SETTING (CONSTANT PIN)



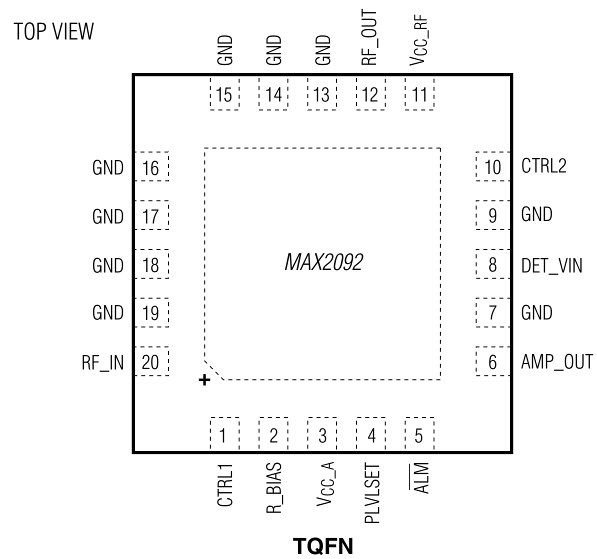
Typical Operating Characteristics (continued)

(*Typical Application Circuit* with analog attenuator set to minimum attenuation, V_{CC} = 4.75V to 5.8V, f_{RF} = -16dBm, T_C = -40°C to +95°C, and RF ports are connected to 50Ω sources and loads, unless otherwise noted. Typical values are at T_C = +25°C, V_{CC} = 5.5V, P_{RF} = -16dBm, CTRL1 = 1, CTRL2 = 0, $V_{PLVLSET}$ = 2.5V, unless otherwise noted.)





Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	CTRL1	Control-Mode Logic Input 1 (3.3V Logic)
2	R_BIAS	Bias Resistor Setting Input. Connect a resistor from this pin to ground.
3	VCC_A	Power-Supply Input. Bypass to ground with a 0.01µF capacitor as close as possible to the pin.
4	PLVLSET	Output-Power Level-Setting DC Input or Analog Attenuator Control Voltage
5	$\overline{\text{ALM}}$	Alarm Logic Output
6	AMP_OUT	Error-Amplifier Output
7, 13–19	GND	Ground
8	DET_VIN	Error-Amplifier Input Voltage from an External Detector
9	GND	**Do not directly connect to EP.** Connect to RF ground plane with a short trace using a separate via hole.
10	CTRL2	Control-Mode Logic Input 2 (3.3V Logic)
11	VCC_RF	Driver-Amplifier Supply Voltage Input. Bypass to ground with a 0.01µF capacitor as close as possible to the pin.
12	RF_OUT	Driver-Amplifier Output (50Ω). Requires a DC-blocking capacitor.
20	RF_IN	Attenuator Input (50Ω). Requires a DC-blocking capacitor.
—	EP	Exposed Pad. Internally connected to GND. Solder the exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance. See the *Layout Considerations* section.

Detailed Description

The MAX2092 is a high-linearity analog VGA designed to interface with 50Ω systems operating in the 700MHz to 2700MHz frequency range. The analog attenuator is controlled by an external analog control voltage. The device features a gain range of 18.1dB to -22.3dB, a noise figure of 5.2dB, OIP3 linearity of +32.5dBm, and a wide RF bandwidth. Each of these features makes the device an ideal VGA for numerous receiver and transmitter applications. In addition, the device operates from a single +5V supply.

Applications Information

Modes of Operation

The device can operate in several different modes, as summarized in Table 1.

VGA-Only Mode Operation

VGA-only mode operation consists of setting CTRL1 = logic 1 and CTRL2 = logic 0, and applying a DC value to PLVLSET between 0V and 2.5V DC to manually adjust the attenuation, and subsequently the RF_OUT power to any desired value. The output power at RF_OUT increases at a rate of 19.4dB/V as PLVLSET is increased. In VGA-only mode, operation components R5, R6, R7, and C8–C11 can be left unpopulated, and CTRL2 needs to be tied directly to ground.

Closed-ALC Mode Operation

Closed-ALC mode operation consists of setting CTRL1 = CTRL2 = logic 1. The voltage on PLVLSET is set externally to adjust output power from -20dBm to +5dBm when input power is in the recommended power range, typically -6dBm. See the *Typical Application Circuit*. As PLVLSET increases, the output power also increases at a rate set by the external detector chosen. Ideally, a detector with an output voltage range of 0.1V DC to 2.4V DC is recommended, but the device operates with any detector whose output ranges from 0V DC to 2.5V DC (output coupler at RF_OUT already taken into account). An error amplifier compares the DET_VIN voltage to PLVLSET, and drives the attenuator in servo fashion until the error-amplifier's differential input error voltage is near zero. The servo loop acts to maintain a regulated output power level over an input power range depending on the setting of PLVLSET.

When used in conjunction with the MAX2091 IF VGA, it is recommended that an external voltage of 1.65V be applied to the IF PLVLSET. This ensures that a nominal RF signal level of approximately -3dBm is output from the MAX2091. With this specific level setting, the complete MAX2091 + MAX2092 cascade yields a constant RF output power of -20.5dBm to +5dBm (depending on the setting of RF PLVLSET) over an IF input power range of -24dBm to +1dBm. See Figure 1 for details. Contact the factory for additional details surrounding Maxim's MAX2091 + MAX2092 reference design.

Control Inputs

The device has three control inputs: CTRL1, CTRL2, and PLVLSET. V_{CC} must be present before voltages are applied to these pins. In cases where this is not possible, a 200Ω resistor must be included in series with the control inputs to limit on-chip ESD diode conduction. CTRL1 and CTRL2 are 3V logic controls, and cannot be driven from 5V logic. In the case where no logic control is available and a logic high is required, a voltage divider can be used from the 5V V_{CC} supply to produce the 3V logic-high.

Alarm Operation

The alarm remains in logic-high state when the voltage on DET_VIN (pin 8) is within the 0.175V to 2.25V range. The alarm threshold amount is an internal fixed value to the device with a nominal hysteresis of approximately 29mV.

Table 1. Control Mode Logic

CTRL1	CTRL2	VGA	ALC LOOP	ALARM	FUNCTIONAL DESCRIPTION
0	0	Disabled	Disabled	Disabled	Power-Down Mode
1	0	Enabled	Disabled	Disabled	VGA-Only Mode
1	1	Enabled	Enabled	Enabled	Closed ALC Mode. ALC loop locks DET_VIN to PLVLSET.
0	1	—	—	—	Factory Test Mode (Do Not Use)

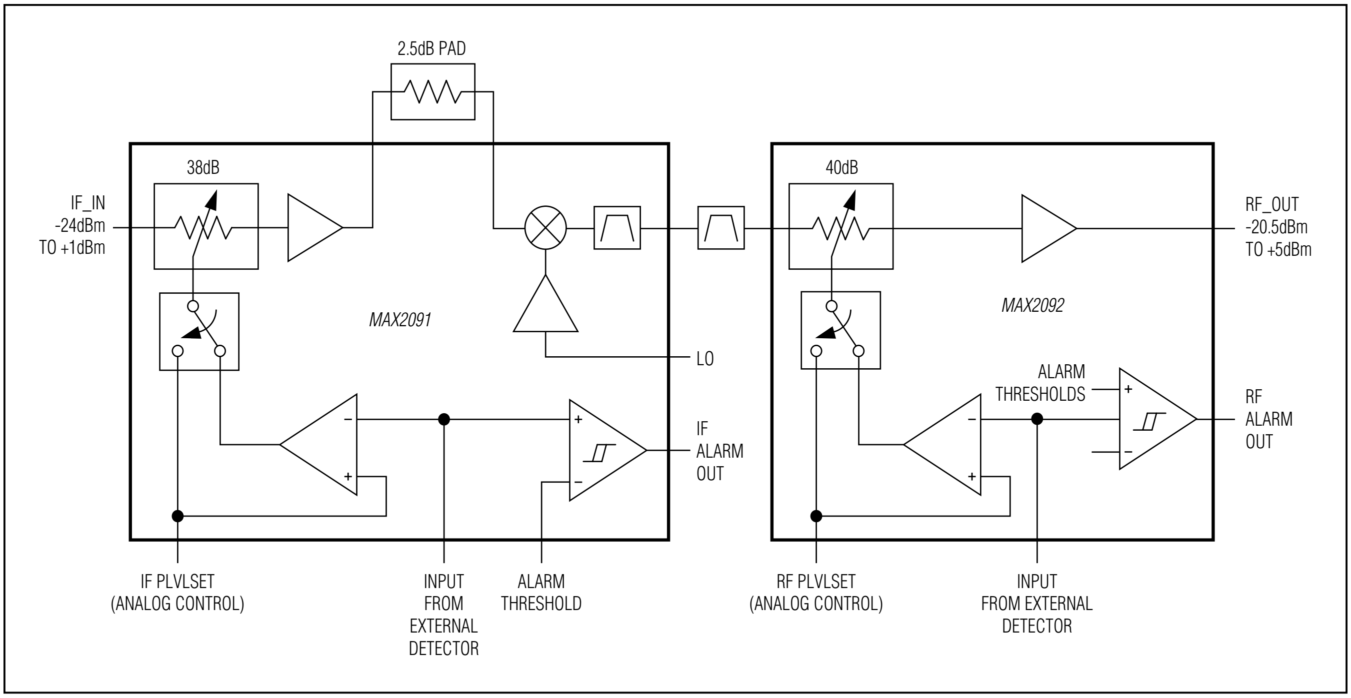


Figure 1. Cascaded IF-RF Lineup Using the MAX2091 + MAX2092

DET_VIN

In closed ALC-loop mode, avoid directly loading pins AMP_OUT and DET_VIN with capacitance in excess of 10pF on each pin. In closed ALC-loop mode, this can cause ringing or instability in the power-control loop. As in any closed-loop system, one must be careful not to load DET_VIN or AMP_OUT with additional external circuitry. Therefore, it is suggested that in the closed-loop ALC mode, no additional connections be made to DET_VIN or AMP_OUT. AMP_OUT and DET_VIN support a total trace routing capacitance of 10pF or less. Connect pin 9 to the RF ground plane with a via separated from the exposed pad (EP) ground connection. Pin 9 must not connect to the exposed pad or share a ground with any other component, and must connect directly to the solid ground plane below. As a reference, refer to the MAX2092EVKIT+ PCB artwork.

Layout Considerations

The pin configuration of the MAX2092 is optimized to facilitate a very compact physical layout of the device and its associated discrete components. The exposed pad of the device’s 20-pin TQFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the device is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes. Pin 9 must not connect to the exposed pad or share a ground with any other component and must connect directly to the solid ground plane below.

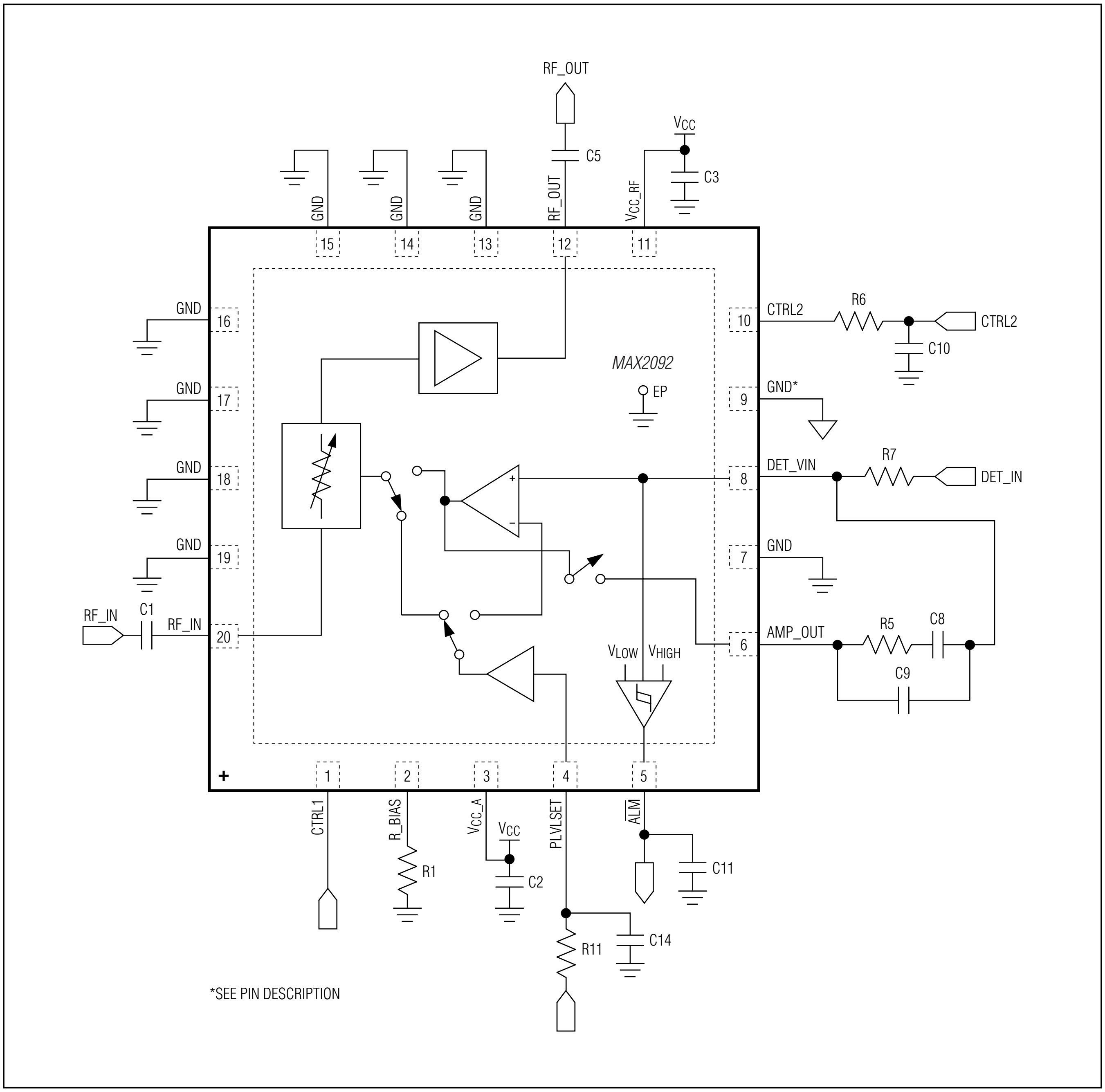
Table 2. Typical Application Circuit Component Values

COMPONENT	MODE OF OPERATION		VALUE	SIZE	VENDOR	DESCRIPTION
	VGA ONLY	CLOSED ALC				
C1	✓	✓	12pF	0402	Murata	C0G dielectric
C2, C3	✓	✓	0.01µF	0402	Murata	X7R dielectric
C5	✓	✓	8.2pF	0402	Murata	C0G dielectric
C8	—	✓	100nF	0603	Murata	X7R dielectric
C9	—	✓	680pF	0402	Murata	C0G dielectric
C10	—	✓	120pF	0402	Murata	C0G dielectric
C11	—	✓	120pF	0402	Murata	C0G dielectric
C14*	—	—	Do not install	0402	—	—
R1	✓	✓	1.78kΩ	0402	Panasonic	1% tolerance
R5	—	✓	200Ω	0402	Panasonic	1% tolerance
R6	—	✓	51Ω	0402	Panasonic	5% tolerance
R7	—	✓	10kΩ	0402	Panasonic	5% tolerance
R11*	✓	✓	0Ω	0402	Panasonic	5% tolerance
U1	✓	✓	—	20-pin TQFN (5mm x 5mm)	Maxim	MAX2092ETP+

Note: *The checkmarks in the Mode of Operation columns indicate that the component is used within each respective application.*

**C14 and R11 form an optional lowpass network to filter out potential noise from the external PLVLSET control source.*

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2092ETP+	-40°C to +95°C	20 TQFN-EP*
MAX2092ETP+T	-40°C to +95°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
**T = Tape and reel.*

Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN	T2055+3	21-0140	90-0008

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/12	Initial release	—
1	7/15	Removed military reference from *Applications* and updated the *Benefits and Features* section	1

