

General Description

The DVRFM631DF18N50 and DVRFM631DF12N100 development boards are general purpose circuit boards designed to simplify the evaluation of the IXZ631DF18N50 and IXZ631DF12N100 combination gate driver and MOSFET module and to provide a building block for power circuit development. While the circuit board is the same, either a 500 V or 1000 V MOSFET is available and is factory installed and fully tested. The board design allows the module to be mounted to a heat sink, and in doing so allows the board assembly to be used as a ground referenced, low-side power switch.

Figures 1 and 2 are top and bottom side pictures of the development board. The low-level input signal SMB connector and companion test point are shown to the left. If no SMB cable is available then the test point can be used as an alternative input connection. Continuing to the right of the SMB connector is the GND or ground and Vcc supply voltage test points, open pad drain connection and open pad for general component mounting.

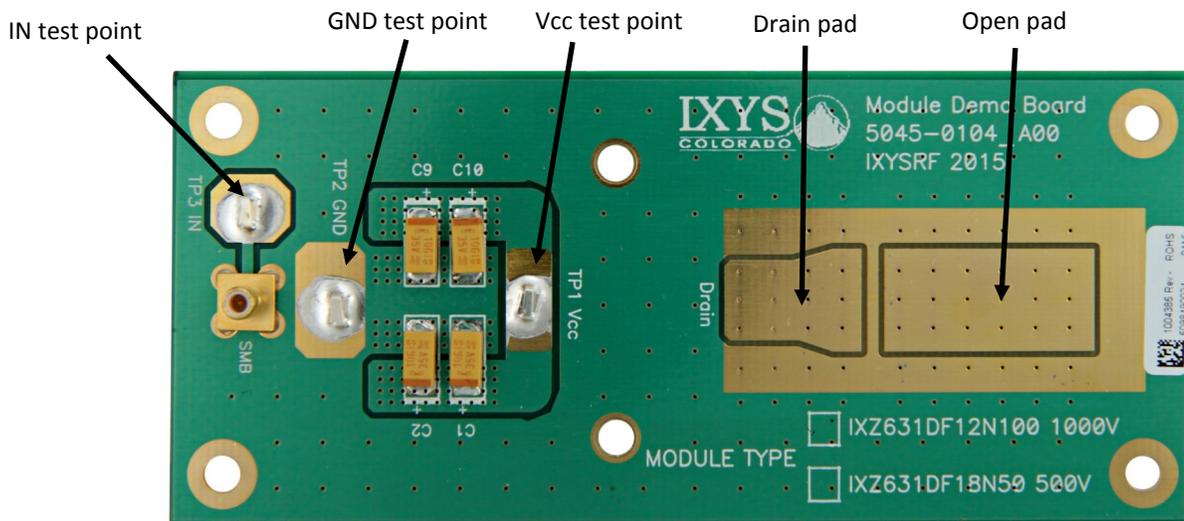


Figure 1 Top side of development board

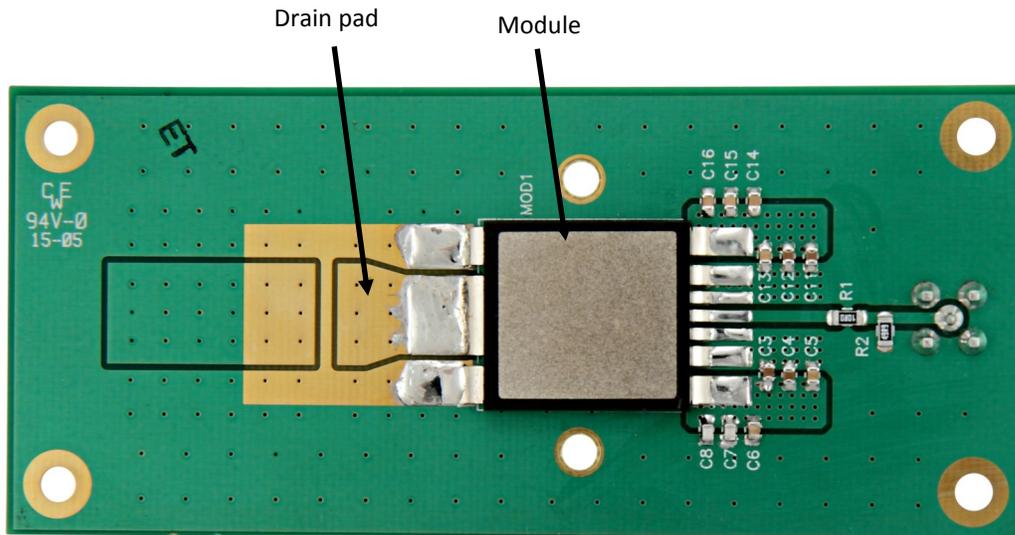


Figure 2 Bottom side of development board

Mounting Orientation

If heat is expected to be generated in a high frequency application, then thermal grease can be applied to the bottom of the module and the board mounted to a heatsink. Figure 3 shows application of thermal grease and Figure 4 shows mounting to a heatsink using the two mounting holes adjacent to the module. Avoid using too much thermal grease, maximum screw torque should not exceed 6 n-M to prevent flexing of the board. If corner holes are to be used to secure the board, spacers should be inserted between board and heatsink to prevent bending of the board. If heavy components are to be mounted on board, then spacers on the corners should be considered to support additional weight. You do not want the board to bend enough to short out against the heatsink.

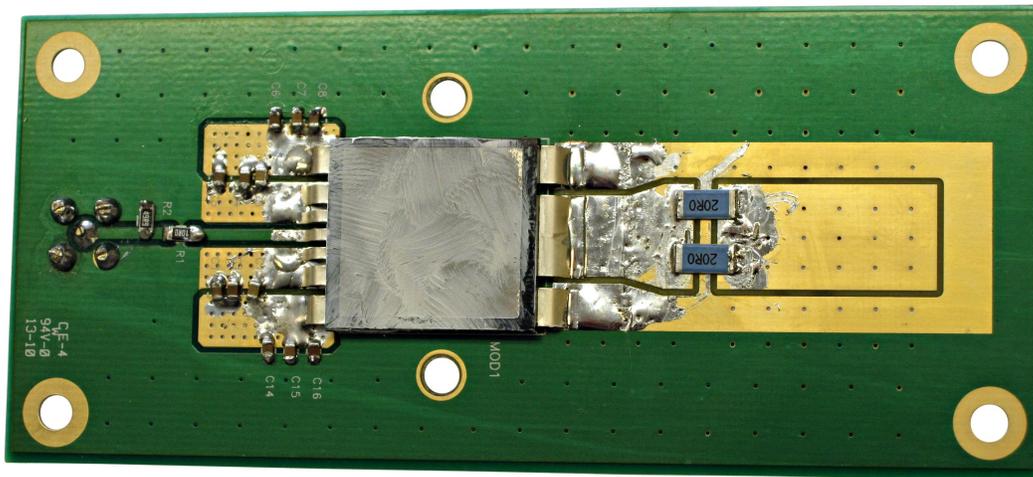


Figure 3 Application of thermal grease

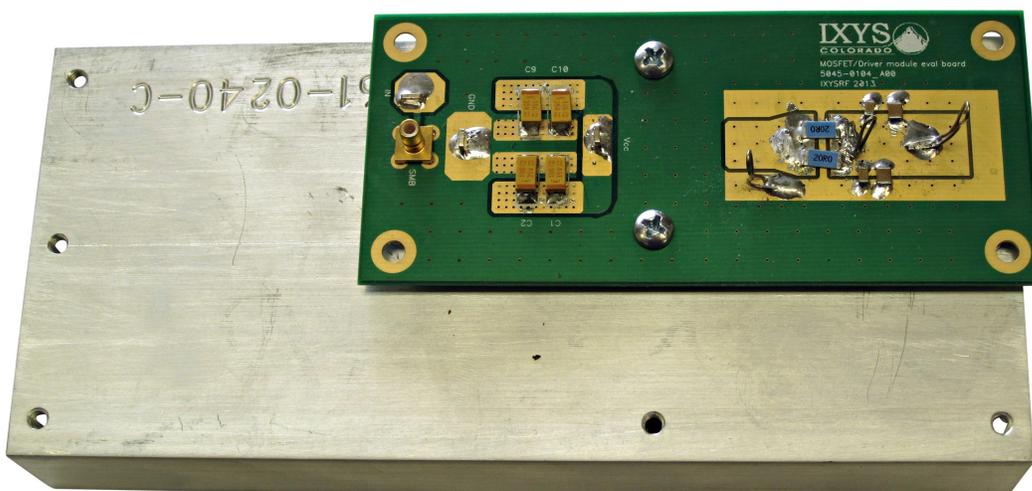
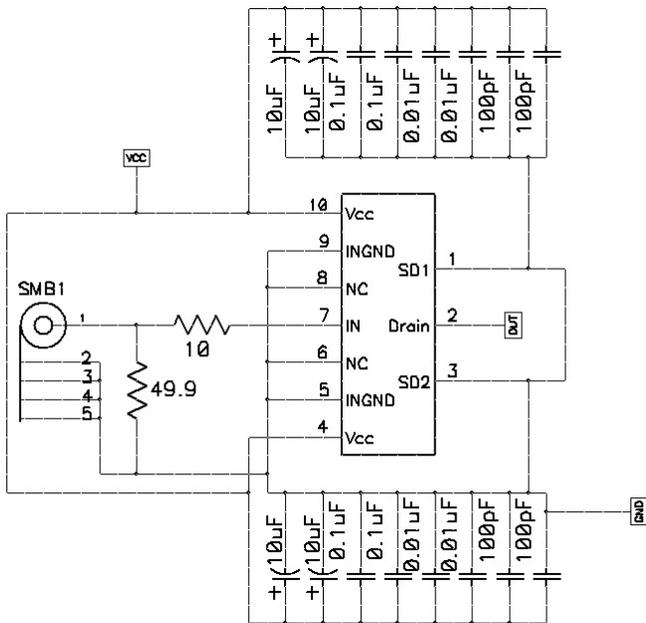


Figure 4 Board mounted to heatsink**

**Heatsink shown is not provided.

Circuit Description

The schematic diagram for the demonstration board is shown in Figure 5 below. The schematic includes the IXRFD630 gate driver die, either a 500 V or 1000 V MOSFET die, input protection and impedance matching resistors, bulk capacitance and bypass capacitance. The bulk capacitance provides local energy storage for the high current needed during a switching event, while the bypass capacitance provide local power supply decoupling at the device.



Test Point	Function
SMB / IN	Input Signal 0 to +5 V into 50 Ω
Vcc	Driver Power Supply (8 V-15 V)
GND	Circuit Ground Test Point
Drain Pad	V _{DS} Connection to Drain

Figure 5 Schematic diagram and test point table

The SMB connector is used to supply an input signal. The IN test point can also be used if no cables are available with an SMB style connector. Test points are as follows: Vcc supply voltage, IN input signal, GND ground for entire board. It is suggested to operate Vcc for the driver section at 12 V for general operation.

The series 10 Ω resistor at the input serves to limit input current but is not mandatory for all driver applications; it is more for input protection. The 49.9 Ω resistor loads the typical 50 Ω output impedance of most bench top signal generators. The input of the gate driver can operate without R1 and R2, where R2 can be removed, if desired, in the case that the input signal generator can't support the loading. In most cases the output level of the signal generator will have to be increased in order to compensate for the input loading. The typical threshold for the input signal is 3.2 V positive going with a negative going 0.2 V hysteresis voltage.

The four 10 μF tantalum bulk storage capacitors provide energy storage local to the driver. During switching of the output stage of the driver, parasitic inductance of the bond wires and traces between the power supply and driver can inhibit fast delivery of energy to the driver. This will result in a voltage drop along the inductance and will cause the voltage at the Vcc pins to sag. To counter this, large-valued bulk storage capacitors are placed close to the Vcc pins of the driver to supply energy right at the driver pins. Tantalum capacitors are used and suggested for use as they can release their stored energy very quickly into the Vcc pins. Aluminum electrolytic capacitors are not used or recommended for bulk storage capacitors due to their high values of ESR, or Equivalent Series Resistance, that slows energy delivery.

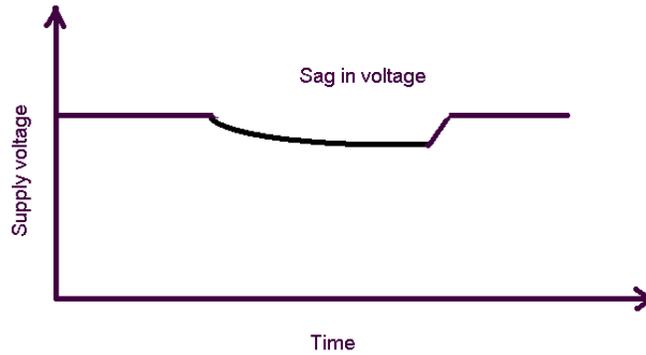


Figure 6– Sag in supply voltage at Vcc pins due to high series resistance from bulk storage capacitors

The network of bypass capacitors includes a wide spread in values: 0.001 μF , 0.01 μF , and 0.1 μF . The purpose of the capacitance spread is to produce overlapping response curves that lower the insertion impedance over a wider band. The bypass capacitors can be viewed as low-pass filters, but the generally ignored series inductance causes a notch or V-shaped response in the impedance curve as frequency goes up.

Figures 7 through 10 represent the progression of a single ideal capacitor response to the parallel combination of multiple capacitor networks.

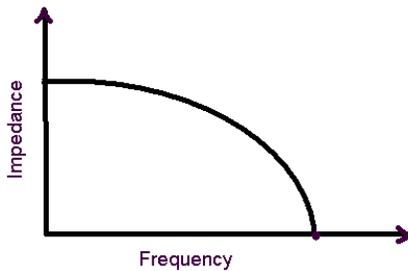


Figure 7– Ideal capacitor frequency response

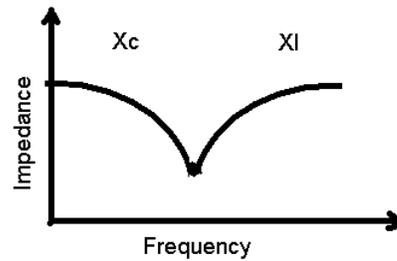


Figure 8– Capacitor frequency response due to self inductance

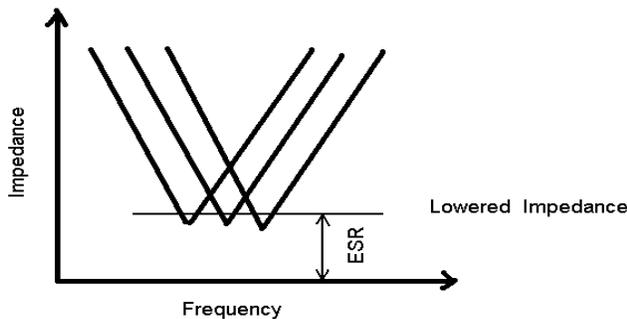


Figure 9– Over-lapping impedance curves

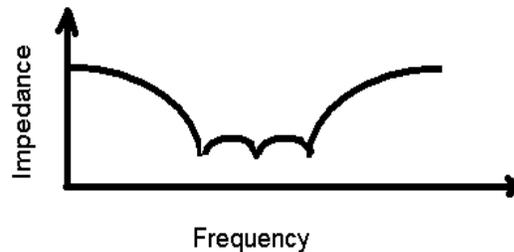


Figure 10– Broadband impedance lowered

Board Connections

Figure 11 shows connections to the board to operate it and includes V_{cc} for the driver section, input signal to drive the module, and V_{DS} drain to source voltage. The supply voltage for the drain is fed through some current limiting resistors using the open pad to drain pad path to supply voltage to the drain. The value of the current limiting resistors are random in this case and are only for demonstration purposes. Various wire leads have been soldered to the board to facilitate test lead and scope probe connections to the board.

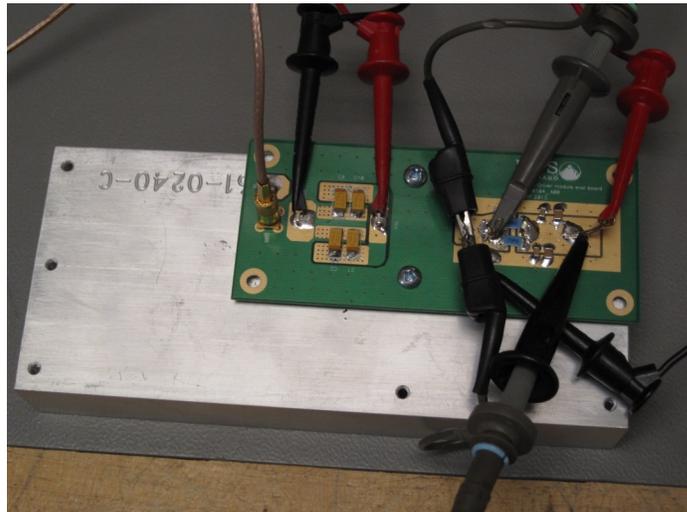


Figure 11 Demonstration board mounted to heat-sink

This note is intended to demonstrate basic functionality of the module in pulse-by-pulse setting and in a non-optimized circuit operating at a very low frequency, voltage and duty cycle. Using clip-on test leads may not work too well trying to run the above circuit at 13.56 MHz or something similar. For this circuit V_{cc} for the driver section is at 12V with V_{DS}, or drain voltage, at 40 V. Four parallel 20 Ω resistors act as a 5 Ω current limit and are in series with the drain and the V_{DS} supply voltage. Figure 12 is a close-up picture detailing the various connections.

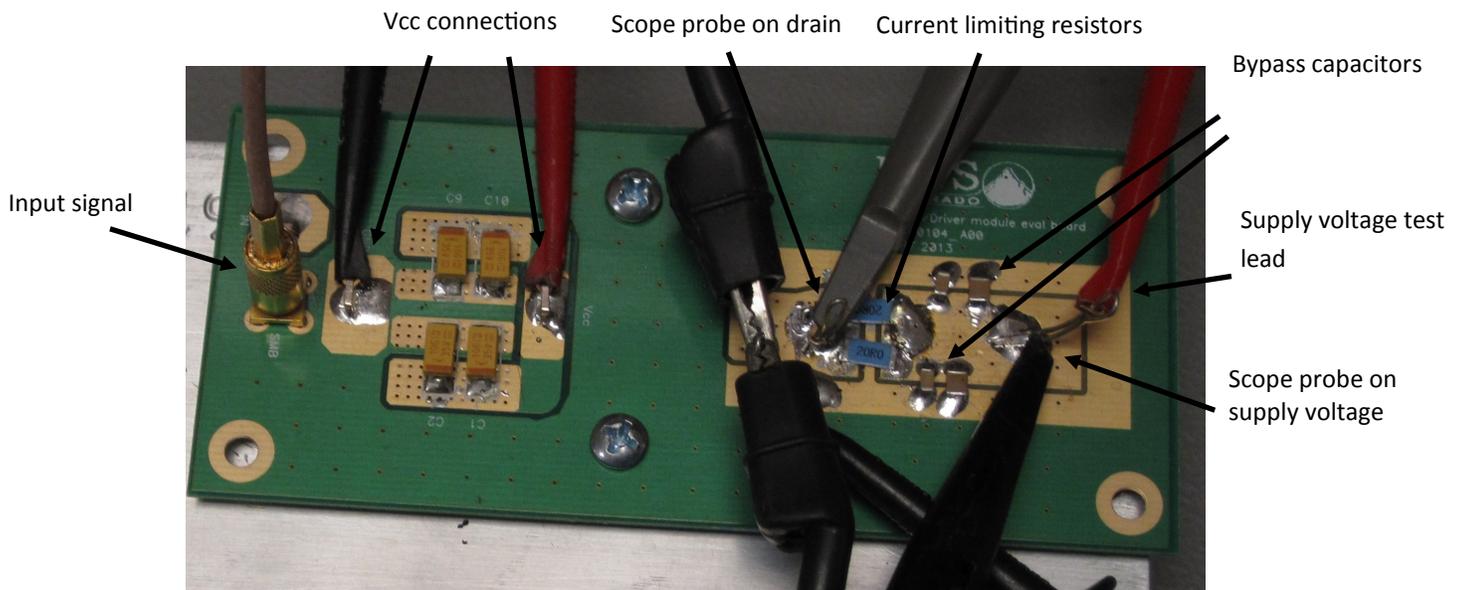


Figure 12 Board connections

Board Operation

The demonstration board was operated at the following values.

$V_{CC} = 12\text{ V}$

$V_{DS} = 40\text{ V}$

$F_{IN} = 100\text{ Hz}$

Pulse width = 100 ns

Channel 1 scope probe placed at the drain

Channel 2 scope probe placed at V_{DS} supply voltage.

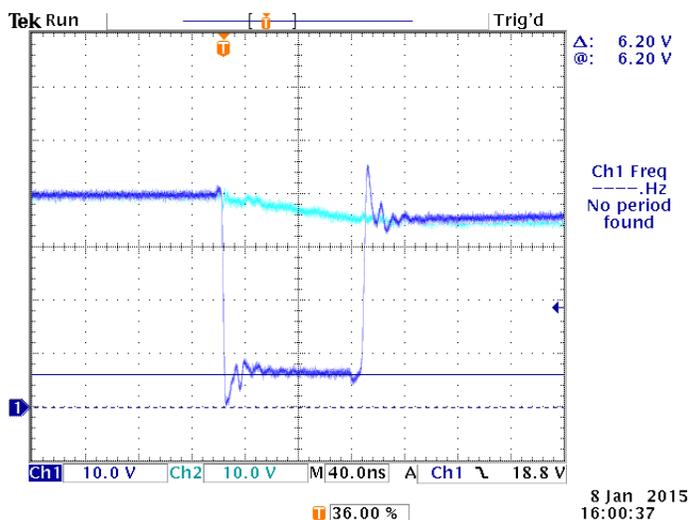


Figure 13 Single pulse event

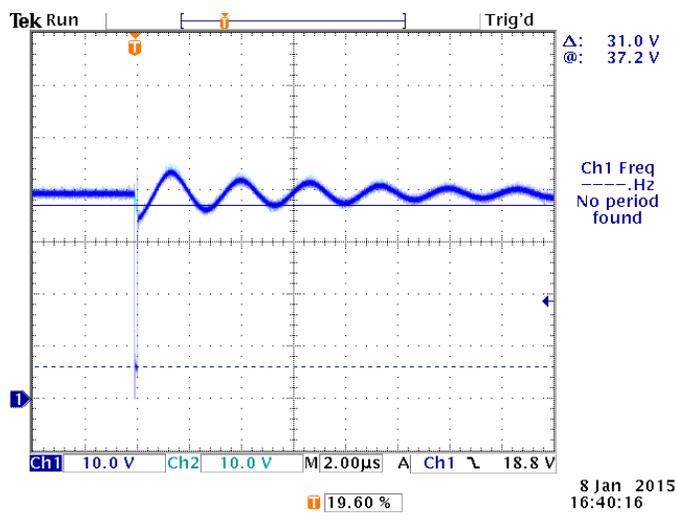


Figure 14 Supply voltage ringing

Operational Results

Figure 13 represents the voltage across the current limiting resistors, which will be used to calculate the various parameters during the pulse event. The channel 2 probe is placed on the supply voltage while channel 1 probe is placed on the drain. During the pulse, the difference between the two probes is the voltage across the current limiting resistors. We can see that there is approximately 30 V between the two probes, and 30 V divided by 5 Ω equals 6 A of drain current. We can now use that current to estimate the drain to source resistance of the MOSFET. Figure 13 also shows that there is 6 V between the bottom of the pulse and ground, which is the voltage across the drain to source resistance or $R_{DS(on)}$. Dividing 6 V by 6 A results in 1 Ω of drain resistance which confirms the datasheet values of 1 ohm for the 1000 V MOSFET used in this particular module.

It was previously indicated that this was a non-optimized circuit, primarily to avoid a complex circuit in developing this application note. Since no bulk capacitance is used with the drain voltage, we notice that the power supply voltage sags during the pulse in Figure 13 and results in a downward sloped trace during the pulse. When the drain is turned off in Figure 14 we see that the supply voltage rings against the parasitic inductance of the circuit. Adding bulk capacitance helps to reduce power supply sag due to the load placed on the supply while by-pass capacitance helps to decouple the V_{CC} pins of the driver. The values of bypass capacitors are closely related to circuit performance. Parasitic inductance is a characteristic of any circuit board and high drive currents cause high frequency ringing to occur at the corners of the rising or falling edge of the output signal as a result of this inductance. Ringing can range 20 - 50 MHz typically, so capacitor values are selected to roll off in this range. Each bypass capacitor is considered its own network with associated frequency response; replacing the individual capacitors with an equivalent capacitor of the total combined value does not have the same effect.



DVRFM631DF18N50 Development Board
DVRFM631DF12N100 Development Board

Ordering Information	
Part Number	MOSFET Installed
DVRFM631DF18N50	500 V, 18 A
DVRFM631DF12N100	1000 V, 12 A



An  IXYS Company

1609 Oakridge Dr., Suite 100
Fort Collins, CO USA 80525
970-493-1901 Fax: 970-232-3025
Email: sales@ixyscolorado.com
Web: <http://www.ixyscolorado.com>

© 2015 IXYS RF