

PIC16C925/926 (Rev. B2 Silicon) Data Sheet Errata

The PIC16C925/926 Rev. B2 parts you have received conform functionally to the Device Data Sheet (DS39544A), except for the anomalies described below.

Revision B2 parts can be identified by the following package markings:

- PIC16LC926-I/PTC03
- PIC16C926-I/PTC02
- PIC16LC926-I/LC03
- PIC16C926-I/LC02

In addition, any PIC16C925/926 part with a date code of 0336XXX and later is B2 silicon.

All the problems listed here will be addressed in future revisions of the PIC16C925/926 silicon.

None.

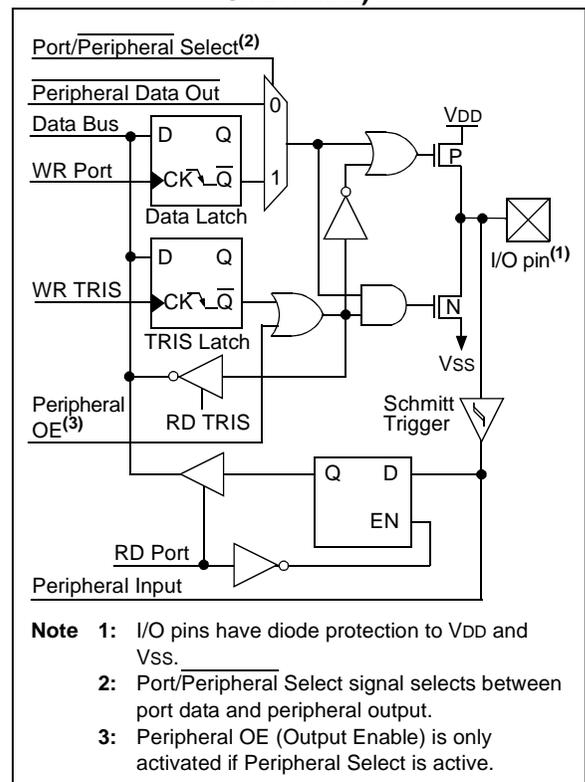
Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39544A), the following clarifications and corrections should be noted.

1. Module: I/O Ports

The block diagram for PORTC presented in Figure 4-5 of the Device Data Sheet (DS39544A) is incorrect. The correct block diagram is shown in Figure 1.

FIGURE 1: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



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2. Module: Memory (Special Function Registers)

The locations of the Special Function Registers, PMADR and PMDATH, are transposed throughout the Device Data Sheet. Specifically, PMADR is located at address 18Eh and PMDATH is located at address 18Dh.

This correction applies to the following specific locations, as well as anywhere else in the data sheet where the addresses of these registers may be referenced:

- Figure 2-3, page 13 (Register File Map – PIC16C925)
- Figure 2-4, page 14 (Register File Map – PIC16C926)
- Table 2-1, page 18 (Special Function Register Summary)
- Table 3-1, page 28 (Registers Associated with Program Memory)

3. Module: LCD

The illustrations of the LCD segment connections, their drive waveforms in various modes and their descriptive titles, have been revised. The changes have been made to make the illustrations and mode descriptions more consistent with those shown for the PIC16C923/924 family of devices in DS30444E.

The diagrams in Figure 11-2 through Figure 11-5 (below and the following pages) replace the corresponding diagrams in the Device Data Sheet (DS39544A).

FIGURE 11-2: WAVEFORMS IN STATIC DRIVE

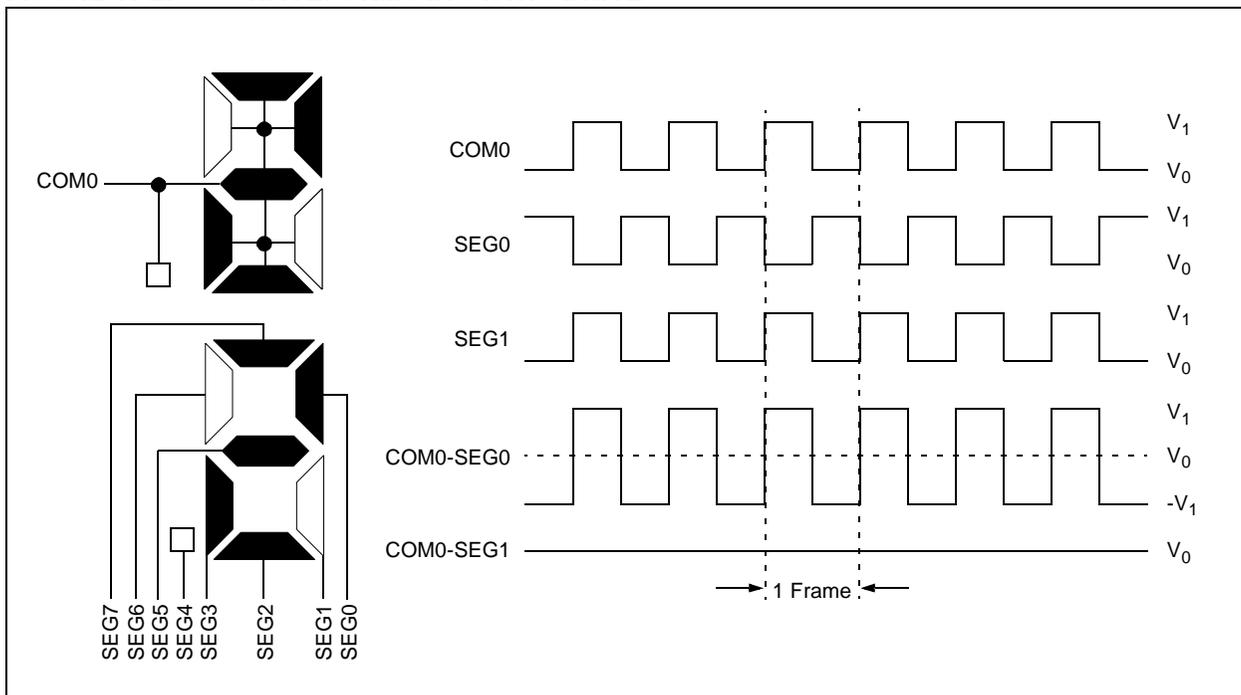
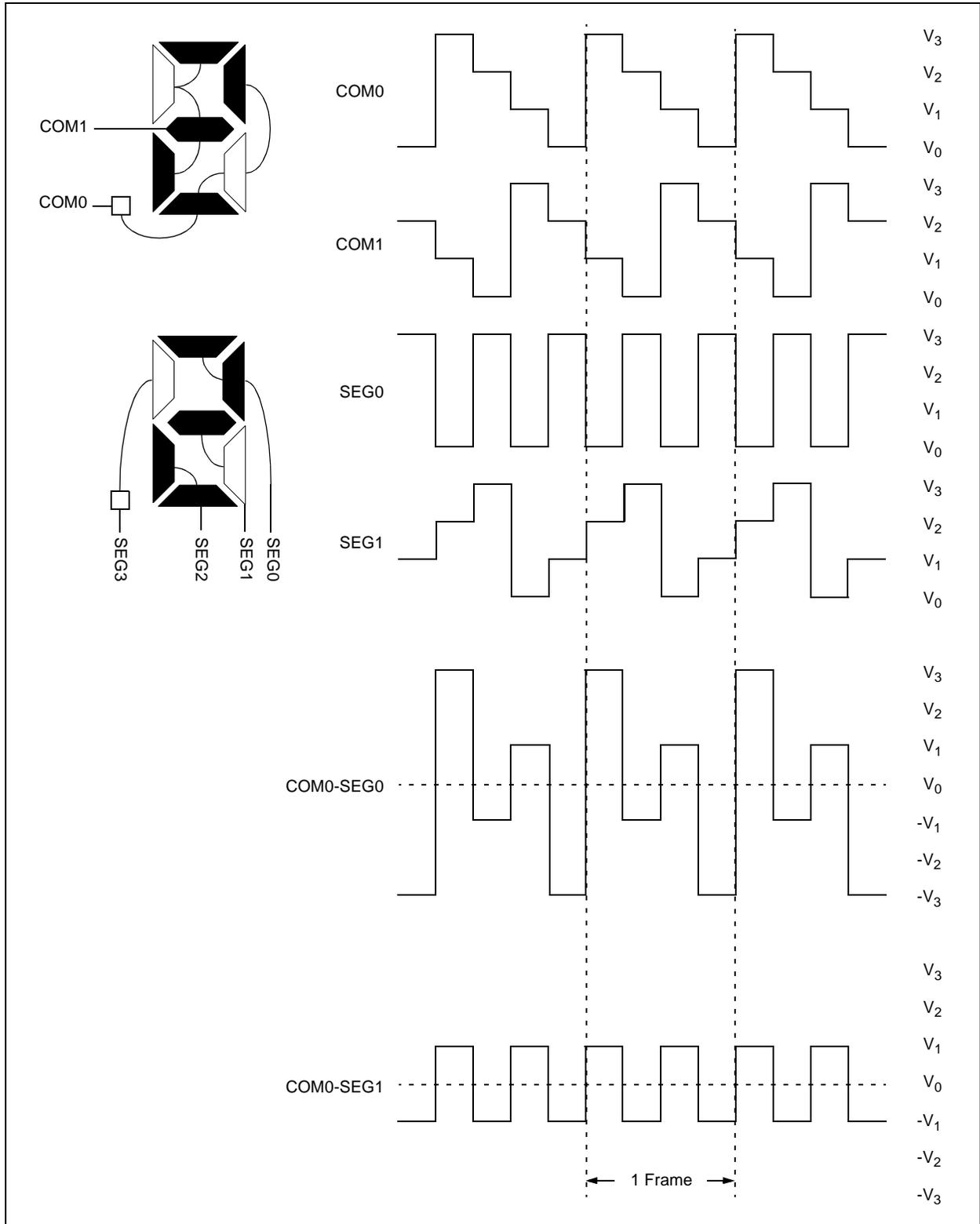


FIGURE 11-3: WAVEFORMS IN 1/2 MUX, 1/3 BIAS DRIVE



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FIGURE 11-4: WAVEFORMS IN 1/3 MUX, 1/3 BIAS

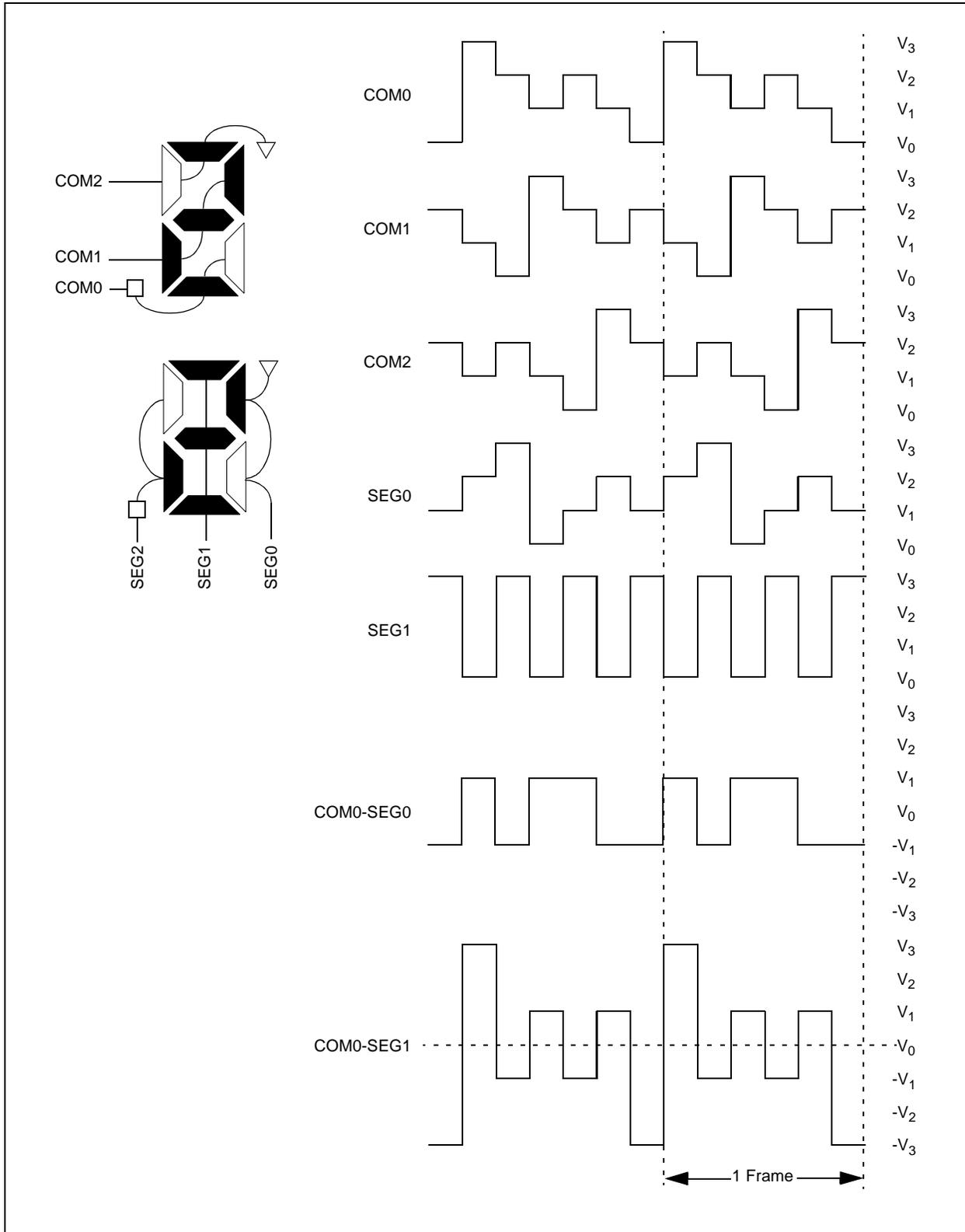
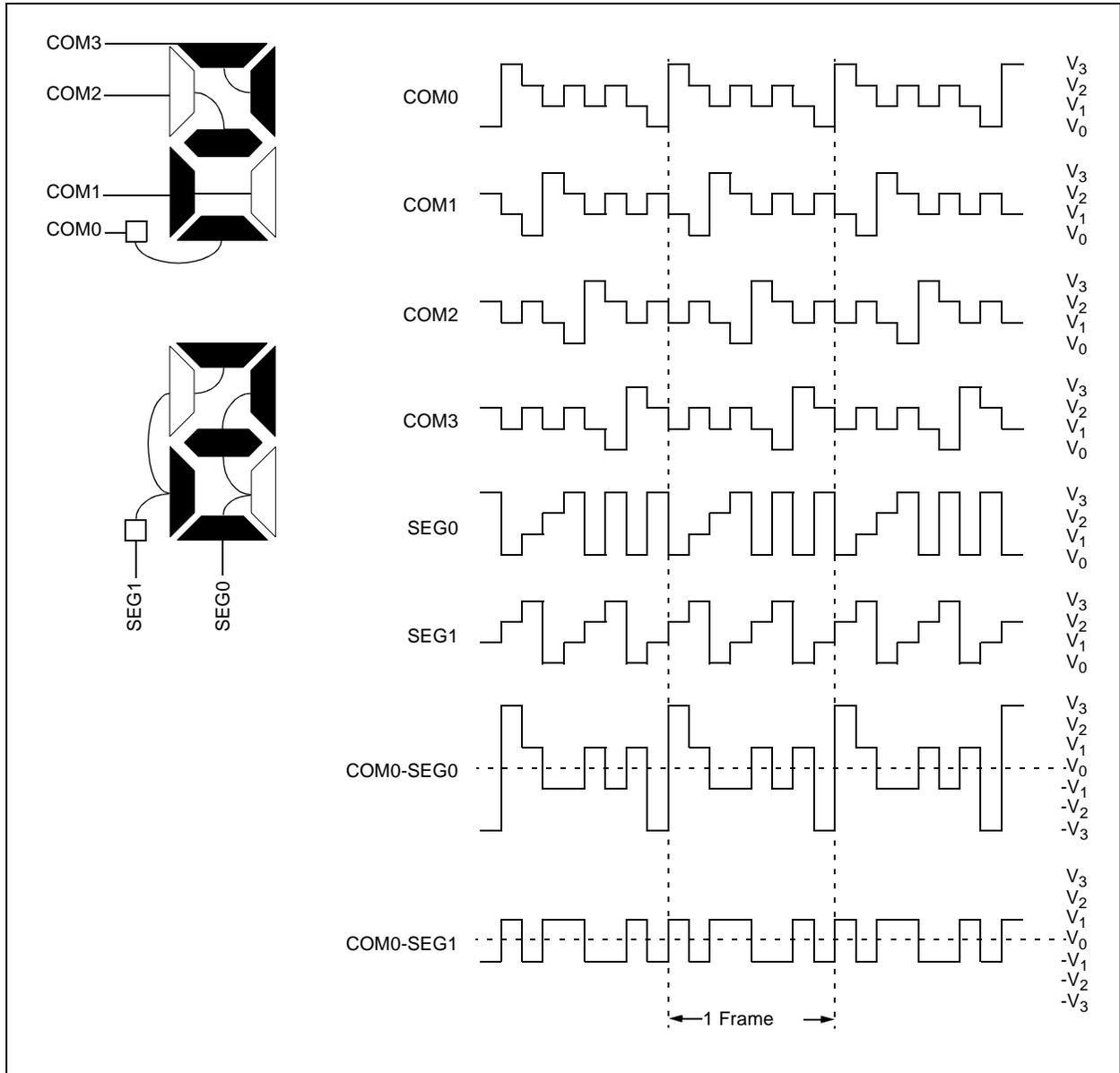


FIGURE 11-5: WAVEFORMS IN 1/4 MUX, 1/3 BIAS



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4. Module: LCD

The following text has been added to Section 11.5.1, "CHARGE PUMP":

The current source associated with the LCD module charge pump has a nominal output of 10 μA (see Figure 11-9). However, current regulation within individual devices may vary from approximately 7 to 15 μA . Since this current sets up the VLCDADJ voltage, variation in this current can create noticeable LCD contrast variations when using the LCD charge pump.

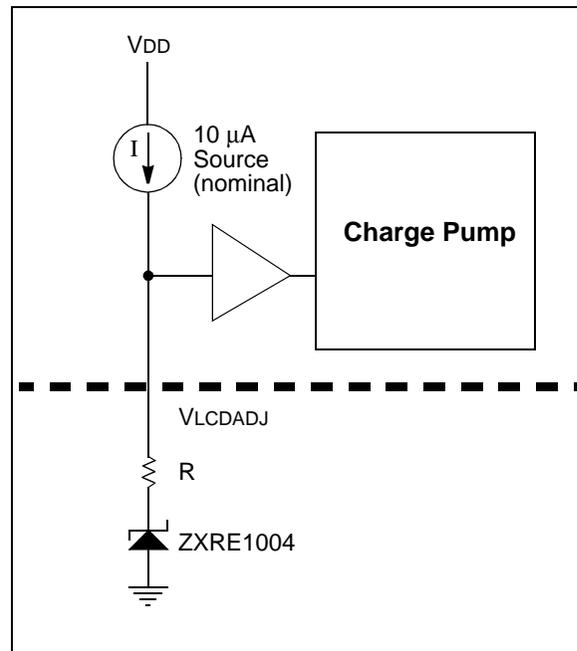
One method to compensate for the varying current regulation is to include a trim potentiometer in series between the VLCDADJ pin and ground. This method is currently noted in Figure 11-9 (page 95) of the Device Data Sheet.

To reduce the variation in the VLCDADJ voltage, without using a trim potentiometer or trim resistors (which must be manually adjusted), it is possible to use a band gap voltage reference circuit such as the 1.22V ZXRE1004 reference from Zetex, as shown in Figure 2. Resistor Rx placed in series with the band gap reference and the VLCDADJ pin can be used to set a voltage higher than the band gap reference voltage, if necessary. The voltage is determined by the formula:

$$V_{\text{LCDADJ}} = 1.22\text{V} + (I \times R)$$

As can be seen from this equation, a smaller series resistor, R, results in smaller variations in VLCDADJ voltage.

FIGURE 2: ALTERNATE METHOD FOR REDUCING VARIATIONS IN VLCDADJ VOLTAGE



5. Module: VLCD Charge Pump

Parameter D250 in Table 15-2 of the Device Data Sheet has been updated to include the minimum and maximum values for IVADJ. Changes to the table are shown in bold text.

TABLE 15-2: VLCD CHARGE PUMP ELECTRICAL SPECIFICATIONS

Parameter No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions	
D250	IVADJ	VLCDADJ Regulated Current Output	7	10	15	μA		
D252	Δ IVADJ/Δ VDD	VLCDADJ Current VDD Rejection	—	—	0.1	μA/V		
D265	VVADJ	VLCDADJ Voltage Limits	PIC16 C 925/926	1.0	—	2.3	V	
			PIC16 LC 925/926	1.0	—	V _{DD} – 0.7V	V	V _{DD} < 3V

6. Module: Timer1 Oscillator

Timer1 oscillator operating current has been improved on revision B2 devices. Section 15-1 has been updated to show the current typical and maximum values for parameter D025. Changes to the table are shown in bold text.

15.1 DC Characteristics

PIC16LC925/926 (Commercial, Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for industrial 0°C ≤ T _A ≤ +75°C for commercial					
PIC16C925/926 (Commercial, Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for industrial 0°C ≤ T _A ≤ +75°C for commercial					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D025	ΔI _{T1OSC}	Timer1 Oscillator PIC16LC925/926	—	3	6	μA	V _{DD} = 3.0V
D025		Timer1 Oscillator PIC16C925/926	—	5	10	μA	V _{DD} = 5.0V

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested and apply only to revision B2 silicon.

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APPENDIX A: REVISION HISTORY

Rev A Document (9/2003)

First revision of this document, Data Sheet Clarification issues 1 (I/O Ports), 2 (Memory), 3 (LCD), 4 (LCD), 5 (VLCD Charge Pump) and 6 (Timer1 Oscillator).

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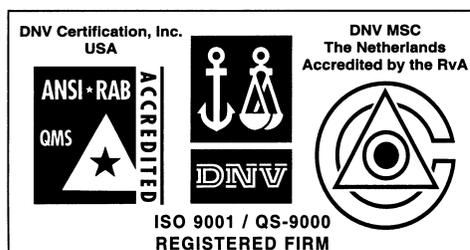
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