



# Spread Spectrum Clock Generator

#### **Features**

- Generates a 1x (PCS3P25811), 2x (PCS3P25812) and 4x(PCS3P25814) low EMI spread spectrum clock of the input frequency
- Provides up to 15dB of EMI suppression
- Input Frequency: 4MHz 32MHz
- Output Frequency:

PCS3P25811: 4MHz - 32MHz PCS3P25812: 8MHz - 64MHz PCS3P25814: 16MHz - 128MHz

- Selectable spread options: Down Spread and Center Spread
- Low Power Dissipation:

3.3V: 20mW (typ) @ 6MHz 3.3V: 24mW (typ) @ 12MHz 3.3V: 30mW (typ) @ 24MHz

- Low inherent Cycle-to-Cycle Jitter
- Supply Voltage: 2.8V to 3.6V
- LVCMOS Input and output
- Functional and Pinout compatible to Cypress CY25811, CY25812 and CY25814
- 8-pin SOIC, and 8L 2mmX2mm WDFN (TDFN) Packages

#### **Product Description**

The PCS3P25811/12/14 devices are versatile spread spectrum frequency modulators designed specifically for a wide range of input clock frequencies from 4MHz to 32MHz.

The PCS3P25811/12/14 reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data

dependent signals. It allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The PCS3P25811/12/14 can generate an EMI reduced clock from crystal, ceramic resonator, or system clock.

The PCS3P25811/12/14 modulate the output of a single PLL in order to "spread" the bandwidth of a synthesized cock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation.'

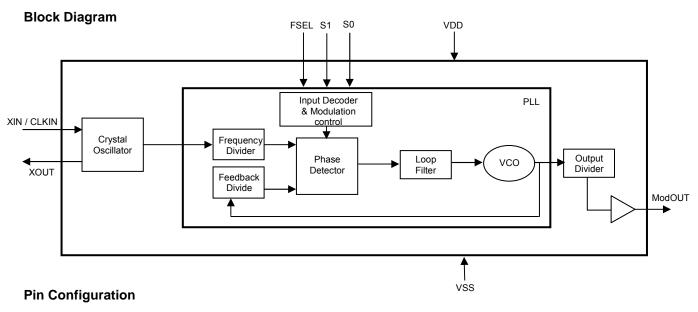
The PCS3P25811/12/14 use the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

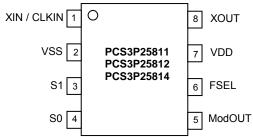
The PCS3P25811/12/14 have 2 pins S0 and S1 to control the selection of Center Spread, Down Spread and No-Spread functions. Additionally there is a 3 level logic contol FSEL, for selecting one of the three different frequency ranges within the operating frequency range. Refer *Input/Output Frequency Range Selection Table*.

The PCS3P25811/12/14 operate from a 2.8V to 3.6V supply and are available in 8 pin SOIC, and 8L 2mmX2mm WDFN packages.

#### **Applications**

The PCS3P25811/12/14 are targeted towards EMI management in applications such as LCD Panels, MFPs, Digital copiers, Networking, PC peripheral devices, consumer electronics, and embedded controller systems.





### **Pin Description**

FIII Des	scription						
Pin#	Pin Name	Туре	Description				
1	XIN / CLKIN	I	Crystal connection or External Clock input.				
2	VSS	Р	Ground to entire chip.				
3	S1	I	Digital 3 level logic input (1-M-0) used to select Center, Down and No spread options. (Refer to <i>Frequency Deviation Selection Table</i> ). Default=M.				
4	S0	I	Digital 3 level logic input (1-M-0) used to select Center, Down and No spread options. (Refer to <i>Frequency Deviation Selection Table</i> ). Default=M.				
5	ModOUT	0	Spread Spectrum Clock Output.				
6	FSEL	I	Frequency range select. Digital 3 level logic input (1-M-0) used to select Input Clock frequency range (Refer to <i>Input/Output Frequency Range Selection Table</i> ). Default=M.				
7	VDD	Р	Power supply for the entire chip (2.8V to 3.6V).				
8	XOUT	0	Crystal connection. If using an external reference, this pin must be left unconnected.				

Input/Output Frequency Range Selection Table

			Part N	lumber				
FSEL (pin 6)	PCS3P25811 (1x)		PCS3P25812 (2x)		PCS3P25814 (4x)		Modulation Rate	
	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)		
0	4-8	4-8	4-8	8-16	4-8	16-32	Input Frequency / 128	
1	8-16	8-16	8-16	16-32	8-16	32-64	Input Frequency / 256	
М	16-32	16-32	16-32	32-64	16-32	64-128	Input Frequency / 512	

**Output Frequency Deviation Selection Table** 

CLKIN	FSEL	S1=0 S0=0	S1=0 S0=M	S1=0 S0=1	S1=M S0=0	S1=1 S0=1	S1=1 S0=0	S1=M S0=1	S1=1 S0=M	S1=M S0=M
(MHz)	FSEL	Center	Center	Center	Center	Down	Down	Down	Down	No Spread
4-5	0	±1.4	±1.2	±0.6	±0.5	-3	-2.2	-1.9	-0.7	0
5-6	0	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
6-7	0	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
7-8	0	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0
8-10	1	±1.4	±1.2	±0.6	±0.5	-3	-2.2	-1.9	-0.7	0
10-12	1	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
12-14	1	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
14-16	1	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0
16-20	М	±1.4	±1.2	±0.6	±0.5	-3	-2.2	-1.9	-0.7	0
20-24	М	±1.3	±1.1	±0.5	±0.4	-2.7	-1.9	-1.7	-0.6	0
24-28	М	±1.2	±0.9	±0.5	±0.4	-2.5	-1.8	-1.5	-0.6	0
28-32	М	±1.1	±0.9	±0.4	±0.3	-2.3	-1.7	-1.4	-0.5	0

Note: Frequency Deviation given in the table is for the Input Frequency Range covering PCS3P25811/12 /14.

#### 3 Level Digital Logic

S0, S1, and FSEL digital inputs are designed to sense 3 different logic levels designated as High "1", Low "0" and Middle "M". With this 3-Level digital input logic 9 different logic states can be detected.

S0, S1 and FSEL pins include an on chip 100K (50K/50K) resistor divider. No external application resistors are

needed to implement the 3-Level logic levels as shown below:

Logic	Control Pins	VDD.
1	FSEL, S0, S1 to VDD	<del></del>
M	FSEL, S0, S1 UNCONNECTED	$\longrightarrow$
0	FSEL, S0, S1 to VSS	
		VSS

## **Operating Conditions**

Symbol	Parameter	Min	Max	Unit
VDD	Voltage on any pin with respect to VSS	2.8	3.6	V
T <sub>A</sub>	Operating temperature	0	+70	${\mathbb C}$
C <sub>L</sub>	Load Capacitance		15	pF
C <sub>IN</sub>	Input Capacitance		7	pF

**Absolute Maximum Ratings** 

Symbol	Parameter	Rating	Unit					
$V_{\text{DD}},V_{\text{IN}}$	Voltage on any pin with respect to Ground	-0.5 to +4.6	V					
T <sub>STG</sub>	Storage temperature	-65 to +125	C					
Ts	Max. Soldering Temperature (10 sec)	260	C					
TJ	Junction Temperature 150 ℃							
$T_DV$	T <sub>DV</sub> Static Discharge Voltage (As per JEDEC STD 22- A114-B) 2 KV							
Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.								

### **DC Electrical Characteristics**

Symbol		Parame	ter	Min	Тур	Max	Unit
VDD	Supply Voltage			2.8	3.3	3.6	V
	Input low voltage	Co	mmercial Temp.	0		0.15V <sub>DD</sub>	.,,
$V_{IL}$	(S0, S1, FSEL Inputs	s) Ind	dustrial Temp.	0		0.13 V <sub>DD</sub>	V
V <sub>IM</sub>	Input Middle Voltage	(S0, S1, FS	EL Inputs)	0.4VDD		0.60V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage (S	80, S1, FSEL	Inputs)	0.85VDD		$V_{DD}$	V
\ /	Output low voltage		I <sub>OL</sub> = 4mA			0.4	V
$V_{OL}$	(ModOUT Output)		I <sub>OL</sub> = 10mA			1.2	V
Van	V <sub>OH</sub> Output high voltage (ModOUT Output)		I <sub>OH</sub> = -4mA	2.4			V
VOH			I <sub>OH</sub> = -6mA	2			\ \ \
$C_{IN}$	Input Capacitance (>	KIN And XOL	JT)	6		9	pF
			XIN / CLKIN = 12MHz			8	
		Commercia Temp	XIN / CLKIN = 24MHz			10	mA
	Dynamic supply	Tomp	XIN / CLKIN = 32MHz			13	
I <sub>DD</sub>	current (Unloaded Output) Industrial Temp	XIN / CLKIN = 12MHz			10		
			XIN / CLKIN = 24MHz			12	mA
		Temp	XIN / CLKIN = 32MHz			15	
I <sub>CC</sub>	Static supply current	(XIN / CLKI	N pulled to VSS)			0.5	mA

Note. The voltage on any input or I/O pin cannot exceed the power pin during power up. All parameters are specified at Commercial and Industrial temperature unless stated otherwise.

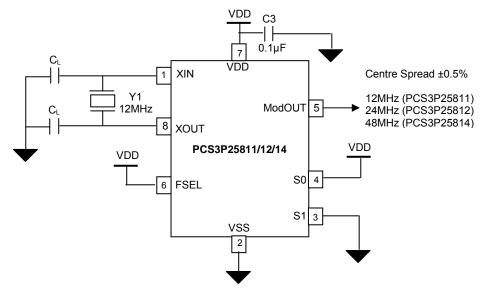
### **AC Electrical Characteristics**

Symbol	Parameter				Min	Тур	Max	Unit
f <sub>IN</sub>	Input Clock freque	ncy for PCS3	3P25811	/12/14	4		32	MHz
	ModOUT Clock fre	equency for F	CS3P25	5811	4		32	MHz
$f_{OUT}$	ModOUT Clock fre	equency for F	CS3P25	5812	8		64	MHz
	ModOUT Clock fre	equency for F	CS3P25	5814	16		128	MHz
1.2	ModOUT Rise time	Δ	PCS3F	P25811/12/14	2		5	
t <sub>LH</sub> <sup>1, 2</sup>	(Measured from 20	-		P25814 FSEL=M	1		2.2	nS
. 12	ModOUT Fall time		PCS3F	P25811/12/14	2		4.4	
t <sub>HL</sub> <sup>1, 2</sup>		(Measured from 80% to 20%) PCS3F		P25814 FSEL=M	1		2.2	nS
TDCIN	Input Clock Duty C	Cycle(XIN / C	ycle(XIN / CLKIN)				60	%
TDCOUT <sup>1, 2</sup>	Output Clock Duty	Cycle (ModOUT)			40		60	%
	Cy-Cy Jitter, For ModOUT with Spread ON (For Commercial temperature)	PCS3P25811		4MHz			600	
		Cy Jitter,	11	8MHz			450	pS
		PCS3P258	12	16MHz			400	
		For Commercial ————————————————————————————————————	12	32MHz			380	
$T_{JC}^2$			4.4	64MHz			380	
ı JC		PCS3P25814		128MHz			380	
	Cy-Cy Jitter, For ModOUT	PCS3P258	11	CLKIN = 6MHz			500	
	with Spread ON	PCS3P258		CLKIN = 12MHz			400	pS
	(For Industrial PCS3P temperature)		14	CLKIN = 24MHz			380	
	PLL Lock Time			Commercial			2	
$t_{\rm ON}^{2}$	(Stable power sup	ply, valid inp	ut clock	Temp.			_	mS
	to valid Clock on N	ModOUT)		Industrial Temp.			3	

Notes: 1.Parameters are specified with 15pF loaded outputs.

2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

### **Application Schematic**

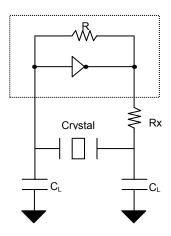


## **Typical Crystal Specifications**

Fundamental AT cut parallel resonant crystal						
Nominal frequency	12MHz					
Frequency tolerance	± 30 ppm or better at 25℃					
Operating temperature range	-25℃ to +85℃					
Storage temperature	-40℃ to +85℃					
Load capacitance(C <sub>P</sub> )	18pF					
Shunt capacitance	7pF maximum					
ESR	25 Ω					

Note: Note: C<sub>L</sub> is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

#### **Typical Crystal Interface Circuit**

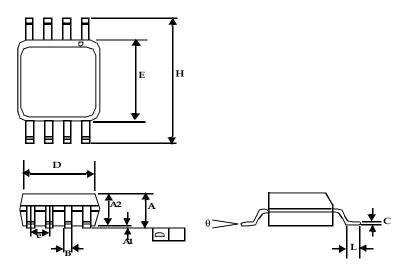


 $C_L = 2*(C_P - C_S),$ 

Where  $C_P$  = Load capacitance of crystal  $C_S$  = Stray capacitance due to  $C_{IN}$ , PCB, Trace etc.

## **Package Information**

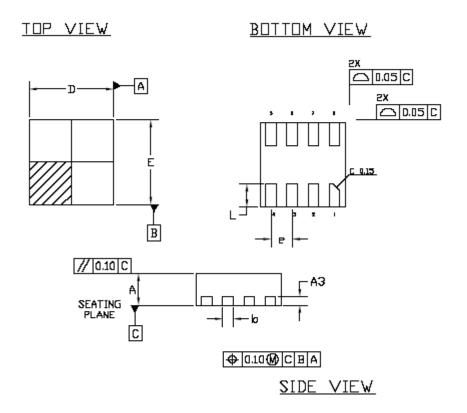
## 8-Pin SOIC Package



	Dimensions					
Symbol	Inc	hes	Millimeters			
	Min	Max	Min	Max		
A1	0.004	0.010	0.10	0.25		
Α	0.053	0.069	1.35	1.75		
A2	0.049	0.059	1.25	1.50		
В	0.012	0.020	0.31	0.51		
С	0.007	0.010	0.18	0.25		
D	0.193	BSC	4.90 BSC			
Е	0.154	BSC	3.91 BSC			
е	0.050 BSC		1.27 BSC			
Н	0.236 BSC		6.00 BSC			
L	0.016	0.050	0.41	1.27		
θ	0°	8° 0°		8°		

Note: Controlling dimensions are millimeters. SOIC: 0.074 grams unit weight.

## 8L 2mmX2mm WDFN package



	Dimensions						
Symbol	Inch	nes	Mill	imeters			
	Min	Max	Min	Max			
Α	0.027	0.0315	0.70	0.80			
A3	0.008	BSC	0.203 BSC				
b	0.008	0.012	0.20	0.30			
D	0.077	0.080	1.95	2.05			
Е	0.077	0.080	1.95	2.05			
е	0.020	BSC	0.50 BSC				
L	0.020	0.024	0.50	0.60			

**Ordering Code** 

Part Number Marking		Package Type	Temperature
PCS3P25811AG08SR	CGL	8-pin SOIC – Tape & Reel, Green	0℃ to +70℃
P3P25812AG-08SR	CIL	8-pin SOIC – Tape & Reel, Green	0℃ to +70℃
P3P25814AG-08SR	CKL	8-pin SOIC – Tape & Reel, Green	0℃ to +70℃
P3P25811AG-08CR	CG	8L-WDFN (2mmX2mm) - Tape & Reel, Green	0℃ to +70℃
P3P25812AG-08CR	CI	8L-WDFN (2mmX2mm) - Tape & Reel, Green	0℃ to +70℃
P3P25814AG-08CR	CK	8L-WDFN (2mmX2mm) - Tape & Reel, Green	0℃ to +70℃

A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. U.S Patent Pending; Timing-Safe and Active Bead are trademarks of PulseCore Semiconductor, a wholly owned subsidiary of ON Semiconductor. This literature is subject to all applicable copyright laws

#### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada

Fax: 303-675-2176 or 800-344-3867 Toll Free

USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5773-3850 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your

local Sales Representative