Doc No. TT4-EA-14177

Revision. 2

# **Panasonic**

MOS FET

### MTM231232LBF

### MTM231232LBF

#### Silicon P-channel MOSFET

#### For Switching

#### MTM76123 in SMini3 type package

#### ■ Features

- Low Drain-source On-state Resistance : RDS(on) typ. = 40 m $\Omega$  (VGS = -4 V)
- Low Drive Voltage: 2.5 V Drive
- Halogen-free / RoHS compliant

(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : BL

#### ■ Packaging

Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

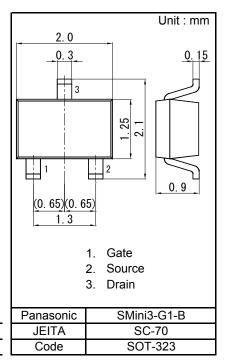
Absolute Maximum Ratings 14 - 25	0			
Parameter	Symbol	Rating	Unit	
Drain to Source Voltage	VDS	-20	V	
Gate to Source Voltage	VGS	±10	V	
Drain Current	ID	-3	Α	
Drain Current (Pulsed) *1	IDp	-16	Α	
Total Power Dissipation *2	PD	500	mW	
Channel Temperature	Tch	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

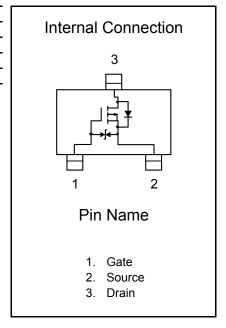
Note \*1 Pulse width  $\leq$  10  $\mu s,$  Duty cycle  $\leq$  1 %

Established: 2012-04-21

Revised

: 2013-03-07





 $<sup>^{*}2</sup>$  Measuring on ceramic board at 40 mm  $\times$  38 mm  $\times$  0.1 mm. Absolute maximum rating PD Non-heat sink shall be made 150 mW.

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#### ■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V
Zero Gate Voltage Drain Current	IDSS	VDS = -20 V, VGS = 0 V			-1	μΑ
Gate-source Leakage Current	IGSS	VGS = $\pm 8$ V, VDS = 0 V			±10	μΑ
Gate-source Threshold Voltage	Vth	ID = -1 mA, VDS = -10 V	-0.4	-0.85	-1.3	V
Drain-source On-state Resistance *1	RDS(on)1	ID = -1 A, VGS = -4 V		40	55	mΩ
	RDS(on)2	ID = -0.5 A, VGS = -2.5 V		45	70	
Forward transfer admittance *1	Yfs	ID = -1 A, VDS = -10 V, f = 1 kHz	3.5			S
Input Capacitance	Ciss	VDS = -10 V. VGS = 0 V		1 000		pF
Output Capacitance	Coss	f = 1 MHz		120		
Reverse Transfer Capacitance	Crss	1 - 1 WITZ		120		
Turn-on Delay Time *2	td(on)	VDD = -10 V, VGS = 0 to -4 V		25		no
Rise Time *2	tr	ID = -1 A		25		ns
Turn-off Delay Time *2	td(off)	VDD = -10 V, VGS = -4 to 0 V		120		ns
Fall Time *2	tf	ID = -1 A		70		

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

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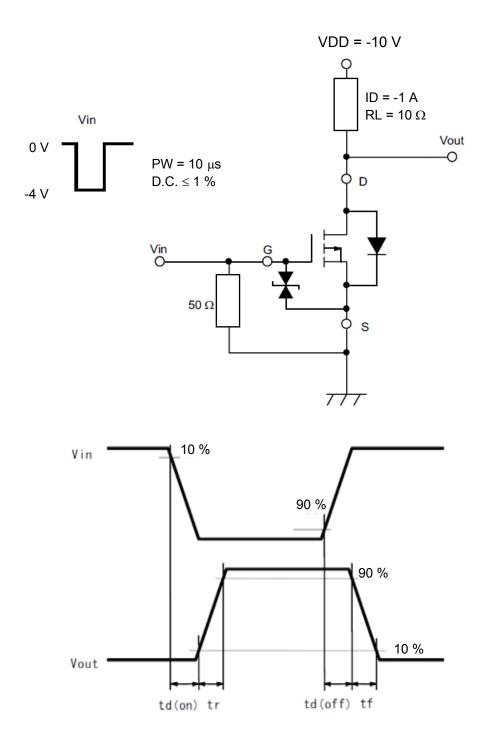
Established: 2012-04-21 : 2013-03-07 Revised

<sup>\*1</sup> Pulse test : Pulse width  $\leq 300~\mu s,$  Duty cycle  $\leq 2~\%$ 

<sup>\*2</sup> Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

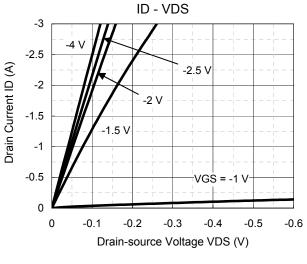
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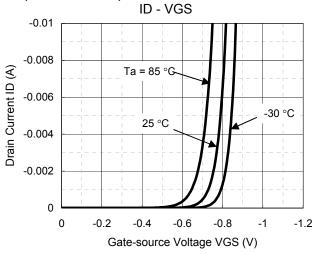
\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

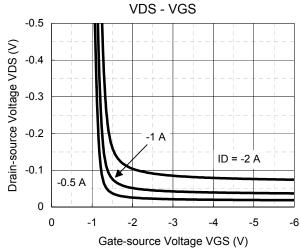


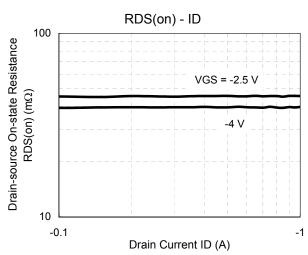
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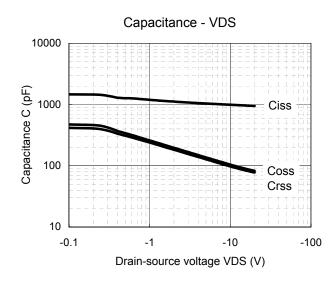
### Technical Data (reference)

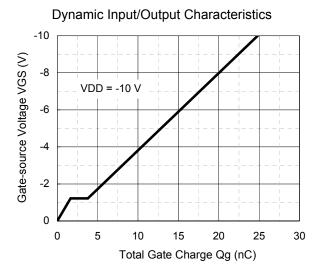








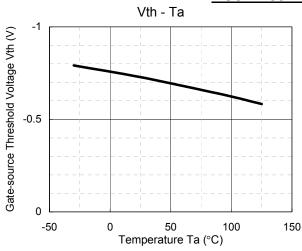


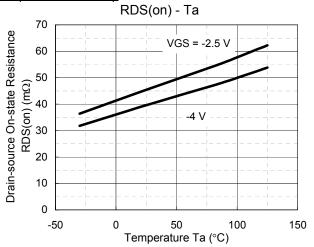


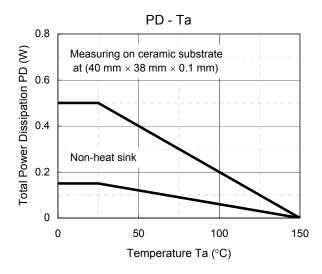
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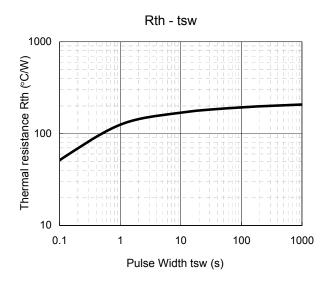
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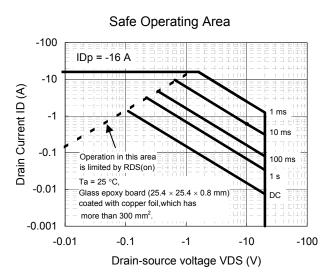
## Technical Data (reference)











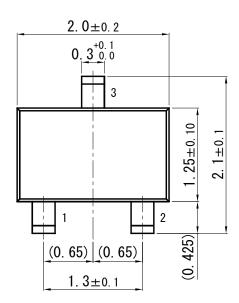
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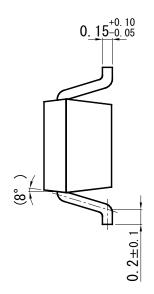
MOS FET

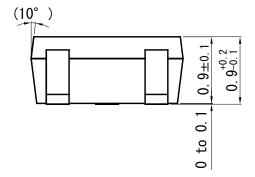
Unit: mm

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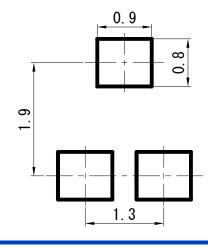
SMini3-G1-B







■ Land Pattern (Reference) (Unit : mm)



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Established: 2012-04-21 Revised: 2013-03-07

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